

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add device type -02 as a substitute for device type -01. Obsolete device type -01. Correct vendor datasheet errors for limits of V _{DD} , V _{OD} , and I _{OZ} parameters. Update boilerplate to current revision. - CFS	04-11-09	Thomas M. Hess
B	Add device type 03. - PHN	06-07-12	Thomas M. Hess
C	Update boilerplate paragraphs to current requirements. - PHN	12-07-23	Thomas M. Hess
D	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	19-03-12	Thomas M. Hess
E	Add device type 04. - PHN	20-09-17	Muhammad A. Akbar

**CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990**



Prepared in accordance with ASME Y14.24

Vendor item drawing

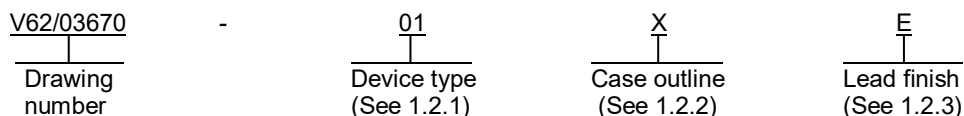
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REV STATUS OF PAGES	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
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PMIC N/A	PREPARED BY Charles F. Saffle	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing 03-08-19	CHECKED BY Charles F. Saffle	TITLE MICROCIRCUIT, DIGITAL, CMOS, THREE-PORT CABLE TRANSCEIVER/ARBITER, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/03670
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Three-Port Cable Transceiver/Arbiter microcircuit, with an operating temperature range of -40°C to +110°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01 <u>1/</u>	TSB41BA3-EP	Three-Port Cable Transceiver/Arbiter
02 <u>1/</u>	TSB41BA3A-EP	Three-Port Cable Transceiver/Arbiter
03	TSB41BA3B-EP	Three-Port Cable Transceiver/Arbiter
04	TSB41BA3F-EP	Three-Port Cable Transceiver/Arbiter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	80	JEDEC MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1/ Device type -02 is a substitute for the obsolete device type -01.

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1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{DD18}) DVDD-CORE, PLLVDD-CORE	-0.3 V to +2.1 V	<u>3/</u>
Supply voltage range (V_{DD33}) DVDD-3.3, PLLVDD-3.3, AVDD	-0.3 V to +4.0 V	<u>3/</u>
Input voltage range (V_{I33}) Sx, Sx_PCx, VREG_PD, PD, LPS, LREQ, LCLK, CTLx, Dx, CPS, SLPEN, <u>RESET</u> , BMODE, TESTM, SDx.....	-0.5 V to $V_{DD33} + 0.5$ V	<u>3/</u>
Output voltage range at any output (V_{O33}) PINT, PCLK, CTLx, Dx, LKON	-0.5 V to $V_{DD33} + 0.5$ V	<u>3/</u>
Analog I/O voltage range (V_A) TPAX, TPBx	-0.5 V to V_{DD33} V	<u>3/</u>
Reference voltage range (V_R) only R1 (R0 is internal ground reference)	-0.5 V to V_{DD33} V	<u>3/</u>
Clock input voltage range (V_X) XI, XO	-0.5 V to V_{DD18} V	<u>3/</u>
Absolute maximum junction temperature (T_J)	150°C	
Operating free-air temperature range (T_A):		
Device type 01 -04:	-40°C to +110°C	
Storage temperature range (T_{STG})	-65°C to +150°C	
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds.....	260°C	
Electrostatic discharge $V_{(ESD)}$		
Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000 V	<u>4/</u>
Charged-device model (CDM), per JEDEC specification JESD22-C1011	±500 V	<u>5/</u>

Dissipation rating table:

Case Outline	$T_A \leq 65^\circ\text{C}$ Power Rating	Derating Factor <u>6/</u> Above $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ Power rating	$T_A = 110^\circ\text{C}$ Power rating
Case X <u>7/</u>	5.05 W	52.5 mW/°C	2.69 W	587 mW
Case X <u>8/</u>	3.05 W	31.7 mW/°C	1.62 W	355 mW
Case X <u>9/</u>	2.01 W	20.3 mW/°C	1.1 W	284 mW

- 2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 3/ All voltage values, except differential I/O bus voltages, are with respect to network ground.
- 4/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- 5/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- 6/ This is the inverse of the traditional junction to ambient thermal resistance ($R_{\theta JA}$).
- 7/ 2 oz. trace and copper pad with solder.
- 8/ 2 oz. trace and copper pad without solder.
- 9/ For more information see manufacturer application report.

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1.4 Recommended operating conditions. 10/

Supply voltage range (3.3 V _{DD}):	
Source power node	+3.0 V to +3.6 V
Non-source power node	+3.0 V to +3.6 V 11/
Supply voltage range (1.8 V _{DD}) Core voltage	+1.75 V to +2.0 V
Minimum high level input voltage (V _{IH}):	
LREQ, CTL0, CTL1, D0-D7, LCLK_PMC	0.7xV _{DD33}
Device 01: S5_LKON_DS2, S4_DS1, S3_DS0, S2_PC0, S1_PC1, S0_PC2, SLPEN, PD, BMODE, TPBIAS0_SD0, TPBIAS1_SD1, TPBIAS2_SD2	0.7xV _{DD33}
Device 02, 03, 04: S5_LKON, S4, S3, S2_PC0, S1_PC1, S0_PC2, SLPEN, PD, BMODE, TPBIAS0_SD0, TPBIAS1_SD1, TPBIAS2_SD2	0.7xV _{DD33}
RESETz or RESET	0.6xV _{DD33} 12/
Maximum low level input voltage (V _{IL}):	
LREQ, CTL0, CTL1, D0-D7, LCLK_PMC	0.25xV _{DD33}
Device 01: S5_LKON_DS2, S4_DS1, S3_DS0, S2_PC0, S1_PC1, S0_PC2, SLPEN, PD, BMODE, TPBIAS0_SD0, TPBIAS1_SD1, TPBIAS2_SD2	0.2xV _{DD33}
Device 02, 03, 04: S5_LKON, S4, S3, S2_PC0, S1_PC1, S0_PC2, SLPEN, PD, BMODE TPBIAS0_SD0, TPBIAS1_SD1, TPBIAS2_SD2	0.2xV _{DD33}
RESETz or RESET	0.3xV _{DD33} 12/
Output current (I _{OL/OH}):	
Device 01: CTL0, CTL1, D0-D7, S5_LKON_DS2, PINT, PCLK	-4.0 mA to +4.0 mA
Device 02, 03, 04: CTL0, CTL1, D0-D7, S5_LKON, PINT, PCLK	-4.0 mA to +4.0 mA
Output current (I _O) (TPBIAS outputs)	-5.6 mA to +1.3 mA
Operating free-air temperature range (T _A)	-40°C to +110°C
Maximum junction temperature (T _J)	-40°C to +125°C
1394b Differential input voltage (V _{ID}):	
Cable inputs, during data reception	200 mV to 800 mV
1394a Differential input voltage range (V _{ID}):	
Cable inputs, during data reception	118 mV to 260 mV
Cable inputs, during arbitration	168 mV to 265 mV
1394a Common-mode input voltage (V _{IC}):	
TPB cable inputs, source power node	0.4706 V to 2.515 V
TPB cable inputs, non-source power node	0.4706 V to 2.015 V 11/
Minimum power-up reset time (t _(pu)) (RESETz or RESET input)	2 ms 12/ 13/
Maximum 1394a receive input jitter:	
TPA, TPB cable inputs, S100 operation	±1.08 ns
TPA, TPB cable inputs, S200 operation	±0.5 ns
TPA, TPB cable inputs, S400 operation	±0.315 ns
Maximum 1394a receive input skew:	
Between TPA and TPB cable inputs, S100 operation	±0.8 ns
Between TPA and TPB cable inputs, S200 operation	±0.55 ns
Between TPA and TPB cable inputs, S400 operation	±0.5 ns

10/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

11/ For a node that does not source power; see Section 4.2.2.2 in IEEE 1394a-2000.

12/ RESETz is for device type 01 and 02; RESET is for device type 03

13/ Time after valid clock received at PHY XI input terminal.

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1.5 Thermal characteristics.

Thermal metric 14/	Case outline X	Units
Junction to ambient thermal resistance, $R_{\theta JA}$	28.7	°C/W
Junction to case (top) thermal resistance, $R_{\theta Jc top}$	22.1	
Junction to board thermal resistance, $R_{\theta JB}$	13.8	
Junction to top characterization parameter, Ψ_{JT}	0.3	
Junction to board characterization parameter, Ψ_{JB}	13.7	
Junction to case (bottom) thermal resistance, $R_{\theta Jc bot}$	2.8	

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JEP155 – Recommended ESD Target Levels For HBM/MM Qualification
- JEP157 – Recommended ESD-CDM Target Levels

Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at <https://www.jedec.org>.

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

- IEEE 1394-1995 - (1394) Standard for High-Performance Serial Bus
- IEEE 1394a-2000 - (1394) Standard for High-Performance Serial Bus Supplement
- IEEE 1394b-2002 - (1394) Standard for High-Performance Serial Bus Supplement

(Copies of these documents are available online at <https://www.ieee.org> .

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Block diagrams. The block diagrams shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{DD}	Temperature, T _A	Device type	Limits		Unit	
						Min	Max		
DEVICE									
Supply current 3.3 V _{DD33}	I _{DD}	2/	3.3 V	25°C	All		150	mA	
Power status threshold, CPS input	V _(TH) 3/	400 kΩ resistor	3.0 V and 3.6 V	-40°C to +110°C		4.7	7.5	V	
High level output voltage	V _{OH}	V _{DD33} = 3 to 3.6 V, I _{OH} = -4 mA For CTL0, CTL1, D0-D7, PCLK, S5_LKON_DS2 or S5_LKON outputs.	3.0 V and 3.6 V			0.85 x V _{DD33}		V	
Low level output voltage	V _{OL}	I _{OL} = 4 mA For CTL0, CTL1, D0-D7, PCLK, S5_LKON_DS2 or S5_LKON outputs.	3.0 V and 3.6 V				0.22 x V _{DD33}	V	
Off-state output current	I _{OZ}	V _O = V _{DD} or 0 V For CTL0, CTL1, D0-D7, S5_LKON_DS2 or S5_LKON I/Os	3.0 V and 3.6 V				±20	μA	
Pullup current, RESETz or RESET input 4/	I _{IRST}	V _I = 1.5 V or 0 V	3.0 V and 3.6 V				-90	-20	μA
Output voltage, TPBIAS	V _O	At rated I _O current.	3.0 V and 3.6 V				1.665	2.015	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{DD}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
DRIVER								
1394a differential output voltage	V _{OD}	R _L = 56Ω See figure 4.	3.0 V and 3.6 V	-40°C to +110°C	All	172	265	mV
1394b differential output voltage	V _{OD}					300	800	mV
Driver difference current	I _{DIFF}	Drivers enabled, speed signaling off For TPA+, TPA-, TPB+, TPB-.				-1.05 <u>5/</u>	1.05 <u>5/</u>	mA
Common-mode speed signaling current	I _{SP200}	S200 speed signaling enabled For TPB+, TPB-.				-4.84 <u>6/</u>	-2.53 <u>6/</u>	mA
	I _{SP400}	S400 speed signaling enabled For TPB+, TPB-.				-12.4 <u>6/</u>	-8.10 <u>6/</u>	mA
Off state differential voltage	V _{OFF}	Drivers disabled. See figure 4.					20	mV
RECEIVER								
Differential impedance	Z _{id}	Drivers disabled.	3.0 V and 3.6 V	-40°C to +110°C	All	4		kΩ
							4	pF
Common-mode impedance	Z _{ic}	Drivers disabled.				20		kΩ
							24	pF
Receiver input threshold voltage	V _{TH-R}	Drivers disabled.				-30	30	mV
Cable bias detect threshold voltage	V _{TH-CB}	Drivers disabled. For TPB+ and TPB- cable inputs				0.6	1.0	V
Positive arbitration comparator threshold voltage	V _{TH+}	Drivers disabled.				89	168	mV
Negative arbitration comparator threshold voltage	V _{TH-}	Drivers disabled.				-168	-89	mV
Speed signal threshold	V _{TH-SP200}	TPBIAS-TPA common-mode voltage, drivers disabled.				49	131	mV
	V _{TH-SP400}					314	396	mV

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{DD}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Switching Characteristics								
TP differential rise time, transmit	t _r	10% to 90% At 1394 connector.	3.0 V and 3.6 V	-40°C to +110°C	All	0.3	0.8	ns
TP differential fall time, transmit	t _f	90% to 10% At 1394 connector.				0.3	0.8	ns
Setup time, CTL0, CTL1, D1-D7, LREQ to PCLK	t _{su}	1394a-2000 50% to 50% See figure 4.				2.5		ns
Hold time, CTL0, CTL1, D1-D7, LREQ after PCLK	t _h	1394a-2000 50% to 50% See figure 4.				0		ns
Setup time, CTL0, CTL1, D1-D7, LREQ to LCLK_PMC	t _{su}	1394b 50% to 50% See figure 4.				2.5		ns
Hold time, CTL0, CTL1, D1-D7, LREQ after LCLK_PMC	t _h	1394b 50% to 50% See figure 4.				0		ns
Delay time, PCLK to CTL0, CTL1, D1-D7, PINT	t _d	1394a-2000 and 1394b 50% to 50% See figure 4.				0.5	7.0	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{DD}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
LPS Timing Parameters								
LPS low time	T _{LPSL}	When pulsed. <u>10/</u>	3.0 V and 3.6 V	-40°C to +110°C	01, 02	0.09	2.60	μs
LPS high time	T _{LPSH}	When pulsed. <u>10/</u>				0.021	2.60	μs
LPS duty cycle		When pulsed. <u>11/</u>				20%	60%	
LPS reset time	T _{LPS_RESET}	Time for PHY to recognize LPS deasserted and reset the interface.				2.60	2.68	μs
LPS disable time,	T _{LPS_DISABLE}	Time for PHY to recognize LPS deasserted and disable the interface.				26.03	26.11	μs
Restore time	T _{RESTORE}	Time to permit optional isolation circuits to restore during an interface reset.				15	23 <u>11/</u>	μs
PCLK activation time	T _{CLK_ACTIVATE}	Time for PCLK to be activated from reassertion of LPS. PHY not in low-power state.					60	ns
		Time for PCLK to be activated from reassertion of LPS. PHY in low-power state.	5.3	7.3	ms			

See footnotes on next sheet.

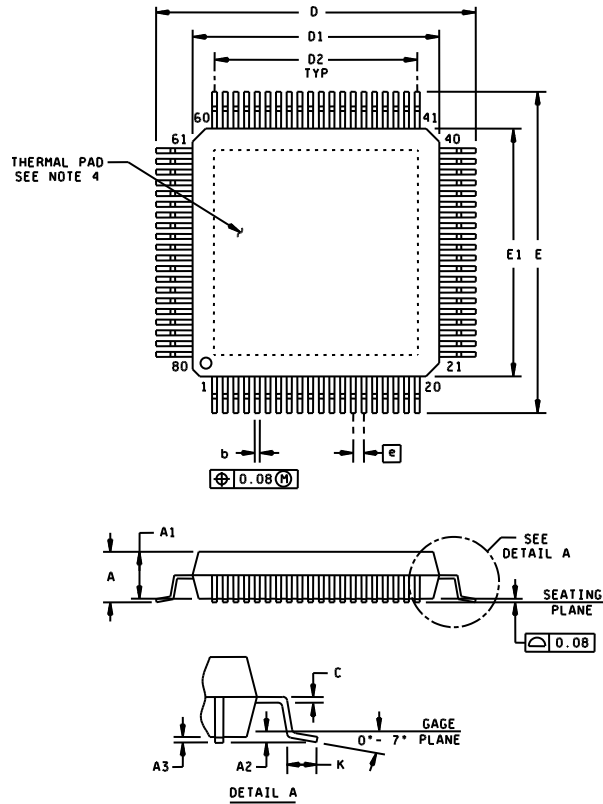
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TABLE I. Electrical performance characteristics - Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Repeat Max Packet (1 port receiving maximum size isochronous packet – 4096 bytes, sent on every isochronous interval, data value of 0xCCCCCCCCh for device type 01, or 0x00FF00FFh for device type 02; 2 ports repeating; all ports with S400 beta-mode connection), $V_{DD3.3} = 3.3\text{ V}$, internal regulator, $T_A = 25^\circ\text{C}$.
- 3/ Measured at cable power side of resistor.
- 4/ RESETz is for device type 01 and 02; $\overline{\text{RESET}}$ is for device type 03 and type 04.
- 5/ Limits defined as algebraic sum of TPA+ and TPA- driver currents. Limits also apply to TPB+ and TPB- algebraic sum of driver currents.
- 6/ Limits defined as absolute limit of each of TPB+ and TPB- driver currents.
- 7/ Board mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land with 2 oz. copper.
- 8/ Board mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land with 2 oz. copper.
- 9/ Board mounted, no air flow, high conductivity JEDEC test board with 1 oz. copper.
- 10/ The specified T_{LPSL} and T_{LPSH} times are worst-case values appropriate for operation with the TSB41BA3. These values are broader than those specified for the same parameters in the 1394a-2000 Supplement (i.e., an implementation of LPS that meets the requirements of 1394a-2000 operates correctly with the TSB41BA3).
- 11/ A pulsed LPS signal must have a duty cycle (ratio of T_{LPSH} to cycle period) in the specified range to ensure proper operation when using an isolation barrier on the LPS signal.
- 12/ The maximum value for $T_{RESTORE}$ does not apply when the PHY-LLC interface is disabled, in which case an indefinite time may elapse before LPS is reasserted. Otherwise, in order to reset but not disable the interface it is necessary that the LLC ensure that LPS is deasserted for less than $T_{PLS_DISABLE}$.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		0.047		1.20	D1	0.465	0.480	11.80	12.20
A1	0.037	0.41	0.95	1.05	D2	0.374 TYP		9.50 TYP	
A2	0.010 TYP		0.25 TYP		E	0.543	0.559	13.80	14.20
A3	0.002	0.006	E1	0.465	0.480	11.80	12.20		
b	0.007	0.011	0.17	0.27	e	0.020 TYP		0.50 TYP	
C	0.005 NOM		0.13 NOM		K	0.018	0.030	0.45	0.75
D	0.543	0.559	13.80	14.20					

NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MS-026.
3. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
4. Body dimensions include mold flash or protrusions.

FIGURE 1. Case outline.

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Device type 01

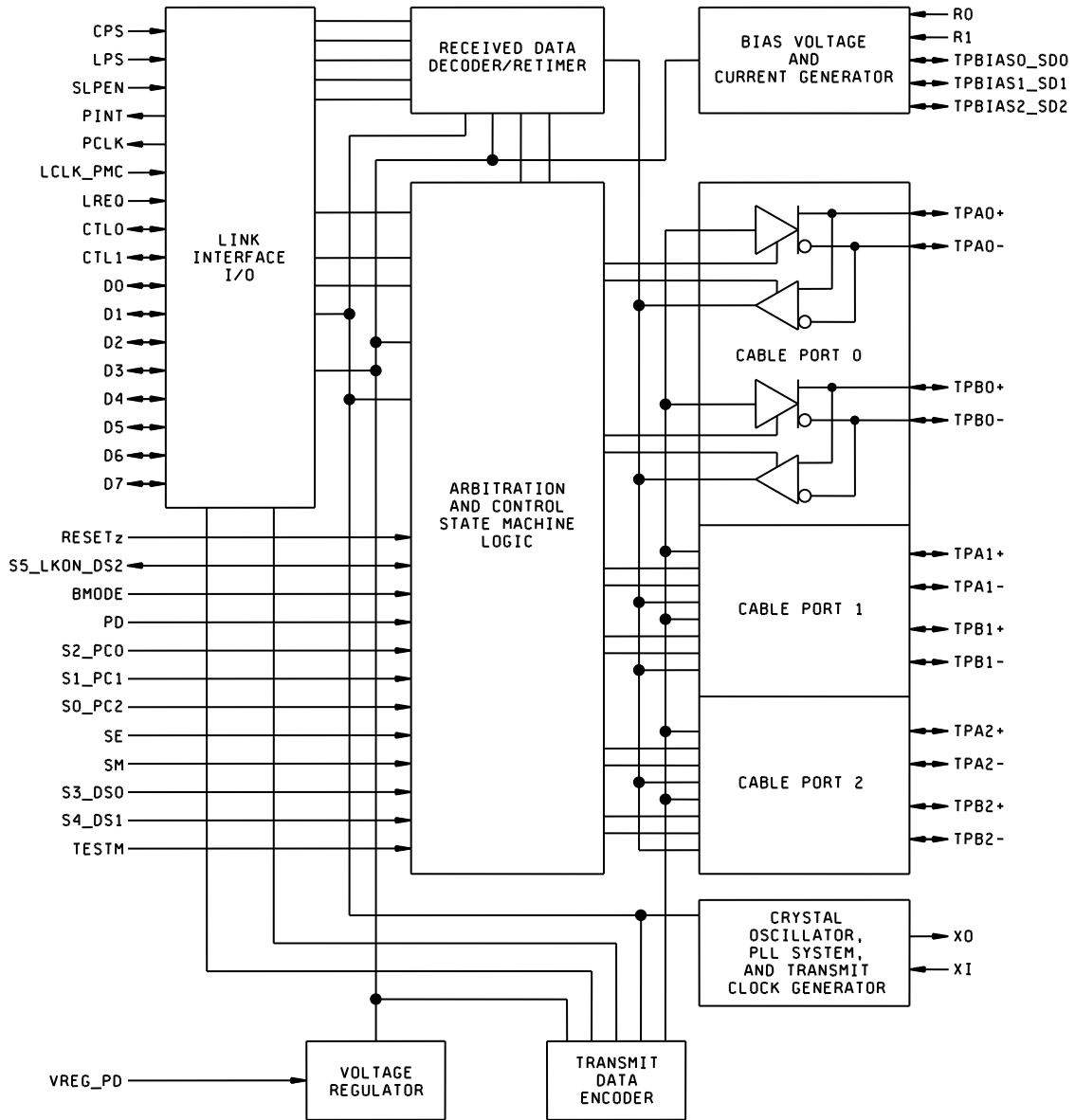
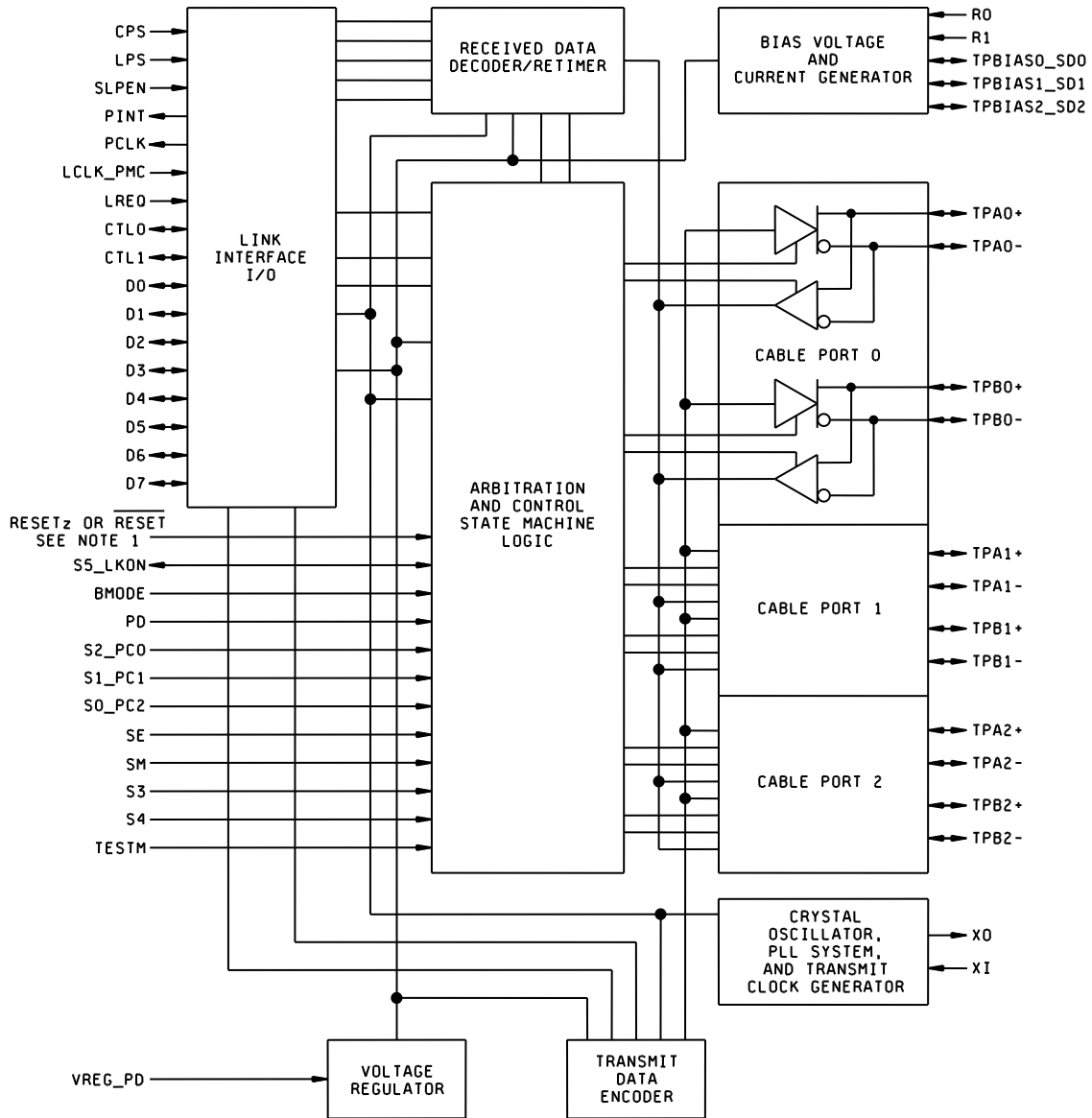


FIGURE 2. Block diagrams.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03670</p>
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Device type 02, 03



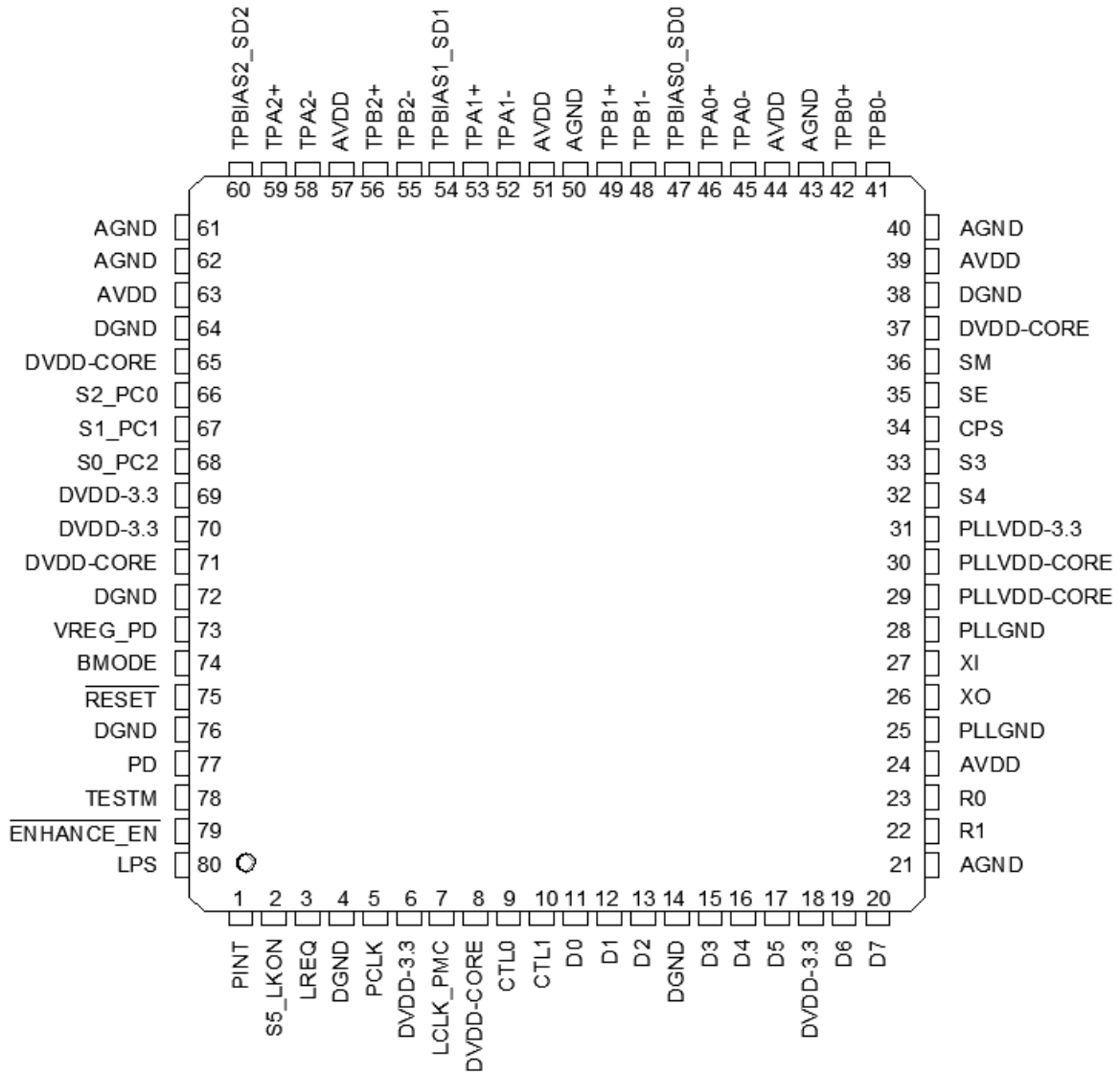
Note:

1. RESET_z is for device type 02 and $\overline{\text{RESET}}$ is for device type 03.

FIGURE 2. Block diagrams - Continued.

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Case X (Device type 01, 02, 03 and 04)

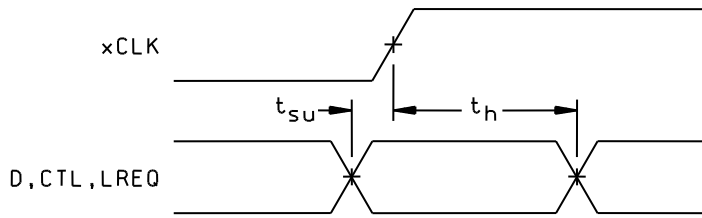


Notes:

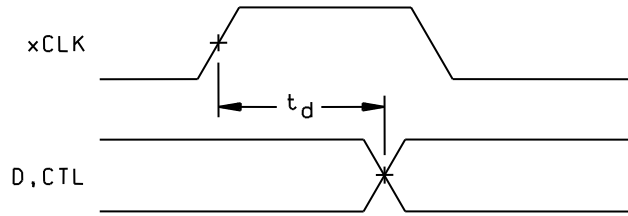
- 1/ Pin 2: S5_LKON_DS2 is for device type 01 and S5_LKON is for device type 02, 03 and 04.
- 2/ Pin 75: RESETz is for device type 02 and RESET is for device type 03 and 04.

FIGURE 3. Terminal connections.

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D_x,CTL_x,LREQ INPUT SETUP AND HOLD TIME WAVEFORMS



D_x AND CTL_x OUTPUT DELAY RELATIVE TO xCLK WAVEFORMS

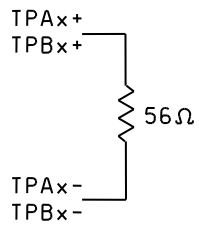


FIGURE 4. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/> .

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03670-01XE	<u>2/</u>	TSB41BA3TPFPEP	TSB41BA3TEP
V62/03670-02XE	01295	TSB41BA3ATPFPEP	TSB41BA3ATEP
V62/03670-03XE	01295	TSB41BA3BTPFPEP	TSB41B3BTEP
V62/03670-04XE	01295	TSB41BA3FTPFPEP	TSB41BA3F-EP

- f
- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
 - 2/ No longer available from an approved source of supply.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest lane
P.O. Box 660199
Dallas, TX 75243

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