

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - CFS	08-03-12	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-12-22	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236  
HAS CHANGED NAMES TO:  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

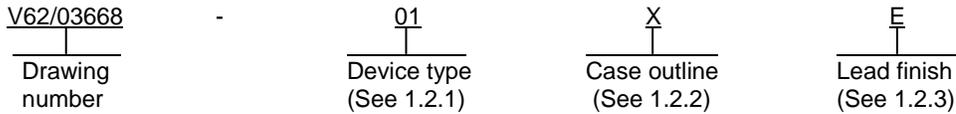
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REV STATUS OF PAGES	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
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PMIC N/A	PREPARED BY Charles F. Saffle	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing  YY-MM-DD  03-11-03	CHECKED BY Charles F. Saffle	TITLE MICROCIRCUIT, DIGITAL, CMOS, EMBEDDED TEST-BUS CONTROLLER, IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. <b>V62/03668</b>
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance embedded test-bus controller, IEEE Std 1149.1 (JTAG) TAP masters with 8-bit generic host interfaces microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVT8980A-EP	Embedded test-bus controller, IEEE Std 1149.1 (JTAG) TAP masters with 8-bit generic host interfaces

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	24	JEDEC MS-013	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V to +4.6 V
Input voltage range ( $V_I$ ) .....	-0.5 V to 7.0 V 2/
Voltage range applied to any output in the high or power-off state ( $V_O$ ): 2/	
D, RDY .....	-0.5 V to $V_{CC} + 0.5$ V
TCK, TDO, TMS, $\overline{TRST}$ .....	-0.5 V to 7.0 V
Current into any output in the low state ( $I_O$ ):	
D, RDY .....	12 mA
TCK, TDO, TMS, $\overline{TRST}$ .....	128 mA
Current into any output in the high state ( $I_O$ ): 3/	
D, RDY .....	16 mA
TCK, TDO, TMS, $\overline{TRST}$ .....	64 mA
Input clamp current ( $I_{IK}$ ) ( $V_I < 0$ ) .....	-50 mA
Output clamp current ( $I_{OK}$ ) ( $V_O < 0$ ) .....	-50 mA
Output clamp current ( $I_{OK}$ ) ( $V_O > V_{CC}$ ): D, RDY .....	50 mA
Package thermal impedance ( $\theta_{JA}$ ) .....	81°C/W 4/
Storage temperature range ( $T_{STG}$ ) .....	-65°C to +150°C

1.4 Recommended operating conditions. 5/ 6/

Supply voltage range ( $V_{CC}$ ) .....	+2.7 V to +3.6 V
Minimum high level input voltage ( $V_{IH}$ ) .....	+2.0 V
Maximum low level input voltage ( $V_{IL}$ ) .....	+0.8 V
Input voltage range ( $V_I$ ) .....	0.0 V to +5.5 V
Maximum high level output current ( $I_{OH}$ ):	
D, RDY .....	-8 mA
TCK, TDO, TMS, $\overline{TRST}$ .....	-32 mA
Maximum low level output current ( $I_{OL}$ ):	
D, RDY .....	6 mA
TCK, TDO, TMS, $\overline{TRST}$ .....	64 mA
Maximum input transition rise or fall rate ( $\Delta t/\Delta v$ ) .....	10 ns/V
Minimum power-up ramp rate ( $\Delta t/\Delta V_{CC}$ ) .....	200 $\mu$ s/V
Operating free-air temperature range ( $T_A$ ) .....	-40°C to +85°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ This current flows only when the output is in the high state and  $V_O > V_{CC}$ .

4/ The package thermal impedance is calculated in accordance with JESD 51.

5/ Unused control inputs (A, CLKIN, R/W) must be held high or low to prevent them from floating.

6/ use of this product beyond the manufacturer design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE 1149.1-1990 - (JTAG) Test Access Port (TAP) and Boundary-Scan Architecture

(Copies of these documents are available online at <http://www.ieee.org> or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855–1331).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Block diagram. The block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified		V <sub>CC</sub>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
							Min	Max	
Input clamp voltage	V <sub>IK</sub>	I <sub>I</sub> = -18 mA		2.7 V	-40°C to +85°C	01		-1.2	V
High level output voltage	V <sub>OH</sub>	D, RDY	I <sub>OH</sub> = -100 μA	2.7 V and 3.6 V	-40°C to +85°C	01	V <sub>CC</sub> - 0.2		V
			I <sub>OH</sub> = -4 mA	2.7 V			2.3		
			I <sub>OH</sub> = -4 mA	3.0 V			2.6		
			I <sub>OH</sub> = -8 mA	3.0 V			2.4		
		TCK, <u>TD0</u> , TMS, TRST	I <sub>OH</sub> = -100 μA	2.7 V and 3.6 V			V <sub>CC</sub> - 0.2		
			I <sub>OH</sub> = -8 mA	2.7 V			2.4		
			I <sub>OH</sub> = -32 mA	3.0 V			2.0		
Low level output voltage	V <sub>OL</sub>	D, RDY	I <sub>OL</sub> = 100 μA	2.7 V and 3.6 V	-40°C to +85°C	01		0.2	V
			I <sub>OL</sub> = 4 mA	2.7 V				0.55	
			I <sub>OL</sub> = 6 mA	2.7 V				0.8	
			I <sub>OL</sub> = 4 mA	3.0 V				0.55	
			I <sub>OL</sub> = 6 mA	3.0 V				0.8	
		TCK, <u>TD0</u> , TMS, TRST	I <sub>OL</sub> = 100 μA	2.7 V and 3.6 V				0.2	
			I <sub>OL</sub> = 24 mA	2.7 V				0.5	
			I <sub>OL</sub> = 16 mA	3.0 V				0.4	
			I <sub>OL</sub> = 32 mA	3.0 V				0.5	
			I <sub>OL</sub> = 64 mA	3.0 V				0.55	
Input current	I <sub>I</sub>	A, <u>CLKIN</u> , RST, R/W, STRB, TDI, TOE	V <sub>I</sub> = 5.5 V	0.0 V and 3.6 V	-40°C to +85°C	01		10.0	μA
			A, <u>CLKIN</u> , R/W, D, RDY	V <sub>I</sub> = V <sub>CC</sub> or GND			3.6 V		
		RST, STRB, TDI, TOE	V <sub>I</sub> = V <sub>CC</sub>	3.6 V				1.0	
			V <sub>I</sub> = 0.0 V	3.6 V				-100	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified		V <sub>CC</sub>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
							Min	Max	
Input/output power-off leakage current	I <sub>off</sub>	TCK, <u>TDO</u> , TMS, TRST	V <sub>I</sub> or V <sub>O</sub> = 0.0 V to 4.5 V	0.0 V	-40°C to +85°C	01		±100	μA
Three-state output leakage current high	I <sub>OZH</sub>	D, TCK, <u>TDO</u> , TMS, TRST	V <sub>O</sub> = 3.0 V	3.6 V	-40°C to +85°C	01		5.0	μA
Three-state output leakage current low	I <sub>OZL</sub>	D, TCK, <u>TDO</u> , TMS, TRST	V <sub>O</sub> = 0.5 V	3.6 V	-40°C to +85°C	01		-5.0	μA
Three-state output leakage current power-up	I <sub>OZPU</sub>	TCK, <u>TDO</u> , TMS, TRST	V <sub>O</sub> = 0.5 V to 3.0 V TOE = 0	0.0 V to 1.5 V	-40°C to +85°C	01		±100	μA
Three-state output leakage current power-down	I <sub>OZPD</sub>	TCK, <u>TDO</u> , TMS, TRST	V <sub>O</sub> = 0.5 V to 3.0 V TOE = 0	1.5 V to 0.0 V	-40°C to +85°C	01		±100	μA
Quiescent supply current	I <sub>CC</sub>	Outputs high	I <sub>O</sub> = 0.0 A V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	-40°C to +85°C	01		0.5	mA
		Outputs low						7.0	
		Outputs disabled						0.5	
Quiescent supply current delta, TTL input levels	ΔI <sub>CC</sub> <sub>2/</sub>	One input at V <sub>CC</sub> - 0.6 V. Other inputs at V <sub>CC</sub> or GND.		3.0 V and 3.6 V	-40°C to +85°C	01		0.2	mA
Input capacitance	C <sub>I</sub>	V <sub>I</sub> = 3.0 V or 0.0 V		3.3 V	+25°C	01	4.0 TYP		pF
Input/output capacitance	C <sub>IO</sub>	V <sub>O</sub> = 3.0 V or 0.0 V		3.3 V	+25°C	01	5.0 TYP		pF
Output capacitance	C <sub>O</sub>	V <sub>O</sub> = 3.0 V or 0.0 V		3.3 V	+25°C	01	7.0 TYP		pF
Clock frequency, CLKIN	f <sub>clock</sub>	TCK = CLKIN (CDIV = 0)		2.7 V	-40°C to +85°C	01	0	16	MHz
				3.0 V and 3.6 V			0	20	
		TCK = CLKIN/2 (CDIV = 1)	2.7 V	0			32		
			3.0 V and 3.6 V	0			40		
		TCK ≤ CLKIN/4 (CDIV ≥ 2)	2.7 V	0			64		
			3.0 V and 3.6 V	0			70		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified		V <sub>CC</sub>	Temperature, T <sub>A</sub>	Device type	Limits		Unit					
							Min	Max						
Pulse duration	t <sub>w</sub>	CLKIN high or low	TCK = CLKIN (CDIV = 0)	2.7 V	-40°C to +85°C	01	31.0		ns					
				3.0 V and 3.6 V			25.0							
			TCK = CLKIN/2 (CDIV = 1)	2.7 V			15.6							
				3.0 V and 3.6 V			12.5							
			TCK ≤ CLKIN/4 (CDIV ≥ 2)	2.7 V			7.8							
				3.0 V and 3.6 V			7.1							
		$\overline{\text{RST}}$ low	2.7 V	10.0										
			3.0 V and 3.6 V	10.0										
		$\overline{\text{STRB}}$ low	2.7 V	8.0										
			3.0 V and 3.6 V	8.0										
		Setup time	t <sub>su</sub>	A before $\overline{\text{STRB}}\downarrow$			Read or write (R/W high or low)	2.7 V		-40°C to +85°C	01	10.0		ns
								3.0 V and 3.6 V				10.0		
D before $\overline{\text{STRB}}\uparrow$	Write (R/W low)			2.7 V	5.0									
				3.0 V and 3.6 V	5.0									
$\overline{\text{R/W}}$ before $\overline{\text{STRB}}\downarrow$				2.7 V	5.0									
				3.0 V and 3.6 V	5.0									
TDI before CLKIN $\uparrow$				2.7 V	5.0									
				3.0 V and 3.6 V	5.0									

See footnotes at end of table

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/03668</b>
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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified		V <sub>CC</sub>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
							Min	Max	
Hold time	t <sub>h</sub>	A after STRB↑	Read or write (R/W high or low)	2.7 V	-40°C to +85°C	01	5.0		ns
				3.0 V and 3.6 V			5.0		
		D after STRB↑	Write (R/W low)	2.7 V			15.0		
				3.0 V and 3.6 V			15.0		
		R/W after STRB↑		2.7 V			6.0		
				3.0 V and 3.6 V			6.0		
		TDI after CLKIN↑		2.7 V			10.0		
				3.0 V and 3.6 V			10.0		
Propagation delay time, CLKIN to TCK	t <sub>PLH</sub> , t <sub>PHL</sub>	See figure 4.		2.7 V	-40°C to +85°C	01		20.0	ns
				3.0 V and 3.6 V			6.0	17.0	
Propagation delay time, CLKIN to TDO, TMS	t <sub>PLH</sub> , t <sub>PHL</sub>			2.7 V	-40°C to +85°C	01		35.0	ns
				3.0 V and 3.6 V			8.0	30.0	
Propagation delay time, RST↓ to D	t <sub>PLH</sub> , t <sub>PHL</sub>			2.7 V	-40°C to +85°C	01		35.0	ns
				3.0 V and 3.6 V			3.0	30.0	
Propagation delay time, RST↓ to RDY	t <sub>PLH</sub> , t <sub>PHL</sub>			2.7 V	-40°C to +85°C	01		35.0	ns
				3.0 V and 3.6 V			3.0	30.0	
Propagation delay time, RST↓ to TDO, TMS, TRST, TCK	t <sub>PLH</sub> , t <sub>PHL</sub>			2.7 V	-40°C to +85°C	01		30.0	ns
				3.0 V and 3.6 V			5.0	25.0	

See footnotes at end of table.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/03668</b>
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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	V <sub>CC</sub>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
						Min	Max	
Propagation delay time, STRB $\uparrow$ to RDY, STRB $\downarrow$ to RDY	t <sub>PLH</sub> , t <sub>PHL</sub>	See figure 4.	2.7 V	-40°C to +85°C	01		22.0	ns
			3.0 V and 3.6 V			3.0	18.0	
Propagation delay time, STRB $\uparrow$ to TCK, TDO, TMS, TRST (discrete mode)	t <sub>PLH</sub> , t <sub>PHL</sub>		2.7 V	-40°C to +85°C	01		28.0	ns
			3.0 V and 3.6 V			3.0	22.0	
Propagation delay time, STRB $\uparrow$ to TCK, TDO, TMS, TRST (other modes)	t <sub>PLH</sub> , t <sub>PHL</sub>		2.7 V	-40°C to +85°C	01		40.0	ns
			3.0 V and 3.6 V			6.0	35.0	
Enable time, STRB $\downarrow$ to D	t <sub>PZH</sub> , t <sub>PZL</sub>		2.7 V	-40°C to +85°C	01		18.0	ns
			3.0 V and 3.6 V			3.0	15.0	
Enable time, STRB $\uparrow$ to TCK, TDO, TMS, TRST	t <sub>PZH</sub> , t <sub>PZL</sub>		2.7 V	-40°C to +85°C	01		30.0	ns
			3.0 V and 3.6 V			5.0	25.0	
Enable time, TOE $\downarrow$ to TCK, TDO, TMS, TRST	t <sub>PZH</sub> , t <sub>PZL</sub>	2.7 V	-40°C to +85°C	01		15.0	ns	
		3.0 V and 3.6 V			2.0	12.0		
Disable time, STRB $\uparrow$ to D	t <sub>PHZ</sub> , t <sub>PLZ</sub>	2.7 V	-40°C to +85°C	01		18.0	ns	
		3.0 V and 3.6 V			3.0	15.0		
Disable time, STRB $\uparrow$ to TCK, TDO, TMS, TRST	t <sub>PHZ</sub> , t <sub>PLZ</sub>	2.7 V	-40°C to +85°C	01		30.0	ns	
		3.0 V and 3.6 V			5.0	25.0		
Disable time, TOE $\uparrow$ to TCK, TDO, TMS, TRST	t <sub>PHZ</sub> , t <sub>PLZ</sub>	2.7 V	-40°C to +85°C	01		15.0	ns	
		3.0 V and 3.6 V			2.0	12.0		

See footnotes on next sheet.

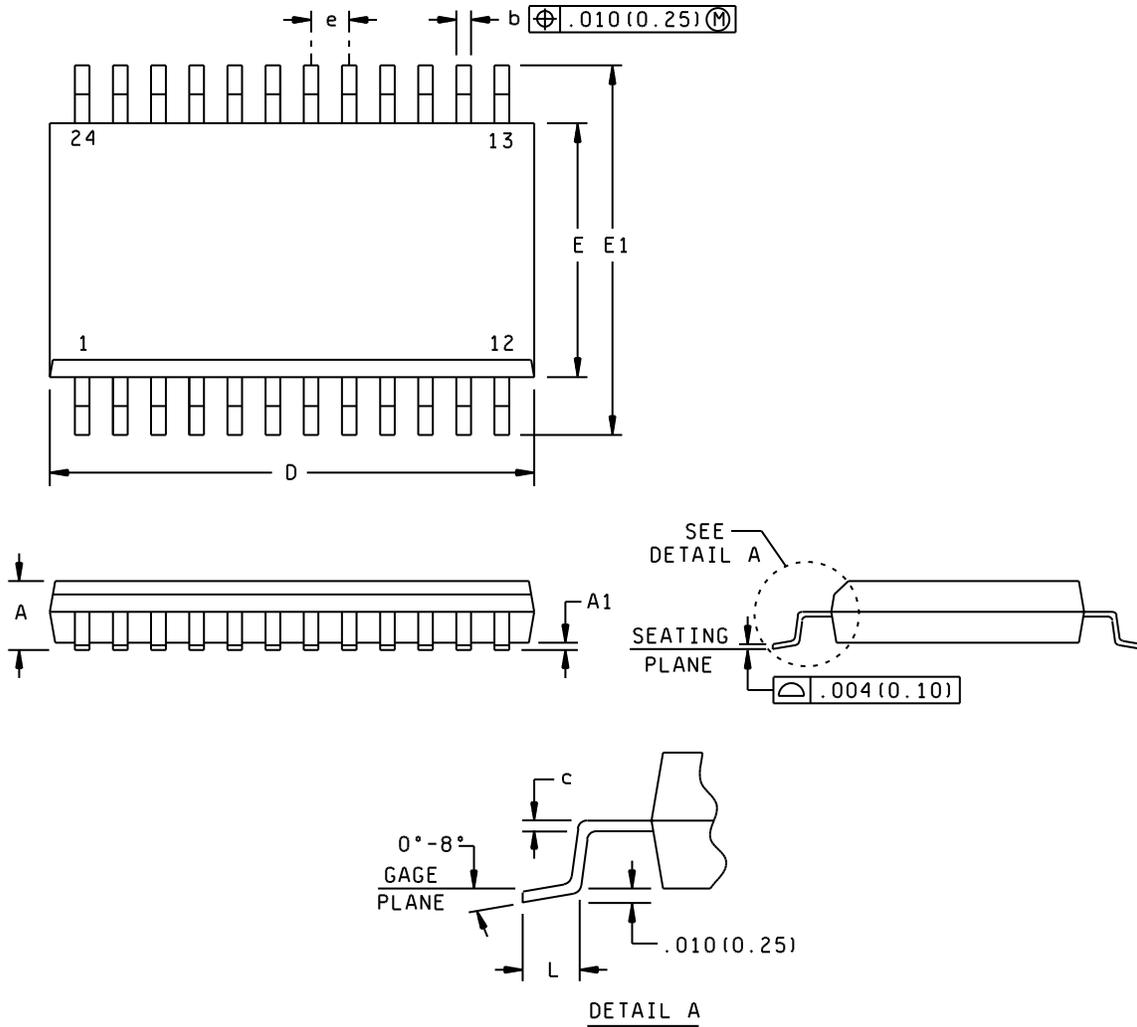
<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	SIZE <b>A</b>	CODE IDENT NO. <b>16236</b>	DWG NO. <b>V62/03668</b>
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TABLE I. Electrical performance characteristics - Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/03668</b></p>
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Case X



NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).
3. Falls within JEDEC MS-013.
4. All linear dimensions are shown in inches (millimeters). Metric equivalents are given for general information only.

FIGURE 1. Case outline.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/03668</b></p>
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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.104		2.65
A1	0.004	0.012	0.10	0.30
b	0.014	0.020	0.35	0.51
c	0.010 NOM		0.25 NOM	
D	0.600	0.610	15.24	15.49
E	0.291	0.299	7.39	7.59
E1	0.400	0.419	10.15	10.65
e	0.050 NOM		1.27 NOM	
L	0.016	0.050	0.40	1.27

FIGURE 1. Case outline - Continued.

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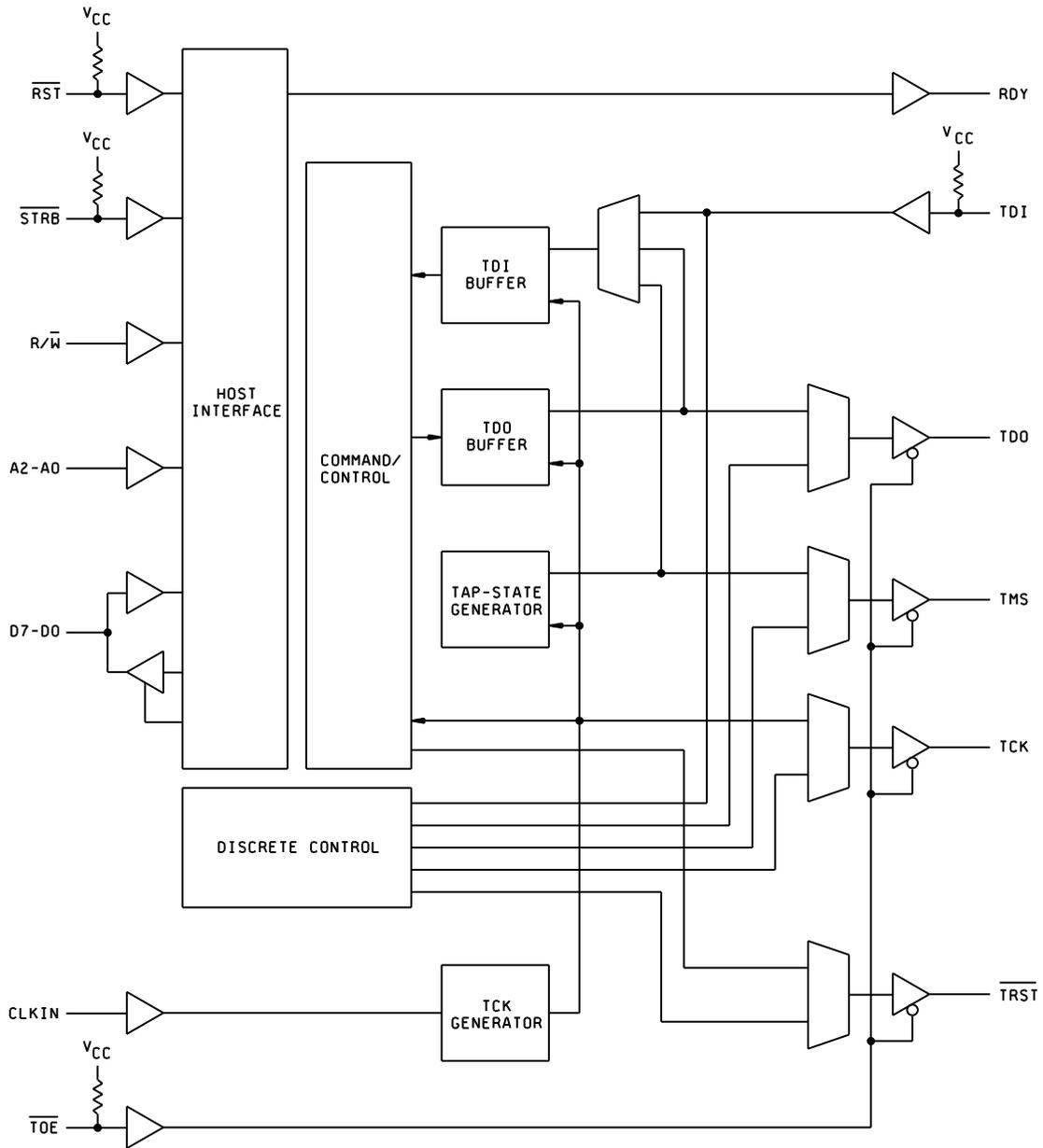


FIGURE 2. Block diagram.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/03668</b>
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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	$\overline{\text{STRB}}$
2	$\overline{\text{R/W}}$
3	D0
4	D1
5	D2
6	D3
7	GND
8	D4
9	D5
10	D6
11	D7
12	CLKIN
13	$\overline{\text{TOE}}$
14	$\overline{\text{RST}}$
15	TDI
16	$\overline{\text{TRST}}$
17	TMS
18	TCK
19	V <sub>CC</sub>
20	TDO
21	RDY
22	A2
23	A1
24	A0

FIGURE 3. Terminal connections.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/03668</b>
		REV B	PAGE 14

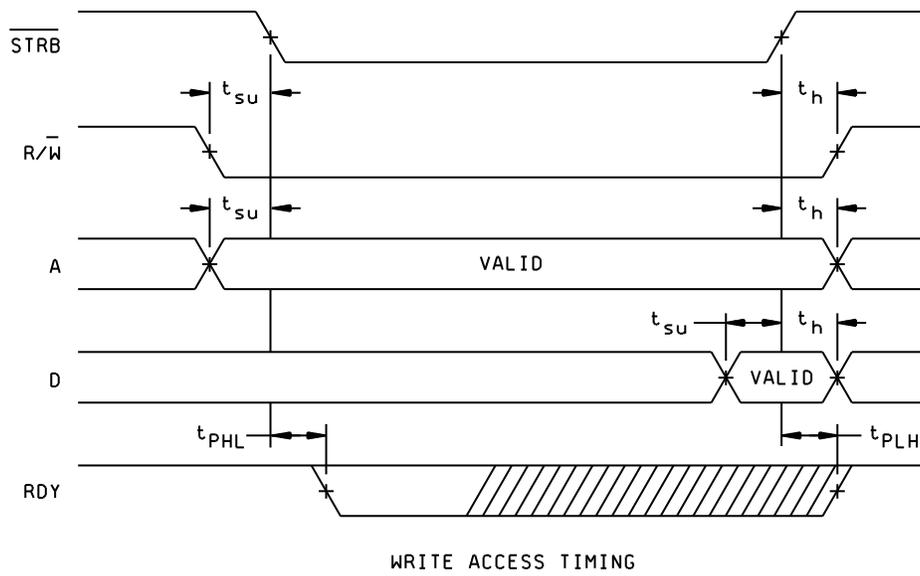
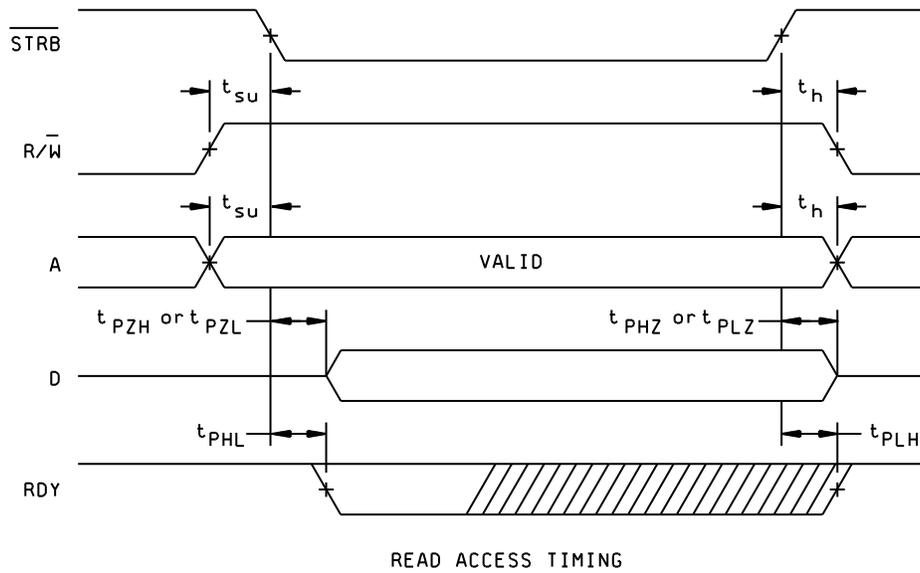
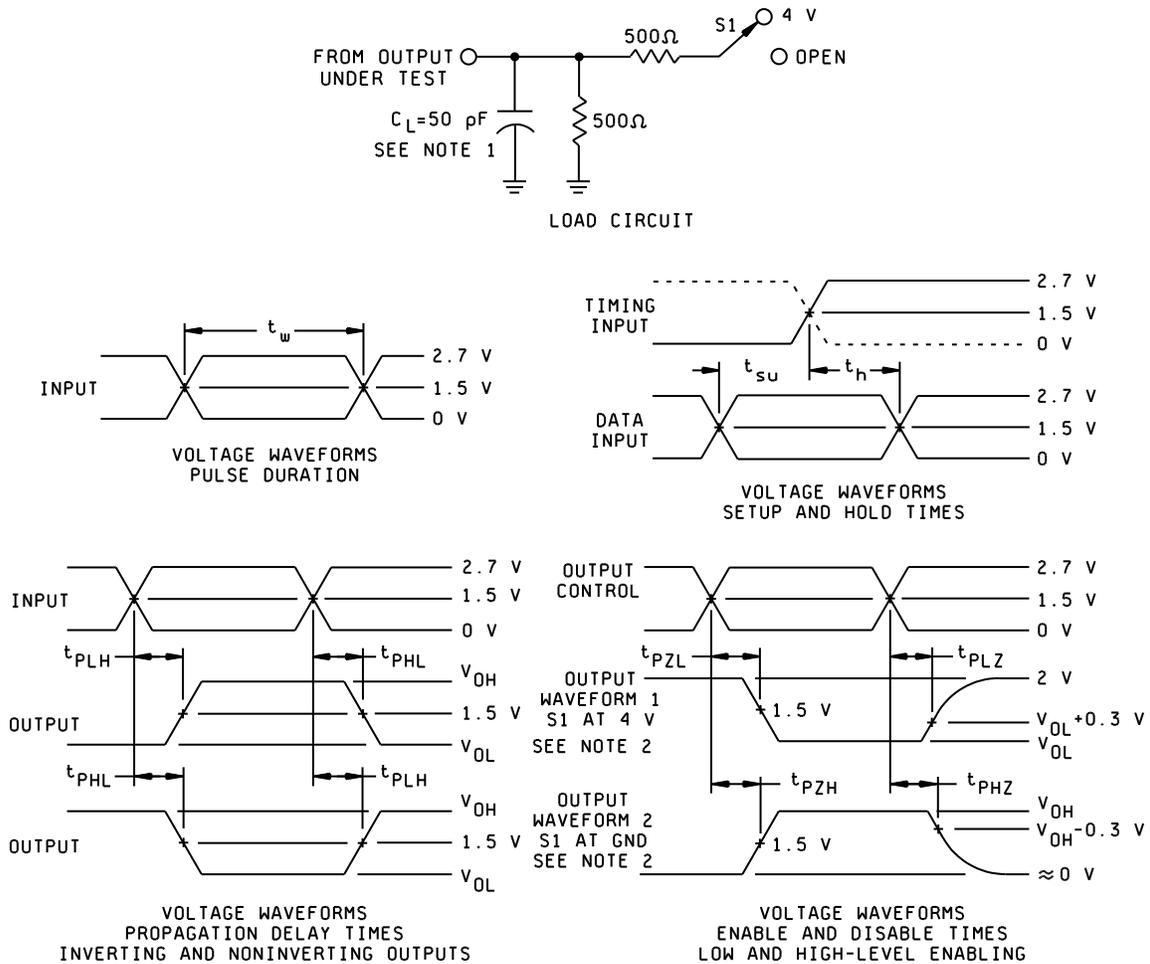


FIGURE 4. Timing waveforms.

<p style="text-align: center;"><b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b></p>	<p style="text-align: center;">SIZE <b>A</b></p>	<p style="text-align: center;">CODE IDENT NO. <b>16236</b></p>	<p style="text-align: center;">DWG NO. <b>V62/03668</b></p>
		<p style="text-align: center;">REV    <b>B</b></p>	<p style="text-align: center;">PAGE    <b>15</b></p>

D and RDY Outputs



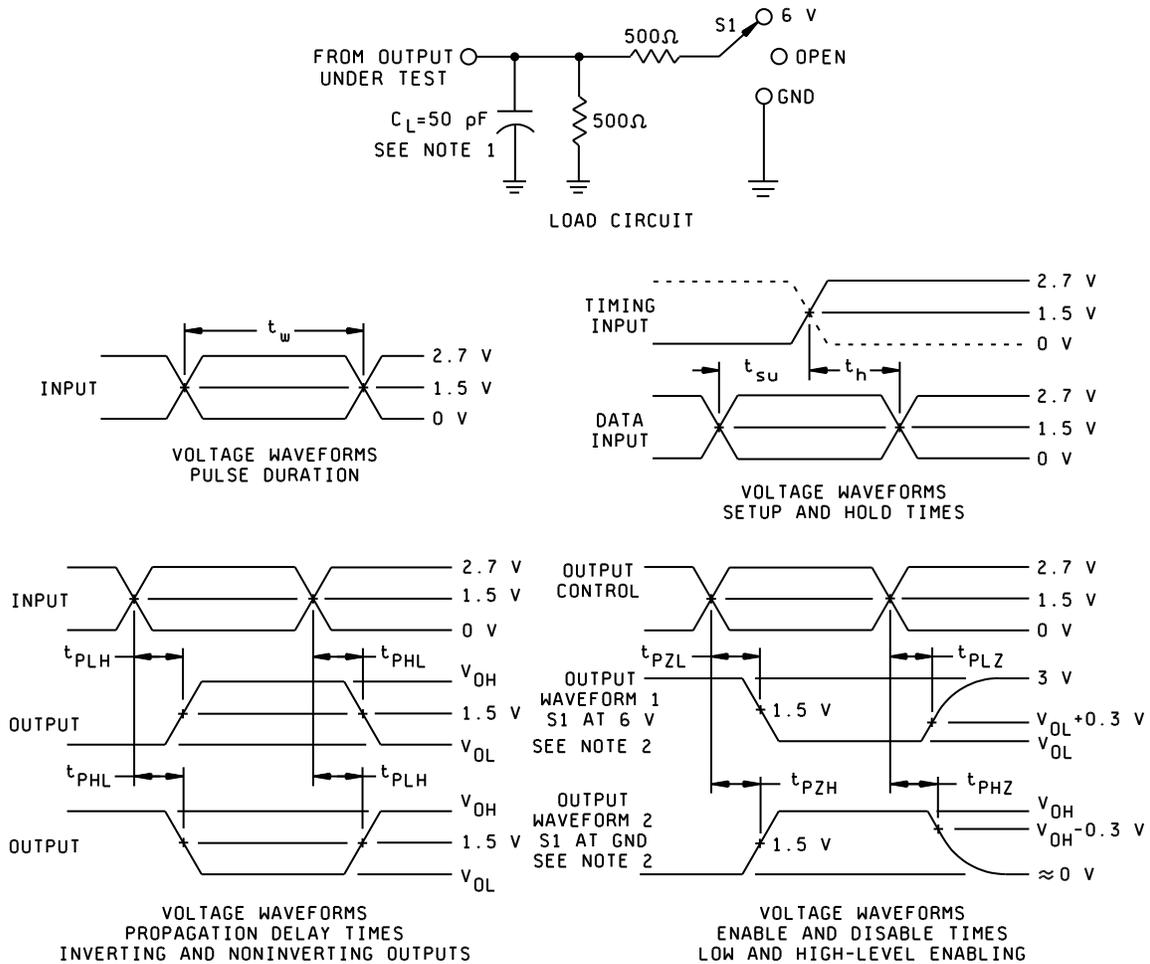
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq \text{ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - For 3-state outputs tests:
 

$t_{PLH}/t_{PHL}$	S1 = Open
$t_{PLZ}/t_{PZL}$	S1 = 4 V
$t_{PHZ}/t_{PZH}$	S1 = GND

FIGURE 4. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/03668</b>
		REV    B	PAGE    16

TCK, TDO, TMS, and TRST Outputs



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ ns.
  - The outputs are measured one at a time with one transition per measurement.
  - For 3-state outputs tests:
 

t <sub>PLH</sub> /t <sub>PHL</sub>	S1 = Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	S1 = 6.0 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	S1 = GND

FIGURE 4. Timing waveforms - Continued.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/03668</b>
		REV B	PAGE 17

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03668-01XE	01295	SN74LVT8980AIDWREP	LVT8980AEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/03668</b>
		<b>REV B</b>	<b>PAGE 18</b>