REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device case outline Y. - CFS	03-12-08	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	15-11-24	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B	B	B						
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13						

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing YY-MM-DD 03-10-07	**CHECKED BY** Charles F. Saffle	**TITLE** MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, 3.3-VOLT ABT OCTAL BUFFER/DRIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/03667**
	REV **B**	**PAGE** 1 **OF** 13

AMSC N/A

5962-V005-16

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3-volt ABT octal buffer/driver with three-state outputs microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03667	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	74LVTH244A-EP	3.3-volt ABT octal buffer/driver with three-state outputs

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-150	Plastic small-outline
Y	20	JEDEC MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to +4.6 V
Input voltage range (V_I) ..... -0.5 V to +7.0 V 2/
Voltage range applied to any output in the high-impedance or power-off state (V_O) ..... -0.5 V to + 7.0 V 2/
Voltage range applied to any output in the high state (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/
Current into any output in the low state (I_O) ..... 96 mA
Current into any output in the high state (I_O) ..... 48 mA 3/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -50 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Package thermal impedance (θ_{JA}):
Case outline X ..... 70°C/W 4/
Case outline Y ..... 83°C/W 4/
Storage temperature range (T_{STG}) ..... -65°C to +150°C 5/

1.4 Recommended operating conditions. 6/

Supply voltage range (V_{CC}) ..... 2.7 V to 3.6 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V
Maximum low level input voltage (V_{IL}) ..... 0.8 V
Input voltage range (V_I) ..... 0.0 V to 5.5 V
Maximum high level output current (I_{OH}) ..... -24 mA
Maximum low level output current (I_{OL}) ..... 32 mA
Maximum input transition rise or fall rate (outputs enabled) ($\Delta t/\Delta v$) ..... 10 ns/V
Minimum power-up ramp rate ($\Delta t/\Delta V_{CC}$) ..... 200 μs/V
Operating free-air temperature range (T_A) ..... -40°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 - Registered and Standard Outlines for Semiconductor Devices
JESD 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at http://www.jedec.org)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3/ This current flows only when the output is in the high state and $V_O > V_{CC}$.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
6/ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V_{IK}	I_I = -18 mA	2.7 V	25°C, -55°C to 125°C	01		-1.2	V
High level output voltage	V_{OH}	I_{OH} = -100 μA	2.7 V to 3.6 V	25°C, -55°C to 125°C	01	V_{CC} – 0.2		V
		I_{OH} = -8 mA	2.7 V			2.4		
		I_{OH} = -24 mA	3.0 V			2.0		
Low level output voltage	V_{OL}	I_{OL} = 100 μA	2.7 V	25°C, -55°C to 125°C	01		0.2	V
		I_{OL} = 24 mA					0.5	
		I_{OL} = 16 mA	3.0 V				0.4	
		I_{OL} = 32 mA					0.5	
Input current, Control inputs	I_I	V_I = 5.5 V	0.0 V or 3.6 V	25°C, -55°C to 125°C	01		50.0	μA
		V_I = V_{CC} or GND	3.6 V				±1.0	
Input current, Data inputs	I_I	V_I = V_{CC}	3.6 V	25°C, -55°C to 125°C	01		1.0	μA
		V_I = 0.0 V					-5.0	
Input bus hold current, Data inputs	$I_{I(hold)}$	V_I = 0.8 V	3.0 V	25°C, -55°C to 125°C	01	75.0		μA
		V_I = 2.0 V				-75.0		
Three-state output leakage current high	I_{OZH}	V_O = 3.0 V	3.6 V	25°C, -55°C to 125°C	01		5.0	μA
Three-state output leakage current low	I_{OZL}	V_O = 0.5 V	3.6 V	25°C, -55°C to 125°C	01		-5.0	μA
Three-state output leakage current power-up	I_{OZPU}	V_O = 0.5 V to 3.0 V OE = don't care	0.0 V to 1.5 V	25°C, -55°C to 125°C	01		±100	μA
Three-state output leakage current power-down	I_{OZPD}	V_O = 0.5 V to 3.0 V OE = don't care	1.5 V to 0.0 V	25°C, -55°C to 125°C	01		±100	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Quiescent supply current	I_{CC}	Outputs high $V_I = V_{CC}$ or GND $I_O = 0$ A	3.6 V	25°C, -55°C to 125°C	01		0.39	mA
		Outputs low $V_I = V_{CC}$ or GND $I_O = 0$ A					14.0	
		Outputs disabled $V_I = V_{CC}$ or GND $I_O = 0$ A					0.39	
Quiescent supply current delta, TTL input levels	ΔI_{CC} 1/	One input at V_{CC} – 0.6 V Other inputs at V_{CC} or GND	3.0 V to 3.6 V	25°C, -55°C to 125°C	01		0.2	mA
Input capacitance	C_I	V_I = 3.0 V or 0.0 V		25°C, -55°C to 125°C	01	3.0 TYP		pF
Output capacitance	C_O	V_O = 3.0 V or 0.0 V		25°C, -55°C to 125°C	01	7.0 TYP		pF
Propagation delay time, A to Y	t_{PLH}	C_L = 50 pF See figure 5	3.0 V and 3.6 V	25°C, -55°C to 125°C	01	0.5	3.8	ns
			2.7 V				4.1	
	t_{PHL}	C_L = 50 pF See figure 5	3.0 V and 3.6 V	25°C, -55°C to 125°C		0.5	3.8	
			2.7 V				3.9	
Propagation delay time, output enable, OE to Y	t_{PZH}	C_L = 50 pF See figure 5	3.0 V and 3.6 V	25°C -55°C to 125°C	01	0.8	5.0	ns
			2.7 V				6.0	
	t_{PZL}	C_L = 50 pF See figure 5	3.0 V and 3.6 V	25°C, -55°C to 125°C		0.8	5.0	
			2.7 V				5.4	

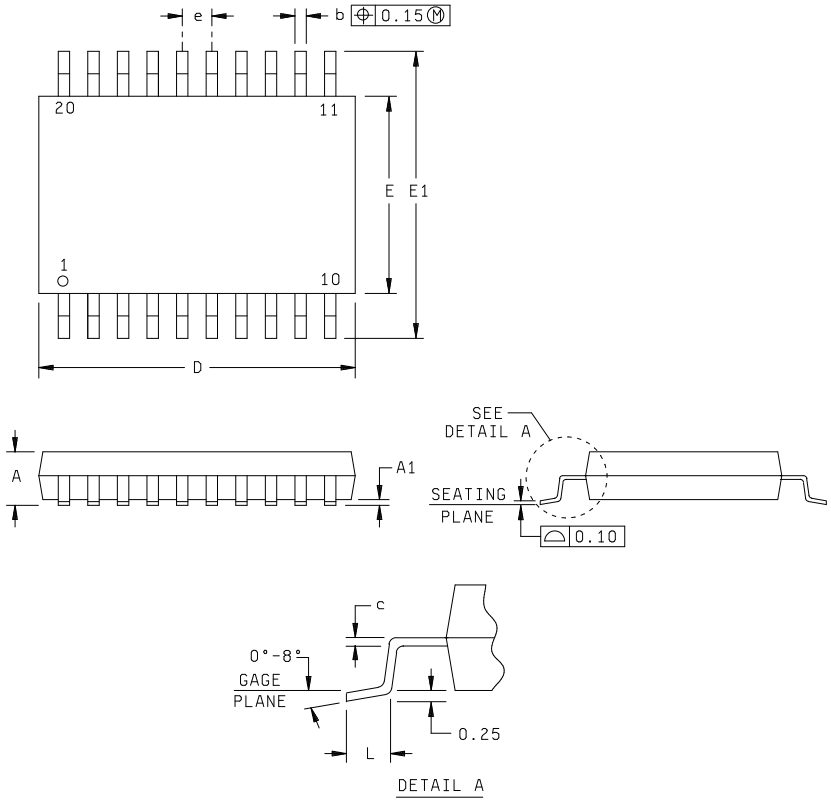
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Propagation delay time, output disable, OE to Y	t_{PHZ}	C_L = 50 pF See figure 5	3.0 V and 3.6 V	25°C -55°C to 125°C	01	1.3	5.5	ns
			2.7 V				5.8	
	t_{PLZ}	C_L = 50 pF See figure 5	3.0 V and 3.6 V	25°C, -55°C to 125°C		1.2	4.7	
			2.7 V				4.8	

1/ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Case X

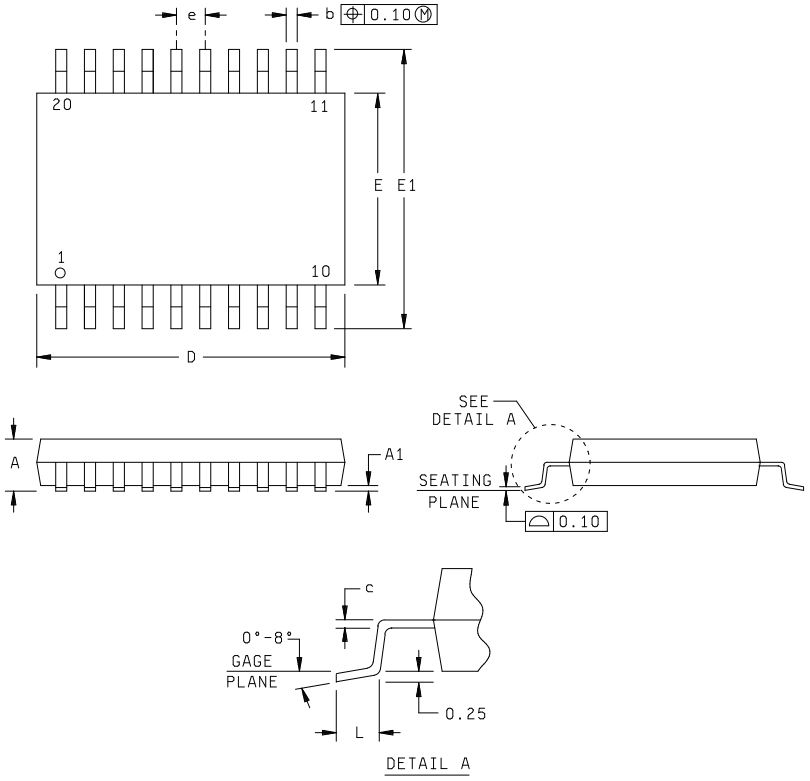


Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	2.00	---	.079	E	5.00	5.60	.197	.220
A1	0.05	---	.002	---	E1	7.40	8.20	.291	.323
b	0.22	0.38	.009	.015	e	0.65 NOM		.026 NOM	
c	0.09	0.25	.004	.010	L	0.55	0.95	.022	.037
D	6.90	7.50	.272	.295					

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm.
3. Falls within JEDEC MO-150.
4. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.

FIGURE 1. Case outlines.

Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 TYP		0.026 TYP	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	6.40	6.60	0.252	0.260					

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm.
3. Falls within JEDEC MO-153.
4. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

(each buffer)

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

X = Immaterial
Z = High impedance state

FIGURE 2. Truth table.

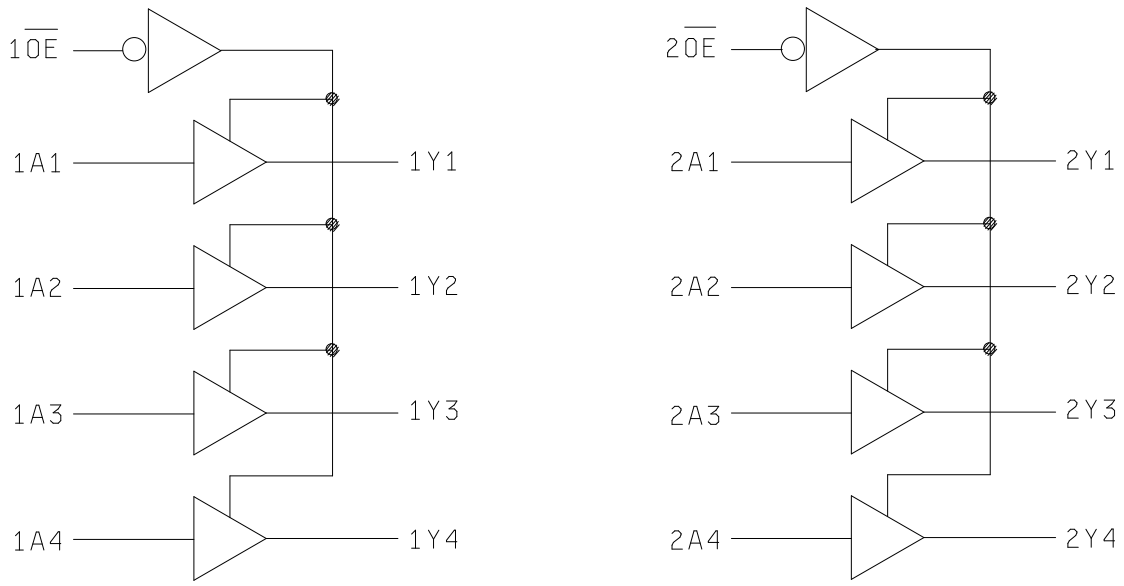
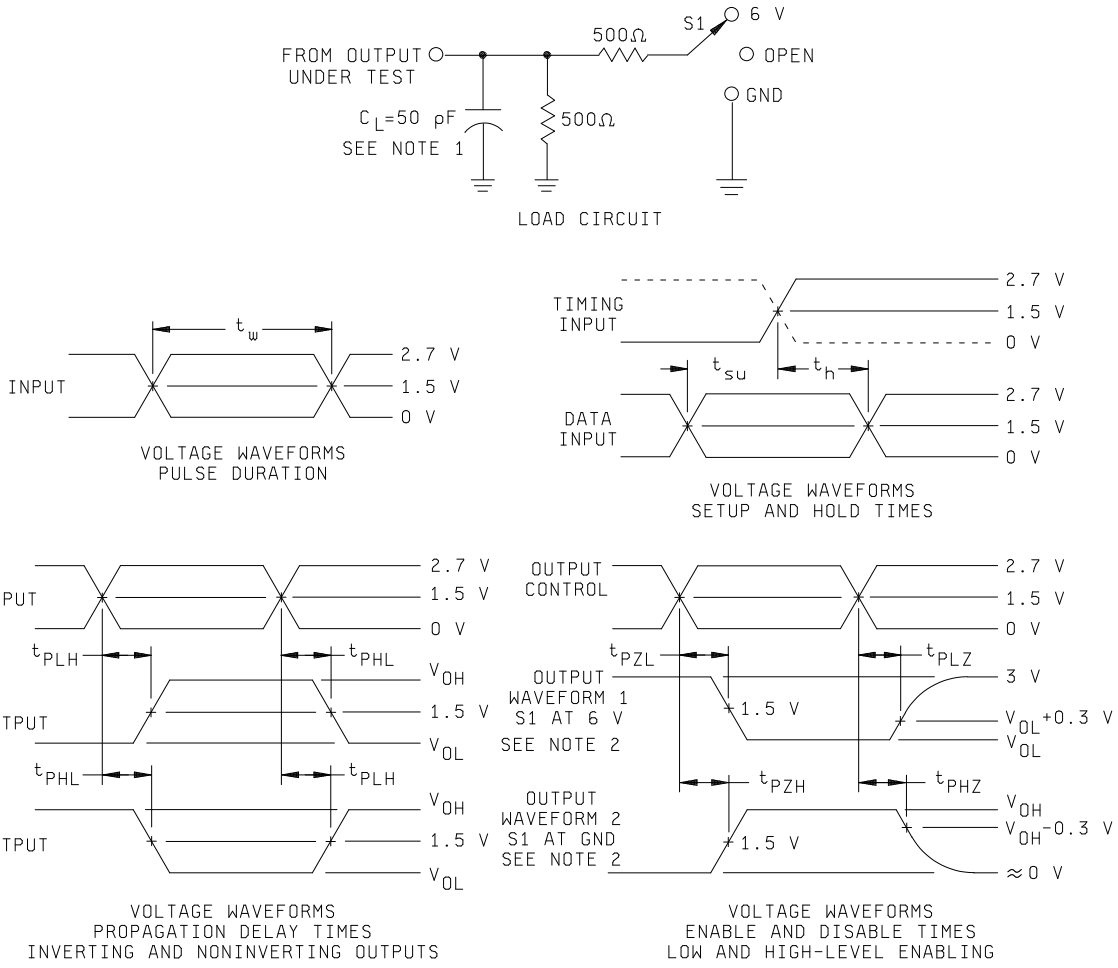


FIGURE 3. Logic diagram.

Device type	01
Case outlines	X, Y
Terminal number	Terminal symbol
1	$1\overline{OE}$
2	1A1
3	2Y4
4	1A2
5	2Y3
6	1A3
7	2Y2
8	1A4
9	2Y1
10	GND
11	2A1
12	1Y4
13	2A2
14	1Y3
15	2A3
16	1Y2
17	2A4
18	1Y1
19	$2\overline{OE}$
20	V_{CC}

FIGURE 4. Terminal connections.



Notes:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
4. The outputs are measured one at a time with one input transition per measurement.
5. For three-state outputs tests: t_{PLH}/t_{PHL} S1 = Open
   t_{PLZ}/t_{PZL} S1 = 6.0 V
   t_{PHZ}/t_{PZH} S1 = GND

FIGURE 5. Timing waveforms and test circuit.

4.0 VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6.0 NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03667-01XE	01295	SN74LVTH244AQDBREP	LH244AEP
V62/03667-01YE	01295	SN74LVTH244AQPWREP	LH244AEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493