REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add case outline Y. - CFS	04-03-08	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	12-06-04	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	19-03-12	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		C	C	C	C	C	C	C	C	C	C	C	C	C	C						
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14						

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing YY-MM-DD 03-10-07	**CHECKED BY** Charles F. Saffle	**TITLE** MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, DUAL 4-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/03665**
	REV **C**	**PAGE** 1 **OF** 14

AMSC N/A

5962-V051-19

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual 4-channel analog multiplexer/demultiplexer microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03665	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	74LV4052A-EP	Dual 4-channel analog multiplexer/demultiplexer

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153	Plastic small-outline
Y	16	JEDEC MS-012	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to +7.0 V
Input voltage range (V_I) ..... -0.5 V to +7.0 V 2/
Switch I/O voltage range (V_{IO}) ..... -0.5 V to V_{CC} + 0.5 V 2/ 3/
Input clamp current (I_{IK}) (V_I < 0) ..... -20 mA
I/O diode current (I_{IOK}) (V_{IO} < 0 or V_{IO} > V_{CC}) ..... ±50 mA
Switch through current (I_T) (V_{IO} = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Package thermal impedance (θ_{JA}): 4/
Case outline X ..... 108°C/W
Case outline Y ..... 73°C/W
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}) ..... 2.0 V to 5.5 V 6/
Minimum high level input voltage (V_{IH}), control inputs:
V_{CC} = 2.0 V ..... 1.5 V
V_{CC} = 2.3 V to 2.7 V ..... V_{CC} x 0.7
V_{CC} = 3.0 V to 3.6 V ..... V_{CC} x 0.7
V_{CC} = 4.5 V to 5.5 V ..... V_{CC} x 0.7
Maximum low level input voltage (V_{IL}), control inputs:
V_{CC} = 2.0 V ..... 0.5 V
V_{CC} = 2.3 V to 2.7 V ..... V_{CC} x 0.3
V_{CC} = 3.0 V to 3.6 V ..... V_{CC} x 0.3
V_{CC} = 4.5 V to 5.5 V ..... V_{CC} x 0.3
Control input voltage range (V_I) ..... 0.0 V to 5.5 V
Input/output voltage range (V_{IO}) ..... 0.0 V to V_{CC}
Maximum input transition rise or fall rate ($\Delta t/\Delta v$):
V_{CC} = 2.3 V to 2.7 V ..... 200 ns/V
V_{CC} = 3.0 V to 3.6 V ..... 100 ns/V
V_{CC} = 4.5 V to 5.5 V ..... 20 ns/V
Operating free-air temperature range (T_A) ..... -40°C to +105°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ This value is limited to 5.5 V maximum.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
6/ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices
JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at https://www.jedec.org.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figure 5.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Limits		Unit
					Min	Max	
On-state switch resistance	r_{on}	I_T = 2 mA V_I = V_{CC} or GND V_{INH} = V_{IL} See figure 5	2.3 V	25°C, -55°C to 125°C		225	Ω
			3.0 V	25°C, -55°C to 125°C		190	
			4.5 V	25°C, -55°C to 125°C		100	
Peak on-state resistance	$r_{on(p)}$	I_T = 2 mA V_I = V_{CC} or GND V_{INH} = V_{IL}	2.3 V	25°C, -55°C to 125°C		600	Ω
			3.0 V	25°C, -55°C to 125°C		225	
			4.5 V	25°C, -55°C to 125°C		125	
Difference in on-state resistance between switches	Δr_{on}	I_T = 2 mA V_I = V_{CC} or GND V_{INH} = V_{IL}	2.3 V	25°C, -55°C to 125°C		40	Ω
			3.0 V	25°C, -55°C to 125°C		30	
			4.5 V	25°C, -55°C to 125°C		20	
Control input current	I_I	V_I = 5.5 V or GND	0.0 V to 5.5 V	25°C, -55°C to 125°C		±1.0	μA
Off-state switch leakage current	$I_{S(off)}$	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC} V_{INH} = V_{IH} See figure 5	5.5 V	25°C, -55°C to 125°C		±1.0	μA
On-state switch leakage current	$I_{S(on)}$	V_I = V_{CC} or GND V_{INH} = V_{IL} See figure 5	5.5 V	25°C, -55°C to 125°C		±1.0	μA
Quiescent supply current	I_{CC}	V_I = V_{CC} or GND	5.5 V	25°C, -55°C to 125°C		20.0	μA
Power dissipation capacitance	C_{pd}	C_L = 50 pF f = 10 MHz	3.3 V	25°C	11.8 TYP		pF

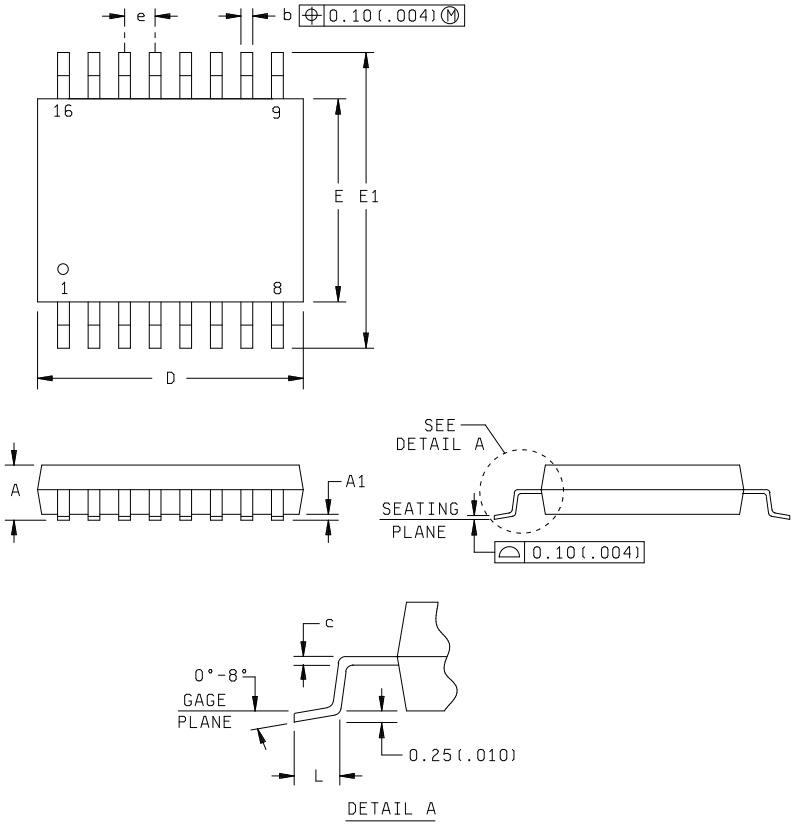
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions		V_{CC}	Temperature, T_A	Limits		Unit
						Min	Max	
Propagation delay time, COM or Y to Y or COM	t_{PLH}, t_{PHL}	C_L = 50 pF See figure 5		3.0 V and 3.6 V	25°C, -55°C to 125°C		12.0	ns
				4.5 V and 5.5 V	25°C, -55°C to 125°C		8.0	
Propagation delay time, INH to COM or Y	t_{PZH}, t_{PZL}	C_L = 50 pF See figure 5		3.0 V and 3.6 V	25°C, -55°C to 125°C		25.0	ns
				4.5 V and 5.5 V	25°C, -55°C to 125°C		18.0	
Propagation delay time, INH to COM or Y	t_{PHZ}, t_{PLZ}	C_L = 50 pF See figure 5		3.0 V and 3.6 V	25°C, -55°C to 125°C		25.0	ns
				4.5 V and 5.5 V	25°C, -55°C to 125°C		18.0	
Frequency response (switch on), COM or Y to Y or COM		C_L = 50 pF R_L = 600 Ω f_{in} = 1 MHz (sine wave) 1/ See figure 5		2.3 V	25°C	30 TYP		MHz
				3.0 V	25°C	35 TYP		
				4.5 V	25°C	50 TYP		
Crosstalk (between any switches), COM or Y to Y or COM		C_L = 50 pF R_L = 600 Ω f_{in} = 1 MHz (sine wave) 2/ See figure 5		2.3 V	25°C	-45 TYP		dB
				3.0 V	25°C	-45 TYP		
				4.5 V	25°C	-45 TYP		
Crosstalk (control input to signal output), INH to COM or Y		C_L = 50 pF R_L = 600 Ω f_{in} = 1 MHz (square wave) See figure 5		2.3 V	25°C	20 TYP		mV
				3.0 V	25°C	35 TYP		
				4.5 V	25°C	65 TYP		
Feed-through attenuation (switch off), COM or Y to Y or COM		C_L = 50 pF R_L = 600 Ω f_{in} = 1 MHz (sine wave) 2/ See figure 5		2.3 V	25°C	-45 TYP		dB
				3.0 V	25°C	-45 TYP		
				4.5 V	25°C	-45 TYP		
Sine wave distortion, COM or Y to Y or COM		C_L = 50 pF R_L = 10 kΩ f_{in} = 1 kHz (sine wave) See figure 5	V_I = 2.0 V_{p-p}	2.3 V	25°C	0.1 TYP		%
			V_I = 2.5 V_{p-p}	3.0 V	25°C	0.1 TYP		
			V_I = 4.0 V_{p-p}	4.5 V	25°C	0.1 TYP		

1/ Adjust f_{in} voltage to obtain 0 dBm output. Increase f_{in} frequency until dB meter reads –3 dB.
2/ Adjust f_{in} voltage to obtain 0 dBm input.

Case X

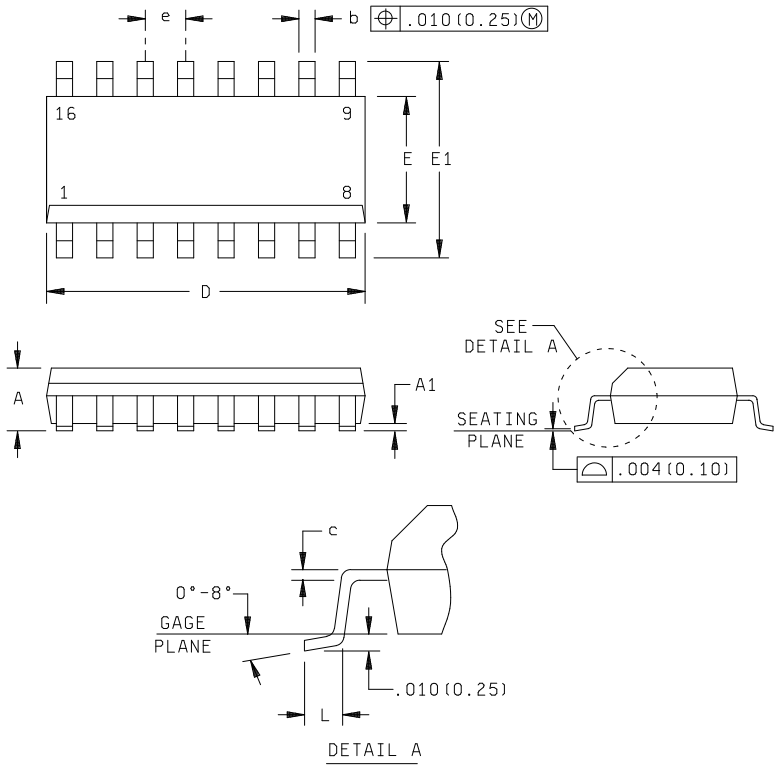


Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	.047	E	4.30	4.50	.169	.177
A1	0.05	0.15	.002	.006	E1	6.20	6.60	.244	.260
b	0.19	0.30	.007	.012	e	0.65 NOM		.026 NOM	
c	0.15 NOM		.006 NOM		L	0.50	0.75	.020	.030
D	4.90	5.10	.193	.201					

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm.
3. Falls within JEDEC MO-153.
4. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.

FIGURE 1. Case outlines.

Case Y



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	.069	---	1.75	E	.150	.157	3.81	4.00
A1	.004	.010	0.10	0.25	E1	.228	.244	5.80	6.20
b	.014	.020	0.35	0.51	e	.050 NOM		1.27 NOM	
c	.008 NOM		0.20 NOM		L	.016	.044	0.40	1.12
D	.386	.394	9.80	10.00					

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).
3. Falls within JEDEC MS-012.
4. All linear dimensions are shown in inches (millimeters). Millimeters equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

Inputs			On Channels
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

X = Immaterial

FIGURE 2. Truth table.

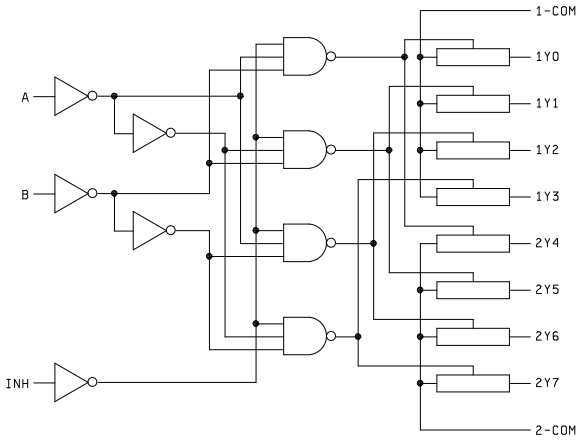
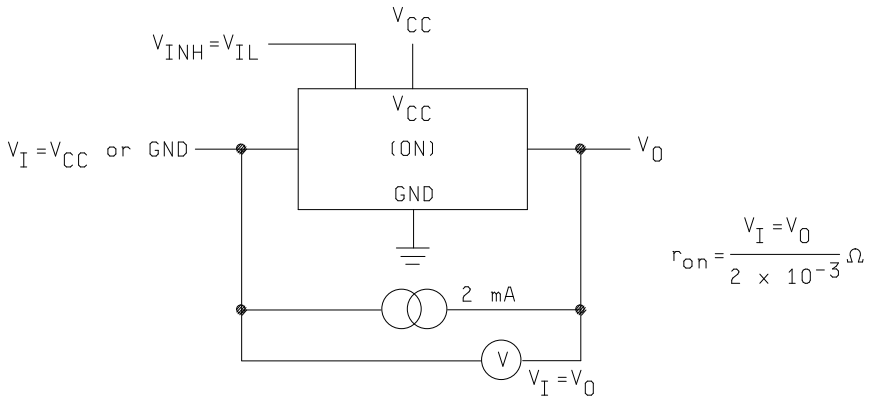


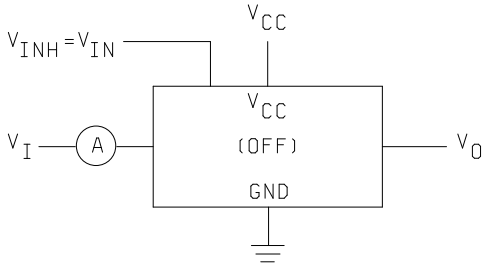
FIGURE 3. Logic diagram.

Device type	01		
Case outlines	X, Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	2Y0	9	B
2	2Y2	10	A
3	2-COM	11	1Y3
4	2Y3	12	1Y0
5	2Y1	13	1-COM
6	INH	14	1Y1
7	GND	15	1Y2
8	GND	16	V_{CC}

FIGURE 4. Terminal connections.

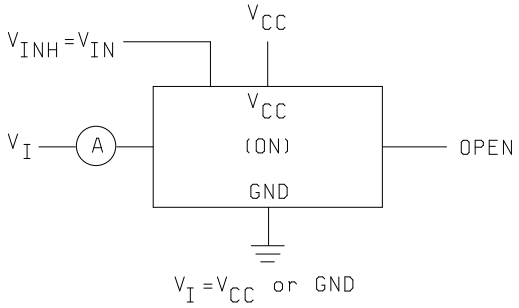


ON-STATE RESISTANCE TEST CIRCUIT



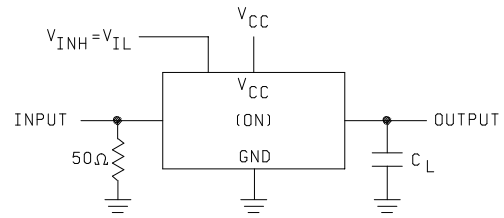
CONDITION 1: $V_I=0, V_O=V_{CC}$
CONDITION 2: $V_I=V_{CC}, V_O=0$

OFF-STATE SWITCH LEAKAGE-CURRENT TEST CIRCUIT

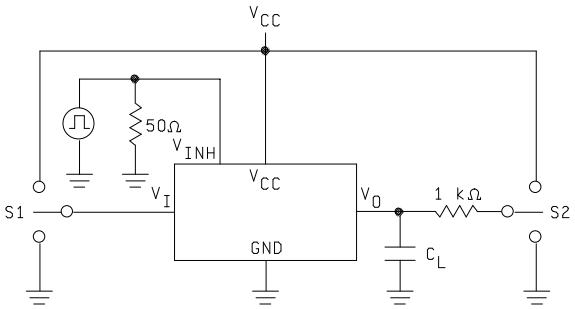


ON-STATE SWITCH LEAKAGE-CURRENT TEST CIRCUIT

FIGURE 5. Timing waveforms and test circuits.

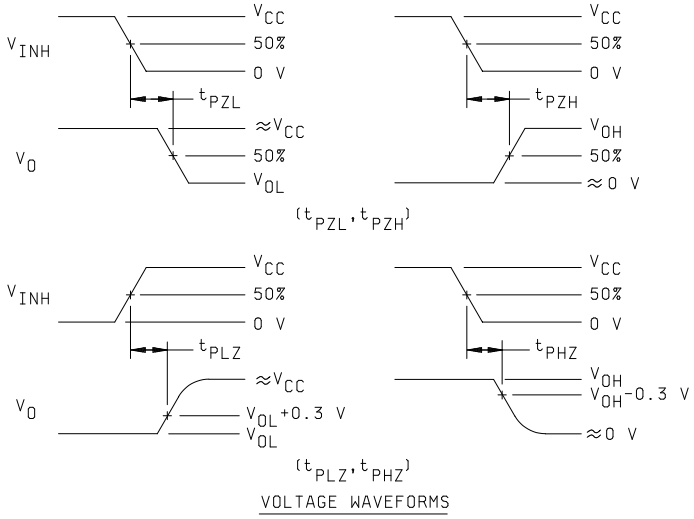


PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT



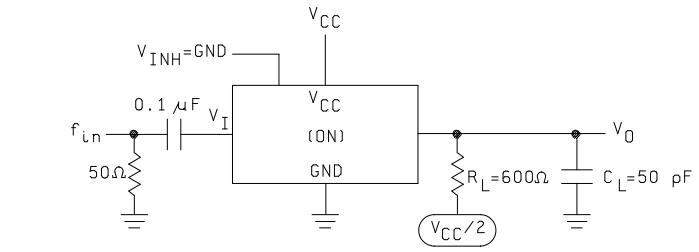
TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

TEST CIRCUIT

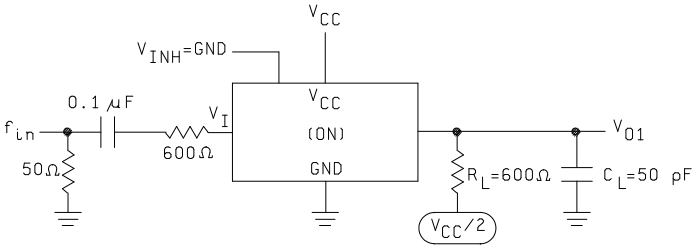


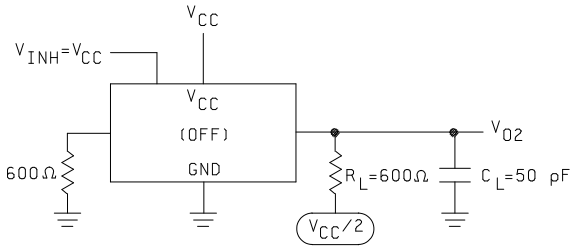
SWITCHING TIME (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

FIGURE 5. Timing waveforms and test circuits - Continued.

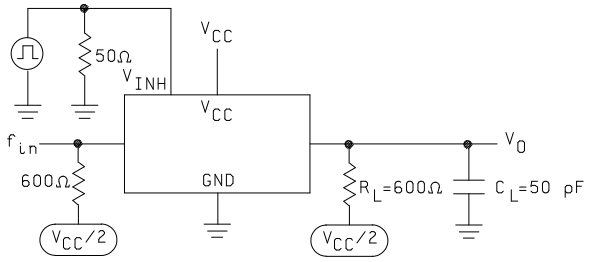


FREQUENCY RESPONSE (SWITCH ON)





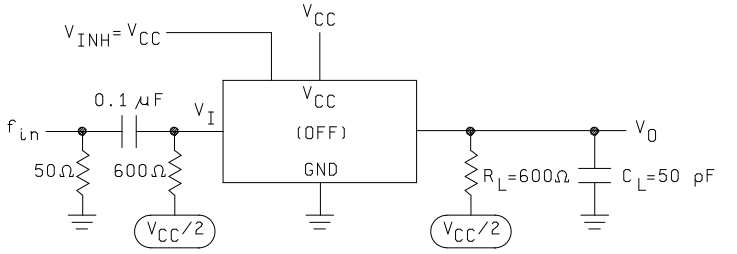
CROSSTALK BETWEEN ANY TWO SWITCHES



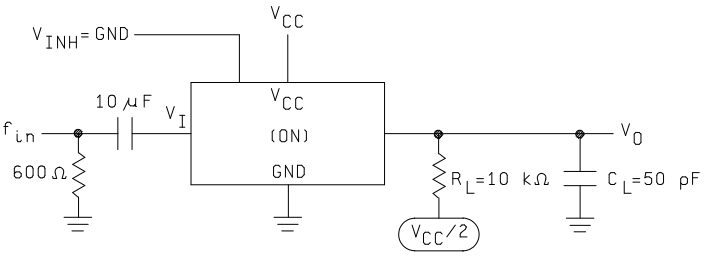
CROSSSTALK BETWEEN CONTROL INPUT AND SWITCH OUTPUT

NOTE: f_{in} is a sine wave.

FIGURE 5. Timing waveforms and test circuits - Continued.



FEED-THROUGH ATTENUATION(SWITCH OFF)



SINE-WAVE DISTORTION

FIGURE 5. Timing waveforms and test circuits - Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03665-01XE	01295	SN74LV4052ATPWREP	L4052EP
V62/03665-01YE	01295	SN74LV4052ATDREP	LV4052ATEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243