

| REVISIONS | | | |
|-----------|--|----------|----------------|
| LTR | DESCRIPTION | DATE | APPROVED |
| A | Add device type 02. Update boilerplate. Editorial change throughout. - phn | 06-02-22 | Thomas M. Hess |
| B | Add case outline Y. Update boilerplate to current revision. - CFS | 06-06-22 | Thomas M. Hess |
| C | Update boilerplate paragraphs to current requirements. - PHN | 12-06-04 | Thomas M. Hess |
| D | Update boilerplate to current MIL-PRF-38535 requirements. - PHN | 18-12-10 | Thomas M. Hess |



CURRENT DESIGN ACTIVITY CAGE CODE 16236
 HAS CHANGED NAMES TO:
 DLA LAND AND MARITIME
 COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | | |
|--|----------------------------------|--------------------------|---|---|---|---|---|---|-----------------------------|---|---|----|----|--|--|--|--|--|--|--|--|
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| REV STATUS OF PAGES | REV | | D | D | D | D | D | D | D | D | D | D | D | | | | | | | | |
| | PAGE | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | | | | | | |
| PMIC N/A | PREPARED BY Charles F. Saffle | | | | | | | DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990 | | | | | | | | | | | | | |
| Original date of drawing YY-MM-DD 03-09-02 | CHECKED BY Charles F. Saffle | | | | | | | TITLE MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, HEX SCHMITT-TRIGGER INVERTER, MONOLITHIC SILICON | | | | | | | | | | | | | |
| | APPROVED BY Thomas M. Hess | | | | | | | | | | | | | | | | | | | | |
| | SIZE A | CODE IDENT. NO. 16236 | | | | | | | DWG NO. V62/03662 | | | | | | | | | | | | |
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance hex Schmitt-trigger inverter microcircuit, with an operating temperature range of -40°C to +105°C for device 01, and of -55°C to +125°C for device 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| | | | | |
|------------------|---|----------------------------|-----------------------------|----------------------------|
| <u>V62/03662</u> | - | <u>01</u> | <u>X</u> | <u>E</u> |
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| <u>Device type</u> | <u>Generic</u> | <u>Circuit function</u> |
|--------------------|----------------|------------------------------|
| 01 | SN74LV14AT-EP | Hex Schmitt-trigger inverter |
| 02 | SN74LV14AM-EP | Hex Schmitt-trigger inverter |

1.2.2 Case outline. The case outline(s) are as specified herein.

| <u>Outline letter</u> | <u>Number of pins</u> | <u>JEDEC PUB 95</u> | <u>Package style</u> |
|-----------------------|-----------------------|---------------------|-----------------------|
| X | 14 | JEDEC MO-153 | Plastic small-outline |
| Y | 14 | JEDEC MS-012 | Plastic small-outline |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| <u>Finish designator</u> | <u>Material</u> |
|--------------------------|----------------------|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| Z | Other |

| | | | |
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1.3 Absolute maximum ratings. 1/

| | |
|--|----------------------------------|
| Supply voltage range (V_{CC}) | -0.5 V to +7.0 V |
| Input voltage range (V_i) | -0.5 V to +7.0 V 2/ |
| Voltage range applied to any output in the high-impedance or power-off state (V_o) | -0.5 V to +7.0 V 2/ 3/ |
| Output voltage range (V_o) | -0.5 V to $V_{CC} + 0.5 V$ 2/ 3/ |
| Input clamp current (I_{IK}) ($V_i < 0$) | -20 mA |
| Output clamp current (I_{OK}) ($V_o < 0$ or $V_o > V_{CC}$) | ± 50 mA |
| Continuous output current (I_o) ($V_o = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Package thermal impedance (θ_{JA}) | 113°C/W 4/ |
| Storage temperature range (T_{STG}) | -65°C to +150°C |

1.4 Recommended operating conditions. 5/

| | |
|---|---------------------|
| Supply voltage range (V_{CC}) | 2.0 V to 5.5 V |
| Minimum high level input voltage (V_{IH}): | |
| $V_{CC} = 2.0 V$ | 1.5 V |
| $V_{CC} = 2.3 V$ to 2.7 V | $V_{CC} \times 0.7$ |
| $V_{CC} = 3.0 V$ to 3.6 V | $V_{CC} \times 0.7$ |
| $V_{CC} = 4.5 V$ to 5.5 V | $V_{CC} \times 0.7$ |
| Maximum low level input voltage (V_{IL}): | |
| $V_{CC} = 2.0 V$ | 0.5 V |
| $V_{CC} = 2.3 V$ to 2.7 V | $V_{CC} \times 0.3$ |
| $V_{CC} = 3.0 V$ to 3.6 V | $V_{CC} \times 0.3$ |
| $V_{CC} = 4.5 V$ to 5.5 V | $V_{CC} \times 0.3$ |
| Input voltage range (V_i) | 0.0 V to 5.5 V |
| Output voltage range (V_o) | 0.0 V to V_{CC} |
| Maximum high level output current (I_{OH}): | |
| $V_{CC} = 2.0 V$ | -50 μA |
| $V_{CC} = 2.3 V$ to 2.7 V | -2 mA |
| $V_{CC} = 3.0 V$ to 3.6 V | -6 mA |
| $V_{CC} = 4.5 V$ to 5.5 V | -12 mA |
| Maximum low level output current (I_{OL}): | |
| $V_{CC} = 2.0 V$ | 50 μA |
| $V_{CC} = 2.3 V$ to 2.7 V | 2 mA |
| $V_{CC} = 3.0 V$ to 3.6 V | 6 mA |
| $V_{CC} = 4.5 V$ to 5.5 V | 12 mA |
| Operating free-air temperature range (T_A) | |
| Device type 01 | -40°C to +105°C |
| Device type 02 | -55°C to +125°C |

- 1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 3/ This value is limited to 5.5 V maximum.
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at <https://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions -40°C ≤ T _A ≤ 105°C 2/ -55°C ≤ T _A ≤ 125°C 3/ unless otherwise specified | V _{CC} | Device type 01 | | Device type 02 | | Unit |
|---|------------------|--|-----------------|-----------------------|---------|-----------------------|---------|------|
| | | | | Limits | | Limits | | |
| | | | | Min | Max | Min | Max | |
| Positive-going threshold voltage | V _{T+} | | 2.5 V | | 1.75 | | 1.78 | V |
| | | | 3.3 V | | 2.31 | | 2.31 | |
| | | | 5.0 V | | 3.5 | | 3.5 | |
| Negative-going threshold voltage | V _{T-} | | 2.5 V | 0.75 | | 0.75 | | V |
| | | | 3.3 V | 0.99 | | 0.99 | | |
| | | | 5.0 V | 1.5 | | 1.5 | | |
| Hysteresis (V _{T+} - V _{T-}) voltage | ΔV _T | | 2.5 V | 0.25 | 1.0 | 0.25 | 1.0 | V |
| | | | 3.3 V | 0.33 | 1.32 | 0.33 | 1.32 | |
| | | | 5.0 V | 0.5 | 2.0 | 0.5 | 2.0 | |
| High level output voltage | V _{OH} | I _{OH} = -50 μA | 2.0 V to 5.5 V | V _{CC} - 0.1 | | V _{CC} - 0.1 | | V |
| | | I _{OH} = -2 mA | 2.3 V | 2.0 | | 2.0 | | |
| | | I _{OH} = -6 mA | 3.0 V | 2.48 | | 2.48 | | |
| | | I _{OH} = -12 mA | 4.5 V | 3.8 | | 3.8 | | |
| Low level output voltage | V _{OH} | I _{OL} = 50 μA | 2.0 V to 5.5 V | | 0.1 | | | V |
| | | I _{OL} = 2 mA | 2.3 V | | 0.4 | | | |
| | | I _{OL} = 6 mA | 3.0 V | | 0.44 | | | |
| | | I _{OL} = 12 mA | 4.5 V | | 0.55 | | | |
| Input current | I _I | V _I = V _{CC} or GND | 0.0 V to 5.5 V | | ±1.0 | | | μA |
| Quiescent supply current | I _{CC} | V _I = V _{CC} or GND I _O = 0 A | 5.5 V | | 20.0 | | | μA |
| Input/output power-off leakage current | I _{off} | V _I or V _O = 0.0 V to 5.5 V | 0.0 V | | 5.0 | | | μA |
| Input capacitance | C _i | V _I = V _{CC} or GND | 3.3 V | | 2.3 Typ | | 2.3 Typ | pF |
| | | | 5.0 V | | 2.3 Typ | | 2.3 Typ | |
| Power dissipation capacitance | C _{pd} | C _L = 50 pF f = 10 MHz | 3.3 V | | 8.8 Typ | | 8.8 Typ | |
| | | | 5.0 V | | 9.6 Typ | | 9.6 Typ | |

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

| Test | Symbol | Conditions -40°C ≤ T _A ≤ 105°C 2/ -55°C ≤ T _A ≤ 125°C 3/ unless otherwise specified | V _{CC} | Device type 01 | | Device type 02 | | Unit |
|--|--|---|-----------------|----------------|------|----------------|------|------|
| | | | | Limits | | Limits | | |
| | | | | Min | Max | Min | Max | |
| Quiet output, maximum dynamic V _{OL} | V _{OL(P)} 4/ | C _L = 50 pF, T _A = 25°C | 3.3 V | | 0.8 | | 0.8 | V |
| Quiet output, minimum dynamic V _{OL} | V _{OL(V)} 4/ | | 3.3 V | | -0.8 | | -0.8 | V |
| Quiet output, minimum dynamic V _{OH} | V _{OH(V)} 4/ | | 3.3 V | 3.1 TYP | | 3.1 TYP | | V |
| High level dynamic input voltage | V _{IH(D)} 4/ | | 3.3 V | 2.31 | | 2.31 | | V |
| Low level dynamic input voltage | V _{IL(D)} 4/ | | 3.3 V | | 0.99 | | 0.99 | V |
| Propagation delay time, from input A to output Y | t _{PLH} , t _{PHL} | C _L = 50 pF, T _A = 25°C See figure 5 | 3.3 V ± 0.3V | | 16.3 | | 16.3 | ns |
| | | | 5.0 V ± 0.5V | | 10.6 | | 10.6 | |
| Propagation delay time, from input A to output Y | t _{PLH} , t _{PHL} | C _L = 50 pF See figure 5 | 3.3 V ± 0.3V | 1.0 | 20.4 | 1.0 | 20.4 | |
| | | | 5.0 V ± 0.5V | 1.0 | 14 | 1.0 | 14 | |

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

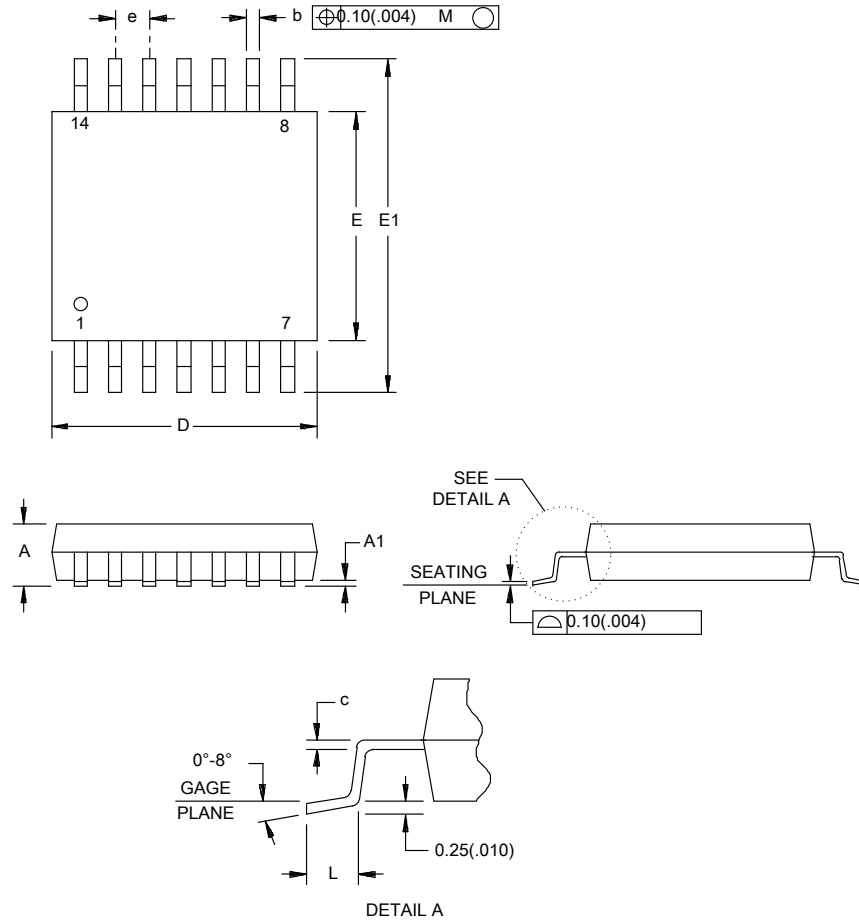
2/ For device type 01 only.

3/ For device type 02 only.

4/ Characteristics are for surface-mount packages only.

| | | | |
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Case X



| Dimensions | | | | | | | | | |
|------------|-------------|------|----------|------|--------|-------------|------|----------|------|
| Symbol | Millimeters | | Inches | | Symbol | Millimeters | | Inches | |
| | Min | Max | Min | Max | | Min | Max | Min | Max |
| A | --- | 1.20 | --- | .047 | E | 4.30 | 4.50 | .169 | .177 |
| A1 | 0.05 | 0.15 | .002 | .006 | E1 | 6.20 | 6.60 | .244 | .260 |
| b | 0.19 | 0.30 | .007 | .012 | e | 0.65 NOM | | .026 NOM | |
| c | 0.15 NOM | | .006 NOM | | L | 0.50 | 0.75 | .020 | .030 |
| D | 4.90 | 5.10 | .193 | .201 | | | | | |

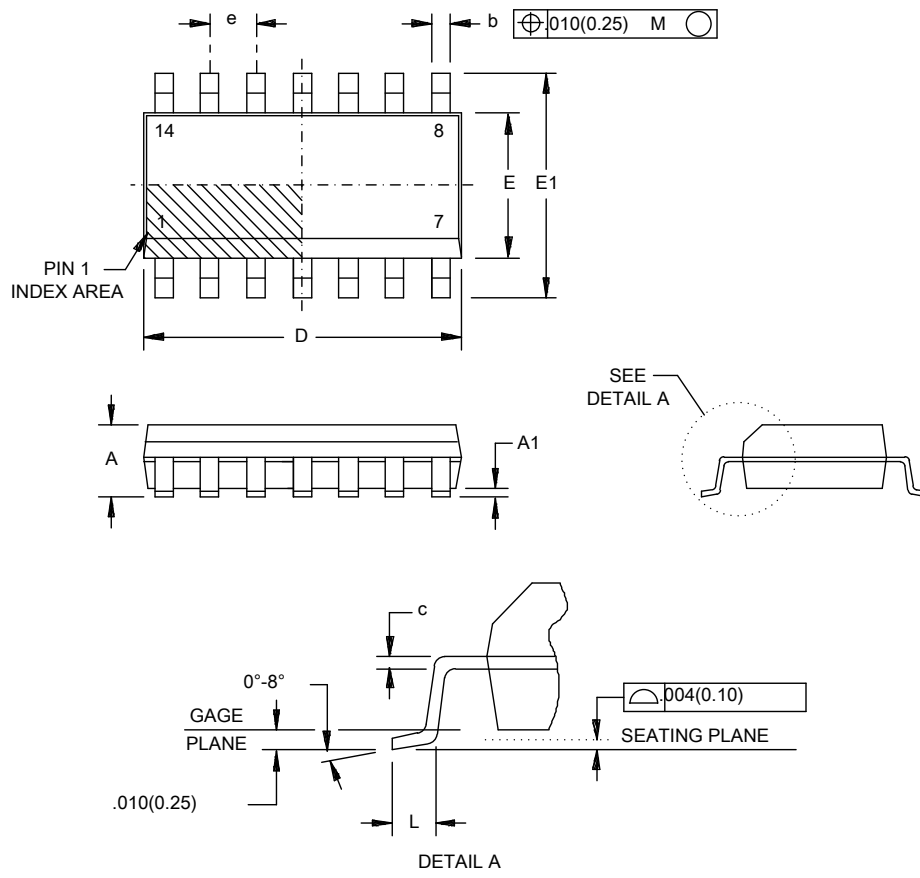
NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm.
3. Falls within JEDEC MO-153.
4. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.

FIGURE 1. Case outlines.

| | | | |
|---|------------------|--------------------------------|-----------------------------|
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Case Y



| Dimensions | | | | | | | | | |
|------------|--------|-------|-------------|------|--------|-----------|-------|-------------|------|
| Symbol | Inches | | Millimeters | | Symbol | Inches | | Millimeters | |
| | Min | Max | Min | Max | | Min | Max | Min | Max |
| A | --- | 0.069 | --- | 1.75 | E | 0.150 | 0.157 | 3.80 | 4.00 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 | E1 | 0.228 | 0.244 | 5.80 | 6.20 |
| b | 0.012 | 0.020 | 0.31 | 0.51 | e | 0.050 NOM | | 1.27 NOM | |
| c | 0.007 | 0.010 | 0.17 | 0.25 | L | 0.016 | 0.050 | 0.40 | 1.27 |
| D | 0.337 | 0.344 | 8.55 | 8.75 | | | | | |

NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).
3. Falls within JEDEC MS-012, variation AB.
4. All linear dimensions are shown in inches (millimeters). Millimeters equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

| | | | |
|---|------------------|--------------------------------|-----------------------------|
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(each inverter)

| Input A | Output Y |
|------------|-------------|
| H | L |
| L | H |

FIGURE 2. Truth table.

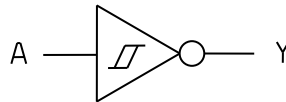
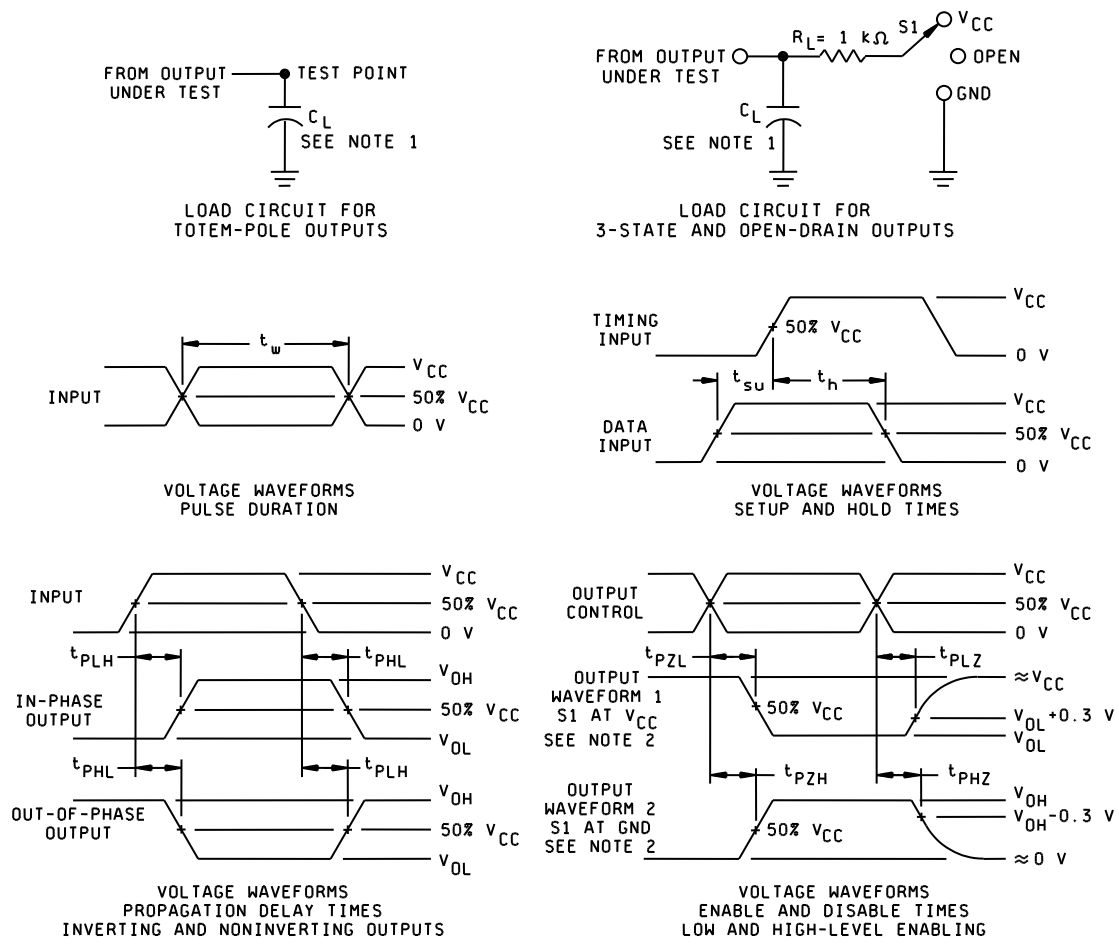


FIGURE 3. Logic diagram.

| | | | |
|-----------------|-----------------|-----------------|-----------------|
| Device types: | 01 and 02 | | |
| Case outlines: | X and Y | | |
| Terminal number | Terminal symbol | Terminal number | Terminal symbol |
| 1 | 1A | 8 | 4Y |
| 2 | 1Y | 9 | 4A |
| 3 | 2A | 10 | 5Y |
| 4 | 2Y | 11 | 5A |
| 5 | 3A | 12 | 6Y |
| 6 | 3Y | 13 | 6A |
| 7 | GND | 14 | V _{CC} |

FIGURE 4. Terminal connections.

| | | | |
|---|-------------------|---------------------------------|------------------------------|
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Notes:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50\Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
4. The outputs are measured one at a time with one input transition per measurement.
5. For 3-state and Open Drain outputs tests:

| | |
|-------------------|---------------|
| t_{PLH}/t_{PHL} | S1 = Open |
| t_{PLZ}/t_{PZL} | S1 = V_{CC} |
| t_{PHZ}/t_{PZH} | S1 = GND |
| Open Drain | S1 = V_{CC} |

FIGURE 5. Timing waveforms and test circuit.

| | | | |
|---|-------------------|---------------------------------|------------------------------|
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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

| Vendor item drawing administrative control number <u>1/</u> | Device manufacturer CAGE code | Vendor part number | Top-Side Marking |
|---|-------------------------------|--------------------|------------------|
| V62/03662-01XE | 01295 | SN74LV14ATPWREP | LV14AEP |
| V62/03662-02XE | 01295 | SN74LV14AMPWREP | LV14AEP |
| V62/03662-02YE | 01295 | SN74LV14AMDREP | LV14AEP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest lane
P.O. Box 660199
Dallas, TX 75243

| | | | |
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