

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	09-11-09	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-11-20	Thomas M. Hess



**CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor item drawing

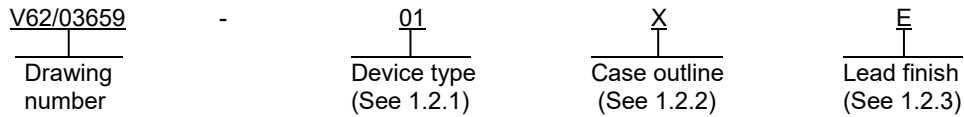
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REV STATUS OF PAGES	REV	B	B	B	B	B	B	B	B	B	B	B	B							
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PMIC N/A	PREPARED BY Charles F. Saffle								DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990										
Original date of drawing YY-MM-DD 03-09-02	CHECKED BY Charles F. Saffle								TITLE MICROCIRCUIT, DIGITAL, ADVANCED HIGH SPEED CMOS, DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET, AND TTL COMPATIBLE INPUTS, MONOLITHIC SILICON										
	APPROVED BY Thomas M. Hess																		
	SIZE A	CODE IDENT. NO. 16236							DWG NO. V62/03659										
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual positive-edge-triggered D-type flip-flop with clear and preset, and TTL compatible inputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	74AHCT74-EP	Dual positive-edge-triggered D-type flip-flop with clear and preset, and TTL compatible inputs

1.2.2 Case outlines. The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	14	JEDEC MO-153	Plastic small-outline
Y	14	JEDEC MS-012	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +7.0 V
Input voltage range (V_i)	-0.5 V to +7.0 V 2/
Output voltage range (V_o)	-0.5 V to $V_{CC} + 0.5$ V 2/
Input clamp current (I_{IK}) ($V_i < 0$)	-20 mA
Output clamp current (I_{OK}) ($V_o < 0$ or $V_o > V_{CC}$)	± 20 mA
Continuous output current (I_o) ($V_o = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance (θ_{JA}):	
X package	113°C/W 3/
Y package	86°C/W 3/
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Minimum high level input voltage (V_{IH})	2.0 V
Maximum low level input voltage (V_{IL})	0.8 V
Input voltage range (V_i)	0.0 V to 5.5 V
Output voltage range (V_o)	0.0 V to V_{CC}
Maximum high level output current (I_{OH})	-8.0 mA
Maximum low level output current (I_{OL})	8.0 mA
Input transition rise or fall rate ($\Delta t/\Delta v$)	20 ns/V
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95	-	Registered and Standard Outlines for Semiconductor Devices
JESD 51-7	-	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at <https://www.jedec.org>)

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 3/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
High level output voltage	V _{OH}	I _{OH} = -50 μA	4.5 V	25°C, -55°C to 125°C	01	4.4		V
		I _{OH} = -8 mA	4.5 V	25°C		3.94		
				-55°C to 125°C		3.80		
Low level output voltage	V _{OL}	I _{OL} = 50 μA	4.5 V	25°C, -55°C to 125°C	01		0.1	V
		I _{OL} = 8 mA	4.5 V	25°C			0.36	
				-55°C to 125°C			0.44	
Input current	I _I	V _I = 5.5 V or GND	0.0 V to 5.5 V	25°C	01		±0.1	μA
				-55°C to 125°C			±1.0	
Quiescent supply current	I _{CC}	V _I = V _{CC} or GND I _O = 0 A	5.5 V	25°C	01		2.0	μA
				-55°C to 125°C			20.0	
Quiescent supply current delta, TTL input levels	ΔI _{CC} 2/	One input at 3.4 V. Other inputs at V _{CC} or GND.	5.5 V	25°C	01		1.35	mA
				-55°C to 125°C			1.5	
Input capacitance	C _I	V _I = V _{CC} or GND	5.0 V	25°C	01		10	pF
Power dissipation capacitance	C _{pd}	No load f = 1 MHz	5.0 V	25°C	01	32 TYP		pF
Quiet output, maximum dynamic V _{OL}	V _{OL(P)} 3/	C _L = 50 pF	5.0 V	25°C	01		0.8	V
Quiet output, minimum dynamic V _{OL}	V _{OL(V)} 3/		5.0 V	25°C	01		-0.8	V
Quiet output, minimum dynamic V _{OH}	V _{OH(V)} 3/		5.0 V	25°C	01	4.0		V
High level dynamic input voltage	V _{IH(D)} 3/		5.0 V	25°C	01	2.0		V
Low level dynamic input voltage	V _{IL(D)} 3/		5.0 V	25°C	01		0.8	V

See footnotes at end of table.

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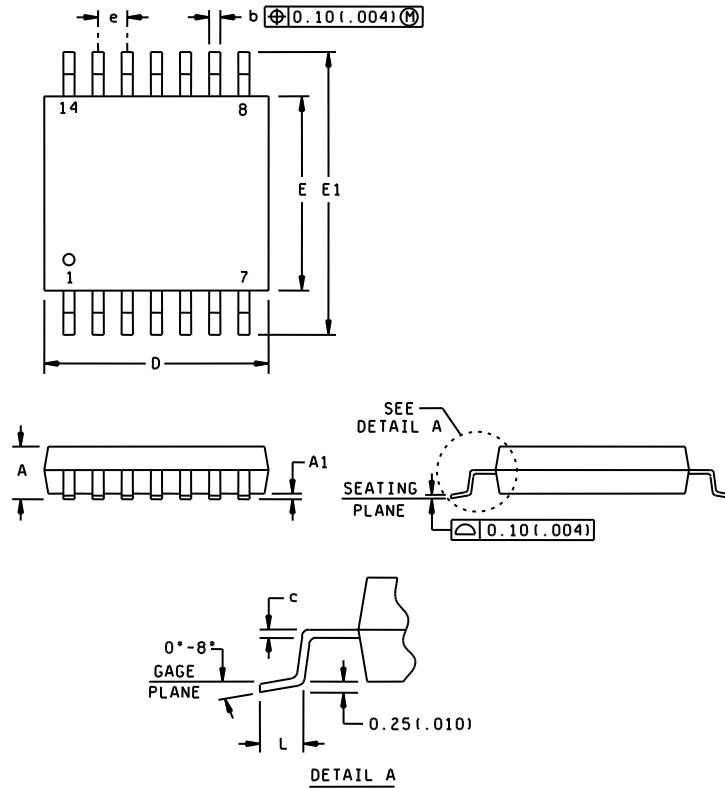
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V _{CC}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Maximum operating frequency	f _{max}	C _L = 15 pF See figure 5	4.5 V and 5.5 V	25°C	01	100		MHz
				-55°C to 125°C		80		
		C _L = 50 pF See figure 5	4.5 V and 5.5 V	25°C		80		
				-55°C to 125°C		65		
Propagation delay time, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ to Q or $\overline{\text{Q}}$	t _{PLH} , t _{PHL}	C _L = 15 pF See figure 5	4.5 V and 5.5 V	25°C	01		10.4	ns
				-55°C to 125°C		1.0	12.0	
		C _L = 50 pF See figure 5	4.5 V and 5.5 V	25°C			11.4	
				-55°C to 125°C		1.0	13.0	
Propagation delay time, CLK to Q or $\overline{\text{Q}}$	t _{PLH} , t _{PHL}	C _L = 15 pF See figure 5	4.5 V and 5.5 V	25°C	01		7.8	ns
				-55°C to 125°C		1.0	9.0	
		C _L = 50 pF See figure 5	4.5 V and 5.5 V	25°C			8.8	
				-55°C to 125°C		1.0	10.0	
Pulse duration	t _w	PRE or CLR low See figure 5	4.5 V and 5.5 V	25°C, -55°C to 125°C	01	5.0		ns
		CLK See figure 5				5.0		
Setup time before CLK↑	t _{su}	Data See figure 5	4.5 V and 5.5 V	25°C, -55°C to 125°C	01	5.0		ns
		PRE or CLR inactive See figure 5				3.5		
Hold time, data after CLK↑	t _h	See figure 5	4.5 V and 5.5 V	25°C, -55°C to 125°C	01	0.0		ns

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.
- 2/ Characteristics are for surface-mount packages only.

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Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	.047	E	4.30	4.50	.169	.177
A1	0.05	0.15	.002	.006	E1	6.20	6.60	.244	.260
b	0.19	0.30	.007	.012	e	0.65 NOM		.026 NOM	
c	0.15 NOM		.006 NOM		L	0.50	0.75	.020	.030
D	4.90	5.10	.193	.201					

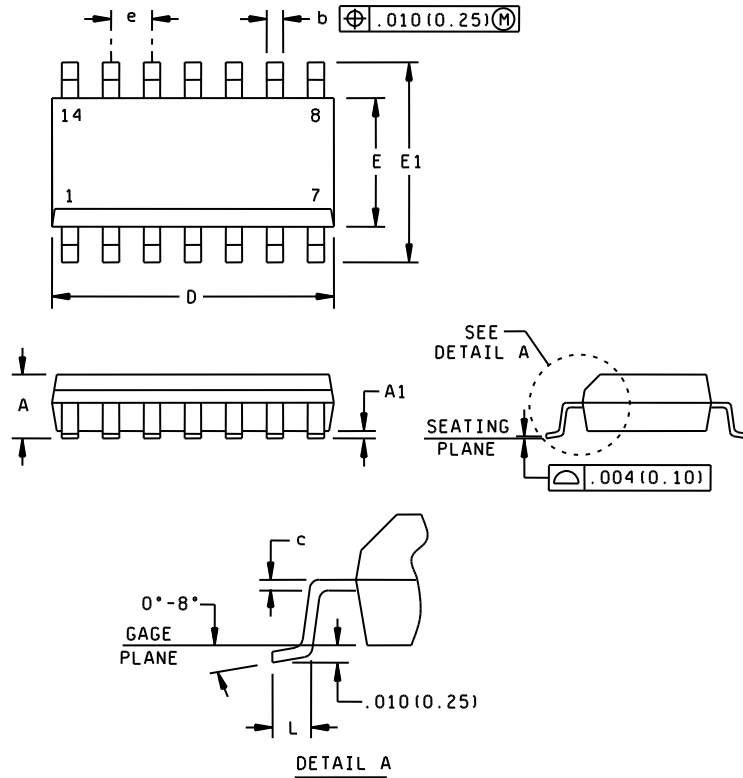
NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm.
3. Falls within JEDEC MO-153.
4. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.

FIGURE 1. Case outlines.

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Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.75	---	.069	E	3.81	4.00	.150	.157
A1	0.10	0.25	.004	.010	E1	5.80	6.20	.228	.244
b	0.35	0.51	.014	.020	e	1.27 NOM		.050 NOM	
c	0.20 NOM		.008 NOM		L	0.40	1.12	.016	.044
D	8.55	8.75	.337	.344					

NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inches (0.15 mm).
3. Falls within JEDEC MS-012.
4. All linear dimensions are shown in inches (millimeters). Metric equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

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(each flip-flop)

Inputs				Outputs	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q ₀

X = Immaterial

↑ = Rising edge of CLK

* = This configuration is unstable; that is it does not persist when PRE or CLR returns to its inactive (high) level.

FIGURE 2. Truth table.

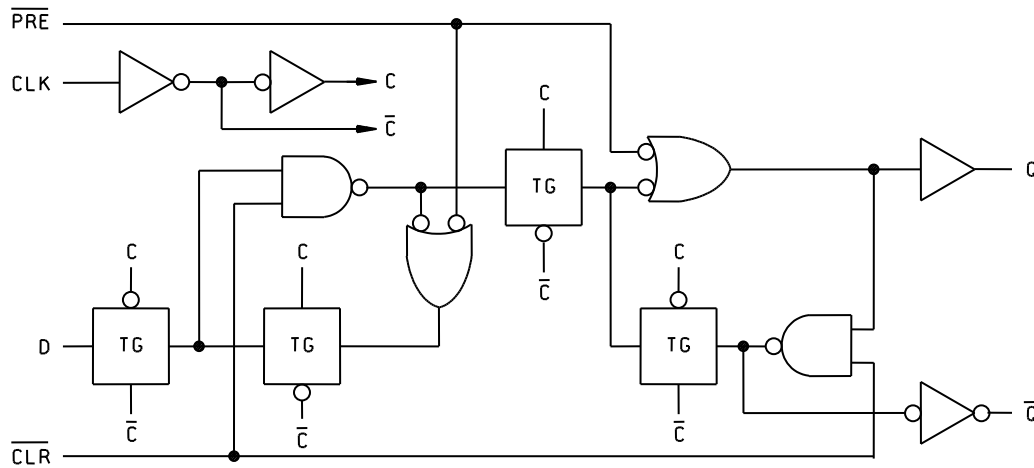


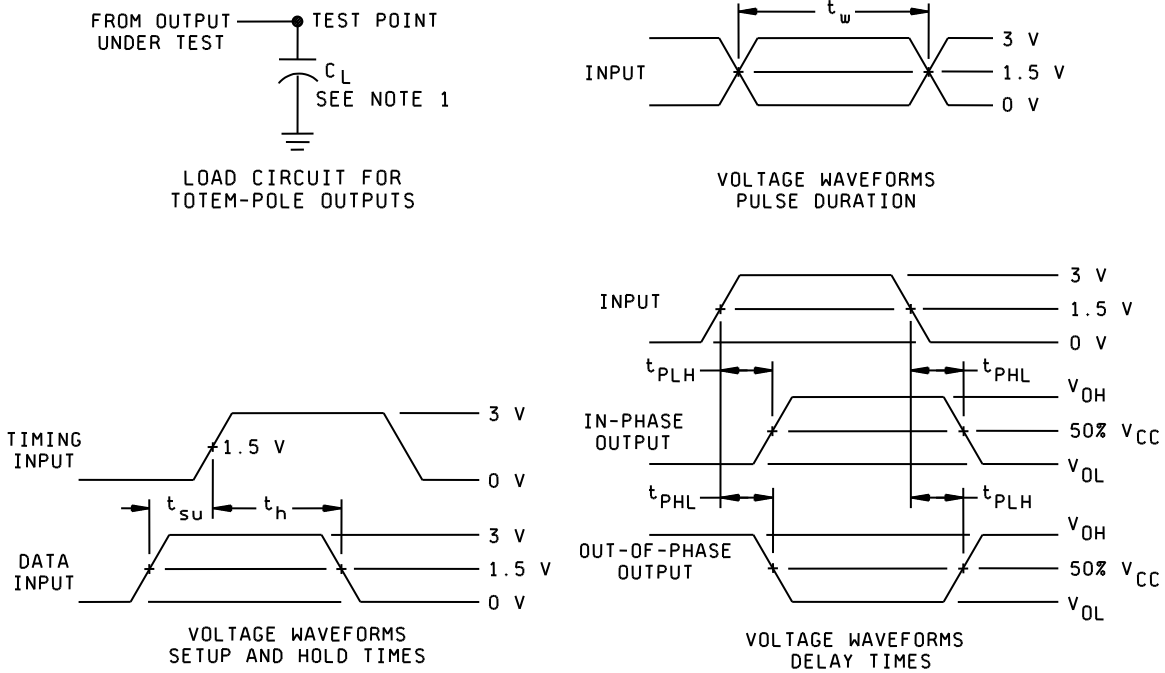
FIGURE 3. Logic diagram.

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Device type	01
Case outlines	X, Y
Terminal number	Terminal symbol
1	1CLR
2	1D
3	1CLK
4	1PRE
5	1Q
6	1Q
7	GND
8	2Q
9	2Q
10	2PRE
11	2CLK
12	2D
13	2CLR
14	V _{cc}

FIGURE 4. Terminal connections.

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Notes:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_o = 50\Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
3. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Timing waveforms and test circuit.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03659-01XE	01295	SN74AHCT74MPWREP	AHT74EP
V62/03659-01YE	01295	SN74AHCT74MDREP	AHCT74MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest lane
P.O. Box 660199
Dallas, TX 75243

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