REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	09-02-25	Charles F. Saffle
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	15-08-25	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	22-05-18	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C												
SHEET	1	2	3	4	5	6	7	8	9	10												

PMIC N/A

Original date of drawing

YY MM DD

03-07-29

PREPARED BY
Charles F. Saffle

CHECKED BY
Charles F. Saffle

APPROVED BY
Charles F. Saffle

DEFENSE SUPPLY CENTER, COLUMBUS
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

TITLE
MICROCIRCUIT, ADVANCED HIGH SPEED CMOS, QUADRUPLE 2-INPUT POSITIVE NOR GATE, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/03645
REV C		PAGE 1 OF 10

AMSC N/A

5962-V055-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quadruple 2-input positive NOR gate microcircuit, with an operating temperature range of-55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03645	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	74AHC02-EP	Quadruple 2-input positive NOR gate

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	JEDEC MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +7.0 V
Input voltage range (V_I)	-0.5 V to +7.0 V 2/
Output voltage range (V_O)	-0.5 V to V_{CC} + 0.5 V 2/
Input clamp current (I_{IK}) (V_I < 0)	-20 mA
Output clamp current (I_{OK}) (V_O < 0 or V_O > V_{CC})	±20 mA
Continuous output current (I_O) (V_O = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance (Θ_{JA})	113ºC/W 3/
Maximum junction temperature (T_J)	150ºC
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (V_{CC})	2.0 V to 5.5 V
Minimum high level input voltage (V_{IH}):	
V_{CC} = 2.0 V	1.5 V
V_{CC} = 3.0 V	2.1 V
V_{CC} = 5.5 V	3.85 V
Maximum low level input voltage (V_{IL}):	
V_{CC} = 2.0 V	0.5 V
V_{CC} = 3.0 V	0.9 V
V_{CC} = 5.5 V	1.65 V
Input voltage range (V_I)	0.0 V to 5.5 V
Output voltage range (V_O)	0.0 V to V_{CC}
Maximum high level output current (I_{OH}):	
V_{CC} = 2.0 V	-50 µA
V_{CC} = 3.3 V ±0.3 V	-4.0 mA
V_{CC} = 5.0 V ±0.5 V	-8.0 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 2.0 V	50 µA
V_{CC} = 3.3 V ±0.3 V	4.0 mA
V_{CC} = 5.0 V ±0.5 V	8.0 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$):	
V_{CC} = 3.3 V ±0.3 V	100 ns/V
V_{CC} = 5.0 V ±0.5 V	20 ns/V
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ The package thermal impedance is calculated in accordance with JESD 51-7.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	I_{OH} = -50 μA	2.0 V	25°C,	01	1.9		V
			3.0 V	-55°C to 125°C		2.9		
			4.5 V			4.4		
		I_{OH} = -4 mA	3.0 V	25°C		2.58		
				-55°C to 125°C		2.48		
		I_{OH} = -8 mA	4.5 V	25°C		3.94		
				-55°C to 125°C		3.80		
Low level output voltage	V_{OL}	I_{OL} = 50 μA	2.0 V	25°C,	01		0.1	V
			3.0 V	-55°C to 125°C			0.1	
			4.5 V				0.1	
		I_{OL} = 4 mA	3.0 V	25°C			0.36	
				-55°C to 125°C			0.5	
		I_{OL} = 8 mA	4.5 V	25°C			0.36	
				-55°C to 125°C			0.5	
Input current	I_I	V_I = 5.5 V or GND	0.0 V to 5.5 V	25°C	01		±0.1	μA
				-55°C to 125°C			±1.0	
Quiescent supply current	I_{CC}	V_I = V_{CC} or GND I_O = 0 A	5.5 V	25°C	01		2.0	μA
				-55°C to 125°C			20.0	
Input capacitance	C_I	V_I = V_{CC} or GND	5.0 V	25°C	01		10	pF
Power dissipation capacitance	C_{pd}	No load f = 1 MHz	5.0 V	25°C	01	15	TYP	pF
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$ 2/	C_L = 50 pF	5.0 V	25°C	01		0.8	V
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$ 2/		5.0 V	25°C	01		-0.8	V
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$ 2/		5.0 V	25°C	01	4.9		V
High level dynamic input voltage	$V_{IH(D)}$ 2/		5.0 V	25°C	01	3.5		V
Low level dynamic input voltage	$V_{IL(D)}$ 2/		5.0 V	25°C	01		1.5	V

See footnote at end of table.

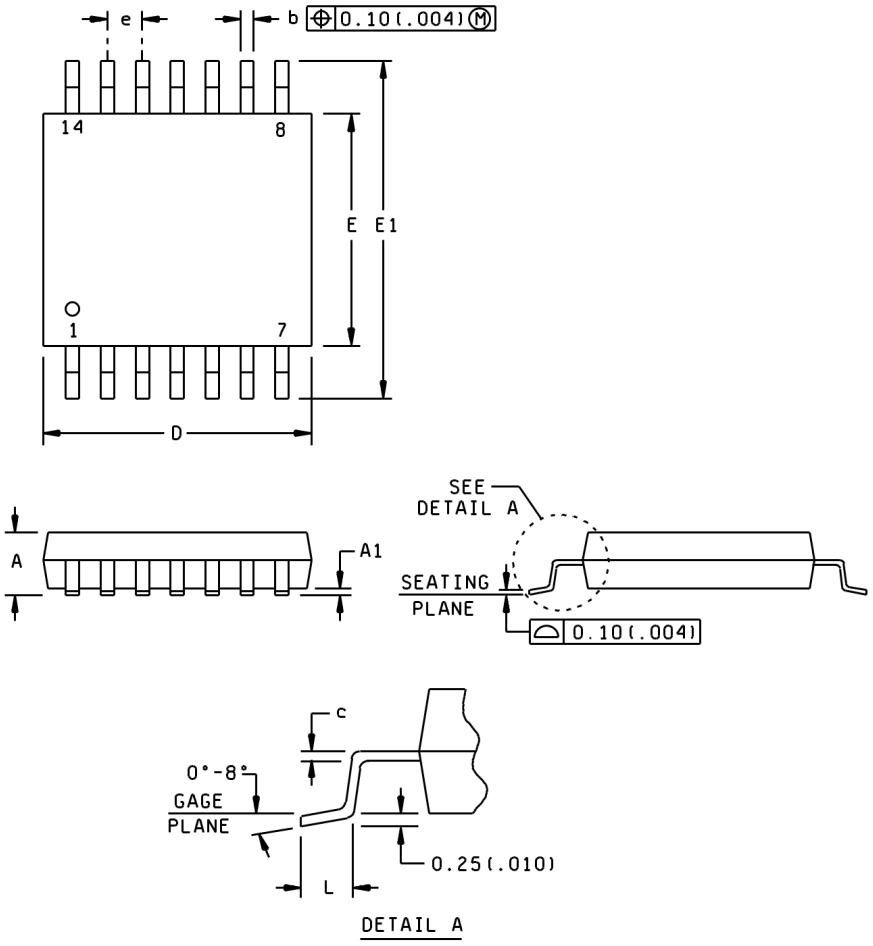
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Propagation delay time, A or B to Y	t_{PLH}, t_{PHL}	C_L = 15 pF See figure 5	3.0 V and 3.6 V	25°C	01		7.9	ns
				-55°C to 125°C		1.0	9.5	
			4.5 V and 5.5 V	25°C			5.5	
				-55°C to 125°C		1.0	6.5	
		C_L = 50 pF See figure 5	3.0 V and 3.6 V	25°C	01		11.4	
				-55°C to 125°C		1.0	13.0	
			4.5 V and 5.5 V	25°C			7.5	
				-55°C to 125°C		1.0	8.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Characteristics are for surface-mount packages only.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	1.20	---	.047	E	4.30	4.50	.169	.177
A1	0.05	0.15	.002	.006	E1	6.20	6.60	.244	.260
b	0.19	0.30	.007	.012	e	0.65 NOM		.026 NOM	
c	0.15 NOM		.006 NOM		L	0.50	0.75	.020	.030
D	4.90	5.10	.193	.201					

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm.
3. Falls within JEDEC MO-153.
4. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.

FIGURE 1. Case outlines.

(each gate)

Inputs		Output
A	B	Y
H	X	L
X	H	L
L	L	H

X = Immaterial

FIGURE 2. Truth table.

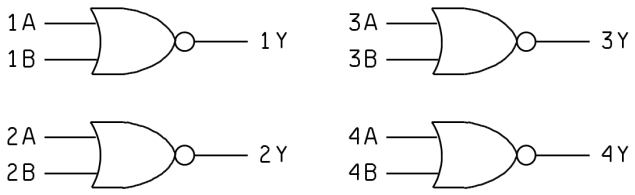


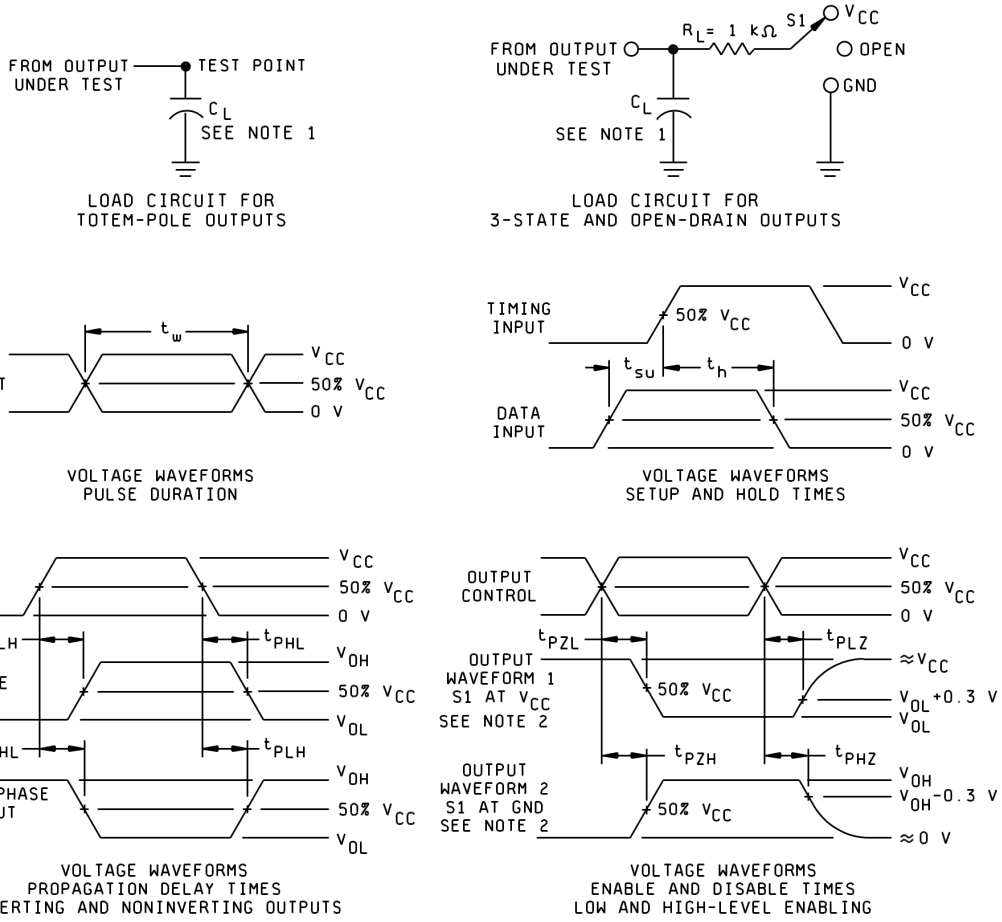
FIGURE 3. Logic diagram.

Device Type 01

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1Y	8	3A
2	1A	9	3B
3	1B	10	3Y
4	2Y	11	4A
5	2A	12	4B
6	2B	13	4Y
7	GND	14	V_{CC}

FIGURE 4. Terminal connections.



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
4. The outputs are measured one at a time with one input transition per measurement.
5. All parameters and waveforms are not applicable to all devices.
6. For 3-state and Open Drain outputs tests: t_{PLH}/t_{PHL} S1 = Open; t_{PLZ}/t_{PZL} S1 = V_{CC}; t_{PHZ}/t_{PZH} S1 = GND; Open Drain S1 = V_{CC}

FIGURE 5. Timing waveforms and test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03645-01XE	01295	SN74AHC02MPWREP	AHC02EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243