

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual, micropower voltage comparator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/03643</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TLC3702-EP	Dual, micropower voltage comparator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MS-012	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V to 18 V 2/
Differential input voltage	± 18 V 3/
Input voltage range (V_I)	-0.3 V to V_{DD}
Output voltage range (V_O)	-0.3 V to V_{DD}
Input current (I_I)	± 5 mA
Output current (I_O) (each output)	± 20 mA
Total supply current into V_{DD}	40 mA
Total current out of ground	40 mA
Continuous total power dissipation (P_D)	See 1.5 dissipation rating table
Storage temperature range	-65°C to +150°C
Lead temperature, 1.6 mm (1/16 inch) from case for 10 seconds	+260°C

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{DD})	4 V minimum to 16 V maximum
Common mode input voltage (V_{IC})	0 V minimum to $V_{DD} - 1.5$ V maximum
High level output current (I_{OH})	-20 mA maximum
Low level output current (I_{OL})	20 mA maximum
Operating free air temperature range (T_A)	-55°C to +125°C

1.5 Dissipation rating table. Ambient temperatures

Case outline	$T_A \leq 25^\circ\text{C}$ Power rating	Derating factor above $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ Power rating	$T_A = 85^\circ\text{C}$ Power rating	$T_A = 125^\circ\text{C}$ Power rating
X	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ All voltage values, except differential voltages, are with respect to network ground.
- 3/ Differential voltages are at the IN+ with respect to IN-.
- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} V _{DD} = 5 V unless otherwise specified	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V _{IO}	V _{DD} = 5 V to 10 V, ^{2/} V _{IC} = V _{ICR} min	25°C	01		5	mV
			-55°C to +125°C			10	
Input offset current	I _{IO}	V _{IC} = 2.5 V	25°C	01	1 typical		pA
			+125°C			15	nA
Input bias current	I _{IB}	V _{IC} = 2.5 V	25°C	01	5 typical		pA
			+125°C			30	nA
Common mode input voltage range	V _{ICR}		25°C	01	0 to V _{DD} - 1		V
			-55°C to +125°C		0 to V _{DD} - 1.5		
Common mode rejection ratio	CMRR	V _{IC} = V _{ICR} min	25°C	01	84 typical		dB
			+125°C		83 typical		
			-55°C		82 typical		
Supply voltage rejection ratio	k _{SVR}	V _{DD} = 5 V to 10 V	25°C	01	85 typical		dB
			+125°C		85 typical		
			-55°C		82 typical		
High level output voltage	V _{OH}	V _{ID} = 1 V, I _{OH} = -4 mA	25°C	01	4.5		V
			+125°C		4.2		
Low level output voltage	V _{OL}	V _{ID} = -1 V, I _{OH} = -4 mA	25°C	01		300	mV
			+125°C			500	
Supply current (both comparators)	I _{DD}	Outputs low, no load	25°C	01		40	μA
			-55°C to +125°C			90	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions ^{1/} V _{DD} = 5 V unless otherwise specified	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Propagation delay time, low-to-high level output ^{3/}	t _{PLH}	Overdrive = 2 mV, f = 10 kHz, C _L = 50 pF	25°C	01	4.5 typical		μs
		Overdrive = 5 mV, f = 10 kHz, C _L = 50 pF			2.7 typical		
		Overdrive = 10 mV, f = 10 kHz, C _L = 50 pF			1.9 typical		
		Overdrive = 20 mV, f = 10 kHz, C _L = 50 pF			1.4 typical		
		Overdrive = 40 mV, f = 10 kHz, C _L = 50 pF			1.1 typical		
Propagation delay time, high-to-low level output ^{3/}	t _{PHL}	V _I = 1.4 V step at IN+	25°C	01	1.1 typical		μs
		Overdrive = 2 mV, f = 10 kHz, C _L = 50 pF			4 typical		
		Overdrive = 5 mV, f = 10 kHz, C _L = 50 pF			2.3 typical		
		Overdrive = 10 mV, f = 10 kHz, C _L = 50 pF			1.5 typical		
		Overdrive = 20 mV, f = 10 kHz, C _L = 50 pF			0.95 typical		
		Overdrive = 40 mV, f = 10 kHz, C _L = 50 pF			0.65 typical		
		V _I = 1.4 V step at IN+			0.15 typical		
Fall time	t _f	Overdrive = 50 mV, f = 10 kHz, C _L = 50 pF	25°C	01	50 typical		ns
Rise time	t _r	Overdrive = 50 mV, f = 10 kHz, C _L = 50 pF	25°C	01	125 typical		ns

^{1/} All characteristics are measured with zero common-mode voltage unless otherwise noted.

^{2/} The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

^{3/} Simultaneous switching of inputs causes degradation in output response.

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Case X

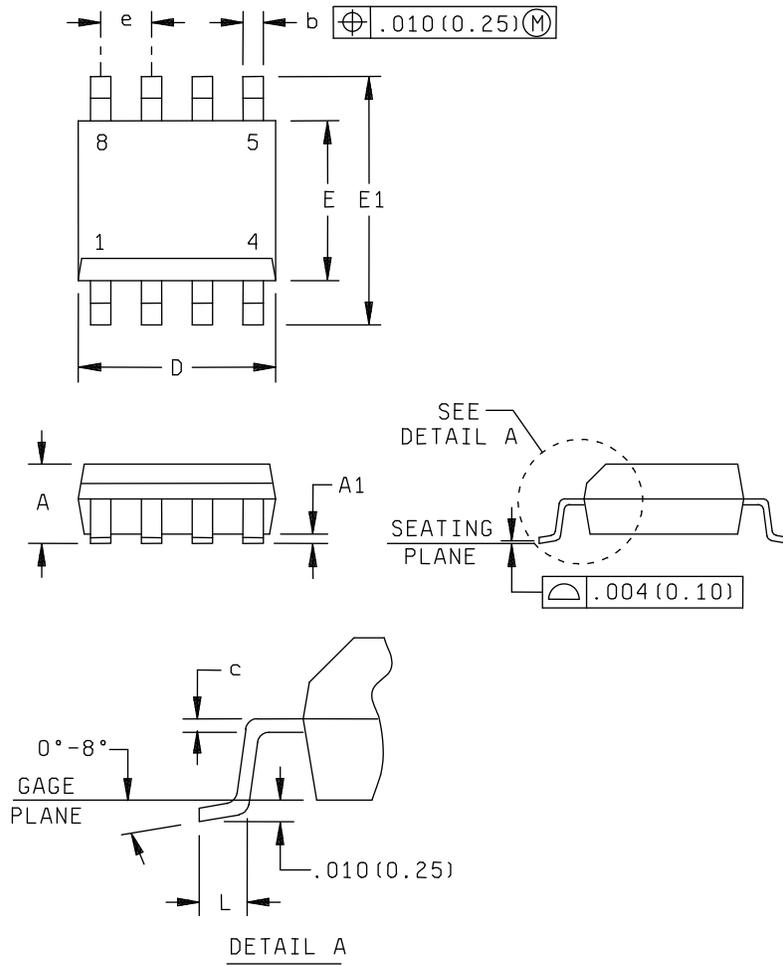


FIGURE 1. Case outline.

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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.014	0.020	0.35	0.51
c	0.008 nominal		0.20 nominal	
D	0.189	0.197	4.80	5.00
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.81	4.00
E1	0.228	0.244	5.80	6.20
L	0.016	0.044	0.40	1.12
n	8 leads		8 leads	

NOTE:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls within reference to JEDEC MS-012.

FIGURE 1. Case outline. – continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	1 OUT
2	1 IN-
3	1 IN+
4	GND
5	2 IN+
6	2 IN-
7	2 OUT
8	V _{DD}

FIGURE 2. Terminal connections.

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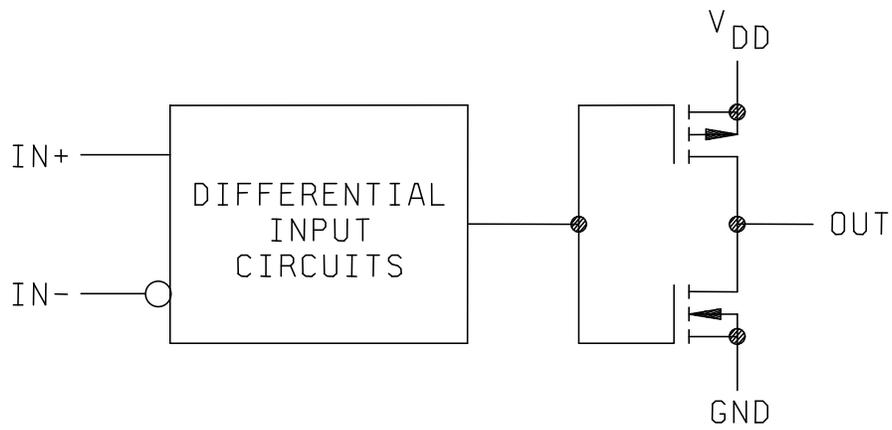
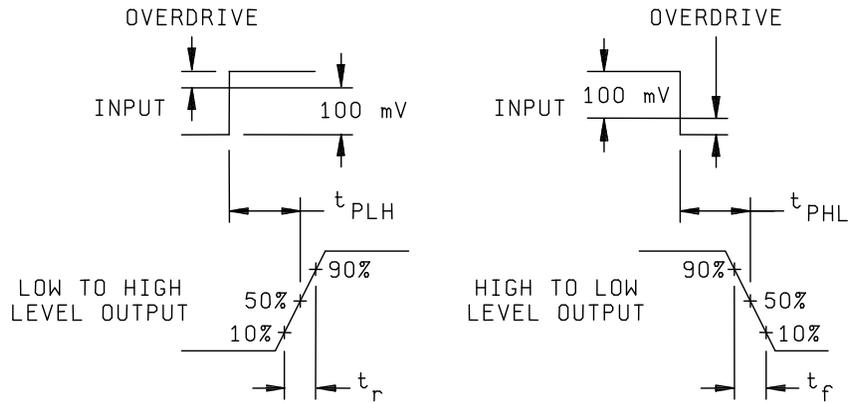
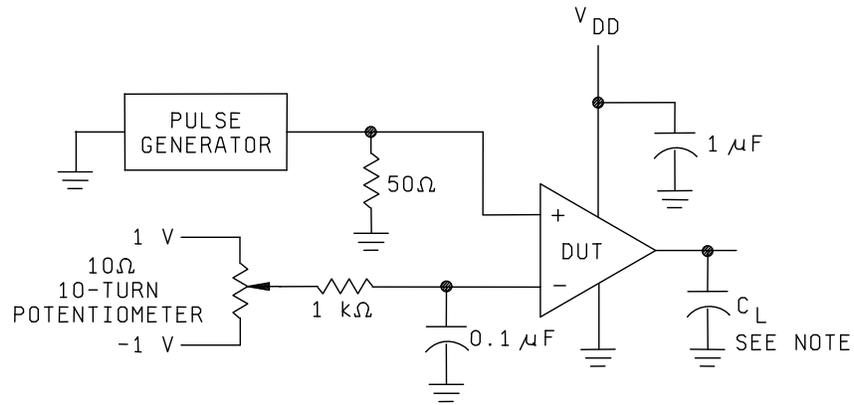


FIGURE 3. Block diagram.

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NOTE: C_L includes probe and jig capacitance.

FIGURE 4. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Package	Top side marking	Vendor part number
V62/03643-01XE	01295	Tape and reel	3702ME	TLC3702MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at www.ti.com/sc/package.

<u>CAGE code</u>	<u>Source of supply</u>
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

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