

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	09-02-25	Charles F. Saffle

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A								
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PMIC N/A	PREPARED BY Phu H. Nguyen	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD 03-09-03	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, DIGITAL, CONFIGURABLE MULTIPLE FUNCTION GATE, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/03641
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a configurable multiple-function gate, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/03641</u> Drawing number	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s). 1/

<u>Device</u>	<u>Generic number</u>	<u>Circuit function</u>
01	SN74LVC1G98-EP	Configurable multiple-function gate

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	6	JEDEC MO-203	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to these devices.

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1.3 Absolute maximum ratings. 2/

Supply voltage range, (V_{CC})	-0.5 V to +6.5 V
Input voltage range, (V_I)	-0.5 V to +6.5 V 3/
Voltage range applied to any output in the high-impedance or power-off state, (V_O)	-0.5 V to +6.5 V 3/
Voltage range applied to any output in the high or low state, (V_O)	-0.5 V to +6.5 V 3/ 4/
Input clamp current, (I_{IK}) ($V_I < 0$)	-50 mA
Output clamp current, (I_{OK}) ($V_O < 0$)	-50 mA
Continuous output current, (I_O)	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, (θ_{JA})	+259°C/W 5/
Storage temperature range, (T_{STG}).....	-65°C to +150°C

1.4 Recommended operating conditions. 6/ 7/

		Min	Max	Unit	
Supply voltage	V_{CC}	Operating	1.65	5.5	V
		Data retention only	1.5		
Input voltage	V_I	0	5.5	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	$V_{CC} = 1.65$ V		-4	mA
		$V_{CC} = 2.3$ V		-8	
		$V_{CC} = 3.0$ V		-16	
		$V_{CC} = 4.5$ V		-24	
Low level output current	I_{OL}	$V_{CC} = 1.65$ V		4	mA
		$V_{CC} = 2.3$ V		8	
		$V_{CC} = 3.0$ V		16	
		$V_{CC} = 4.5$ V		24	
Operating ambient temperature	T_A	-40	85	°C	

- 2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 3/ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 4/ The value of V_{CC} is provided in the recommended operating conditions table.
- 5/ The package terminal impedance is calculated in accordance with JESD 51-7.
- 6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 7/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the manufacturer application report, Implications of Slow or Floating CMOS inputs, literature number SCBA004.

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2. APPLICABLE DOCUMENTS

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.5.4 Logic configuration. The logic configuration shall be as specified on figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as specified on figure 5.

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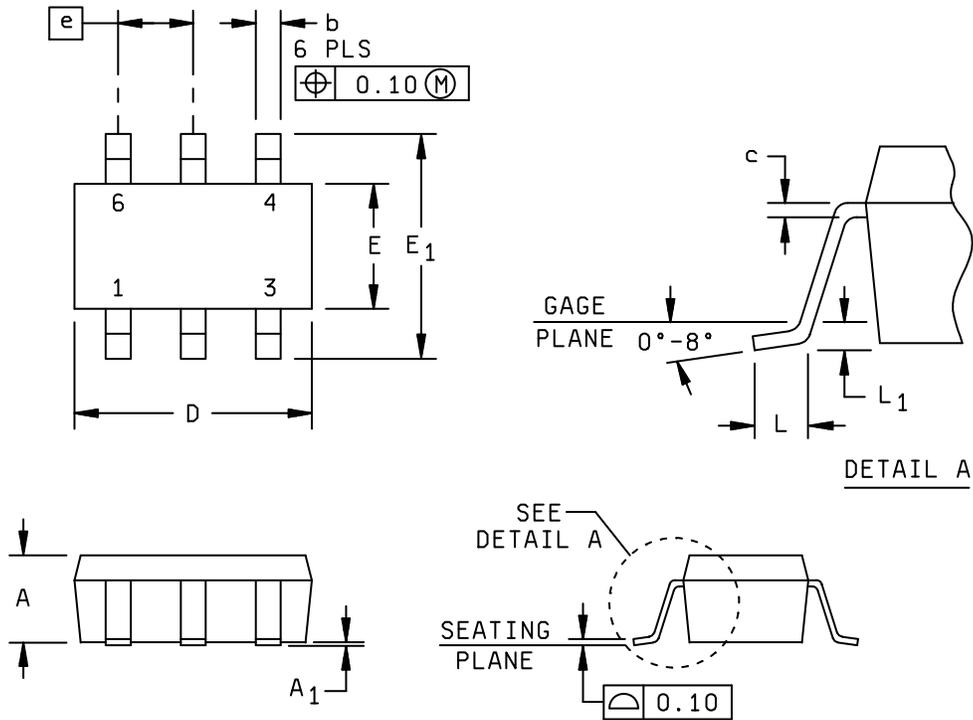
TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions -40°C ≤ T _A ≤ +85°C unless otherwise specified	V _{CC}	Limits		Unit
				Min	Max	
Positive-going input threshold voltage	V _{T+}		1.65 V	0.79	1.16	V
			2.3 V	1.11	1.56	
			3.0 V	1.50	1.87	
			4.5 V	2.16	2.74	
			5.5 V	2.61	3.33	
Negative-going input threshold voltage	V _{T-}		1.65 V	0.39	0.62	V
			2.3 V	0.58	0.87	
			3.0 V	0.84	1.14	
			4.5 V	1.41	1.79	
			5.5 V	1.87	2.29	
Hysteresis (V _{T+} - V _{T-})	ΔV _T		1.65 V	0.37	0.62	V
			2.3 V	0.48	0.77	
			3.0 V	0.56	0.87	
			4.5 V	0.71	1.04	
			5.5 V	0.71	1.11	
High level output voltage	V _{OH}	I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.1		V
		I _{OH} = -4 mA	1.65 V	1.2		
		I _{OH} = -8 mA	2.3 V	1.9		
		I _{OH} = -16 mA	3.0 V	2.4		
		I _{OH} = -24 mA		2.3		
		I _{OH} = -32 mA	4.5 V	3.8		
Low level output voltage	V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V		0.1	V
		I _{OL} = 4 mA	1.65 V		0.45	
		I _{OL} = 8 mA	2.3 V		0.3	
		I _{OL} = 16 mA	3.0 V		0.4	
		I _{OL} = 24 mA			0.55	
		I _{OL} = 32 mA	4.5 V		0.55	
Input current	I _I	V _I = 5.5 V or GND	0 to 5.5 V		±5	μA
Off-state leakage current	I _{off}	V _I or V _O = 5.5 V	0		±10	μA
Quiescent supply current	I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V		10	μA
Quiescent supply current delta	Δ I _{CC}	One input at V _{CC} - 0.6, Other inputs at V _{CC} or GND	3.0 V to 5.5 V		500	μA
Input capacitance	C _i	V _I = V _{CC} or GND, T _A = 25°C	3.3 V	3.5 TYP		pF
From any input to output Y	t _{pd}		1.8 V ±0.15 V	3.2	14.4	ns
			2.5 V ±0.20 V	2.0	8.3	
			3.3 V ±0.30 V	1.5	6.3	
			5.0 V ±0.50 V	1.1	5.1	
Power dissipation capacitance	C _{pd}	f = 10 MHz, T _A = 25°C	1.8 V	23 TYP		pF
			2.5 V	23 TYP		
			3.3 V	23 TYP		
			5.0 V	26 TYP		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.10	E	1.10	1.40
A1	0.00	0.10	E1	1.80	2.40
b	0.15	0.30	e	0.65 TYP	
c	0.13 NOM		L	0.26	0.46
D	1.85	2.15	L1	0.15 TYP	

NOTES:

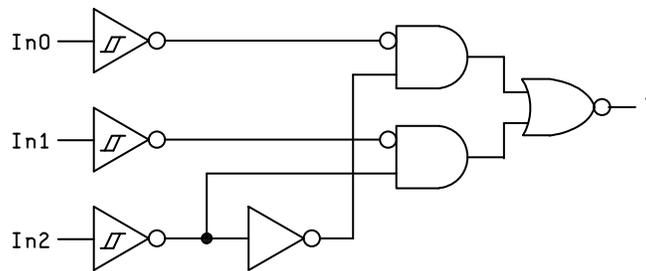
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusions.
4. Falls within JEDEC MS-203.

FIGURE 1. Case outline.

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Terminal number	Terminal symbol
1	In1
2	GND
3	In0
4	Y
5	V _{CC}
6	In2

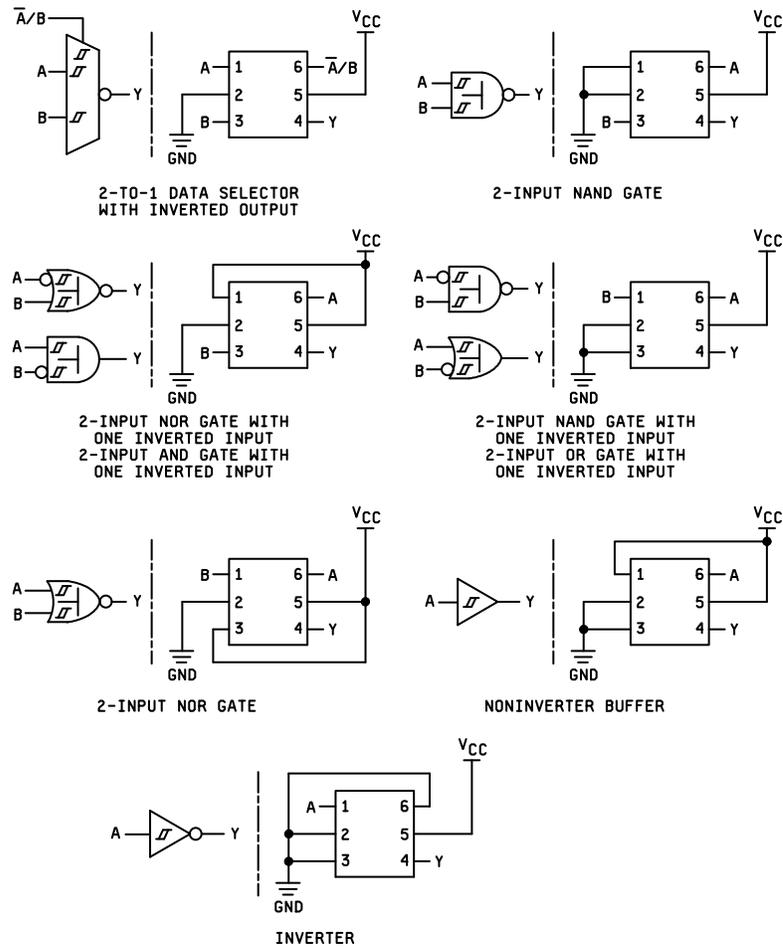
FIGURE 2. Terminal connections.



Function table			
Inputs			Output
In2	In1	In0	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

FIGURE 3. Logic diagram.

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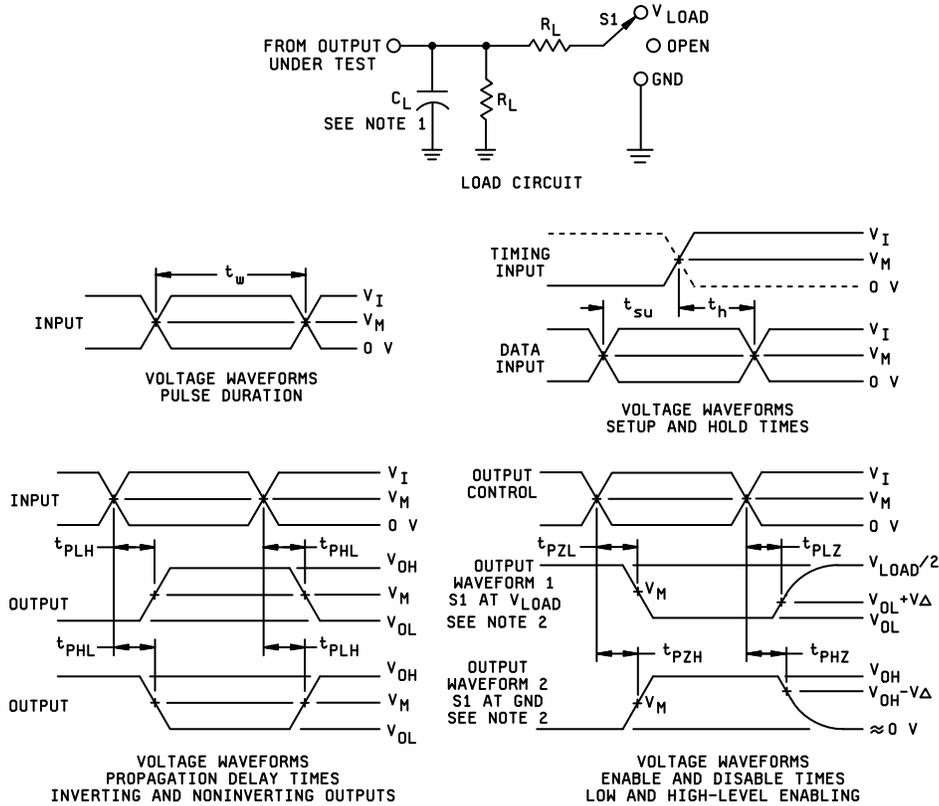
Logic Function
2-to-1 data selector with inverter output
2-input NAND gate
2-input NOR gate with one inverted input
2-input AND gate with one inverted input
2-input NAND gate with one inverted input
2-input OR gate with one inverted input
2-input NOR gate
Noninverted buffer
Inverter

FIGURE 4. Logic configuration.

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Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8 V \pm 0.15 V$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 V \pm 0.20 V$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3 V \pm 0.30 V$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5.0 V \pm 0.50 V$	V_{CC}	$\leq 2.5 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
4. The outputs are measured one at a time with one transaction per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
6. t_{PZL} and t_{PZH} are the same as t_{en} .
7. t_{PLH} and t_{PHL} are the same as t_{pd} .
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number <u>2/</u>	Top-side marking
V62/03641-01XE	01295	SN74LVC1G98IDCKREP	CWR

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ The package is available taped and reeled.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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