REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate paragraphs to current requirements. - PHN	09-11-09	Thomas M. Hess

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV	A	A	A	A	A	A	A	A	A	A												
PAGE	18	19	20	21	22	23	24	25	26	27												

REV STATUS OF PAGES																		
	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 03-11-06	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, 3.3 V CMOS FIRST-IN, FIRST-OUT MEMORIES, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/03639**
	REV A	**PAGE** 1 **OF** 27

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a 3.3 V CMOS first-in, first-out memories, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03639	01	X	E
Drawing number	Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

Device	Memory organization	Generic number	Circuit function
01	8192 x 18/ 16384 x 9	SN74V263	3.3 V CMOS first-in, first-out memories
02	16384 x 18/ 32768 x 9	SN74V273	3.3 V CMOS first-in, first-out memories
03	32768 x 18/ 65536 x 9	SN74V283	3.3 V CMOS first-in, first-out memories
04	65536 x 18/131072 x 9	SN74V293	3.3 V CMOS first-in, first-out memories

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	80	JEDEC MS-026	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes areas specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 2/

Terminal voltage range with respect to GND, (V_{TERM}) ..... -0.5 V to + 4.5 V
Continuous output current, (I_O) (V_O = 0 to V_{CC}) ..... ±50 mA
Storage temperature range, (T_{STG})..... -55°C to +125°C

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to these devices.
2/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

1.4 Recommended operating conditions. 3/ 4/

Supply voltage, (V_{CC}) ..... +3.15 V to +3.45 V 5/
Supply voltage, (GND) ..... 0.0 V
High level input voltage, (V_{IH}) ..... +2.0 V to 5.5 V 6/
Low level input voltage, (V_{IL}) ..... +0.8 V maximum
Operating case temperature, (T_C) ..... -55°C to +125°C 7/

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Block diagram. The block diagram shall be as specified on figure 3.

3.5.4 Load circuit. The load circuit shall be as specified on figure 4.

3.5.5 Timing waveforms. The timing waveforms shall be as specified on figure 5-21.

3/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturer information for additional information on enhanced plastic packaging.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ V_{CC} = 3.3 V ± 0.15 V, JESD8-A compliant.
6/ Outputs are not 5-V tolerant.
7/ For derating information, please refer to manufacturer information.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $3.15\ V \le V_{CC} \le 3.45\ V$ unless otherwise specified	Limits		Unit
			Min	Max	
High level output voltage	V_{OH}	I_{OH} = -2 mA	2.4		V
Low level output voltage	V_{OL}	I_{OL} = 8 mA		0.4	V
Input voltage	I_I	V_I = 0.4 V to V_{CC}		±1	µA
Off state output current	I_{OZ}	$\overline{OE} \ge V_{IH}$, V_O = 0.4 V to V_{CC}		±10	µA
Supply current	I_{CC1}	x9 input to x9 output 2/ 3/ 4/		30	mA
Supply current	I_{CC2}	X18 input to x18 output 2/ 3/ 4/		35	mA
Supply current	I_{CC3}	Stand by, 2/ 5/		15	mA
Input capacitance	C_{IN}	V_I = 0, T_C = +25°C, f = 1 MHz		10	pF
Output capacitance	C_{OUT}	V_O = 0, T_C = +25°C, f = 1 MHz Output deselected ($\overline{OE} \ge V_{IH}$)		10	pF
Clock cycle frequency	f_{CLOCK}	See figure 5 to 21 6/		133	MHz
Data access time	t_A		2	5	ns
Clock cycle time	t_{CLK}		7.5		ns
Clock high time	t_{CLKH}		3.5		ns
Clock low time	t_{CLKL}		3.5		ns
Data setup time	t_{DS}		2.5		ns
Data hold time	t_{DH}		0.5		ns
Enable set up time	t_{ENS}		2.5		ns
Enable hold time	t_{ENH}		0.5		ns
Load set up time	t_{LDS}		3.5		ns
Load hold time	t_{LDH}		0.5		ns
Reset pulse duration 7/	t_{RS}		10		ns
Reset setup time	t_{RSS}		15		ns
Reset recovery time	t_{RSR}		10		ns
Reset to flag and output time	t_{RSF}			15	ns
Retransmit setup time	t_{RTS}		3.5		ns
Output enable to output in low impedance	t_{OLZ}		0		ns
Output enable to output valid	t_{OE}		2	6	ns
Output enable to output in high impedance	t_{OHZ}		2	6	ns
Write clock to $\overline{FF}$ or $\overline{IR}$	t_{WFF}			5	ns
Read clock to $\overline{EF}$ or $\overline{OR}$	t_{REF}			5	ns
Clock to asynchronous programmable almost full flag	t_{PAFA}			12.5	ns
Write clock to synchronous programmable almost full flag	t_{PAFS}			5	ns
Clock to asynchronous programmable almost empty flag	t_{PAEA}			12.5	ns

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $3.15\ V \le V_{CC} \le 3.45\ V$ unless otherwise specified	Limits		Unit
			Min	Max	
Read clock to synchronous programmable almost empty flag	t_{PAES}	See figure 5 to 21 6/		5	ns
Clock to half full flag	t_{HF}			12.5	ns
Skew time between read clock and write clock for $\overline{EF}$ / $\overline{OR}$ and $\overline{FF}$ / $\overline{IR}$	t_{sk1}		5		ns
Skew time between read clock and write clock for $\overline{PAE}$ and $\overline{PAF}$	t_{sk2}		7		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ For derating information, please refer to manufacturer information.

3/ Tested with outputs open ($I_{OUT} = 0$)

4/ RCLK and WCLK switch at 20 MHz and data inputs switch at 10 MHz.

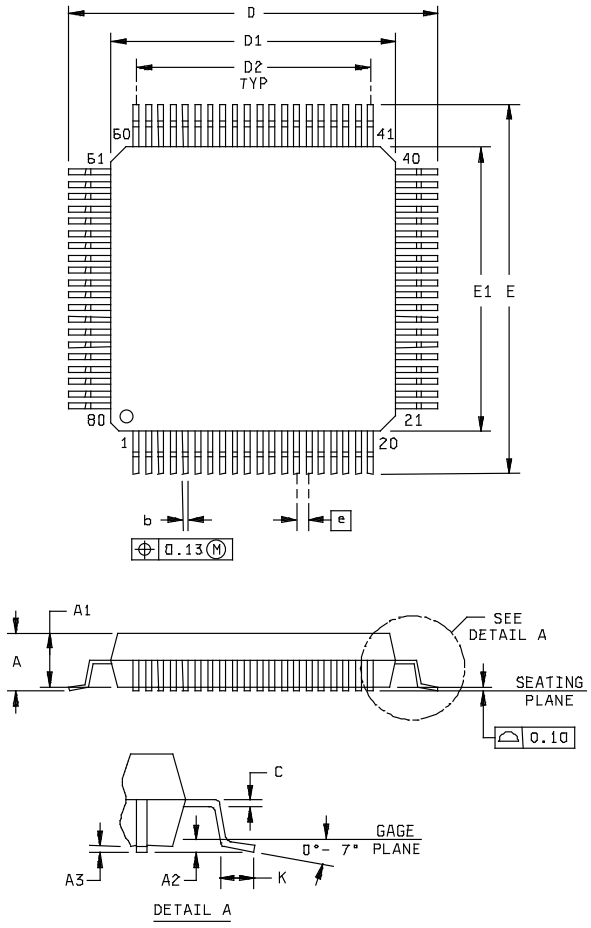
5/ For x18 bus widths, typical $I_{CC2} = 5 + f_S + 0.02 \times C_L \times f_S$ (in mA); for x9 bus widths, typical $I_{CC1} = 5 + 0.775\ f_S + 0.02 \times C_L \times f_S$ (in mA). These equations are valid under the following conditions:

$V_{CC} = 3.3$ V, $T_C = 25°C$, f_S = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at $f_S/2$, C_L = capacitive load (in pF).

6/ All AC timings apply to both FWFT mode and standard modes.

7/ Pulse durations less than minimum values are not allowed.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.60	D/E	15.80	16.20
A1	1.35	1.45	D1/E1	13.80	14.20
A2	0.25 TYP		D2	12.0 TYP	
A3	0.05		e	0.65 TYP	
b	0.22	0.38	K	0.45	0.75
c	0.13 NOM				

Notes:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MS-026.

FIGURE 1. Case outline.

Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name
1	$\overline{WEN}$	21	D7	41	Q7	61	$\overline{REN}$
2	$\overline{SEN}$	22	D6	42	Q8	62	RCLK
3	DNC	23	GND	43	Q9	63	RM
4	V_{CC}	24	D5	44	V_{CC}	64	$\overline{EF}$ / $\overline{OR}$
5	DNC	25	D4	45	Q10	65	PFM
6	IW	26	D3	46	GND	66	$\overline{PAE}$
7	GND	27	D2	47	Q11	67	V_{CC}
8	D17	28	D1	48	GND	68	IP
9	V_{CC}	29	D0	49	Q12	69	$\overline{BE}$
10	D16	30	GND	50	Q13	70	FSEL1
11	D15	31	Q0	51	V_{CC}	71	$\overline{HF}$
12	D14	32	Q1	52	Q14	72	FSEL0
13	D13	33	GND	53	Q15	73	OW
14	GND	34	Q2	54	GND	74	$\overline{PAF}$
15	D12	35	Q3	55	GND	75	$\overline{FF}$ / $\overline{IR}$
16	D11	36	V_{CC}	56	Q16	76	FWFFT/SI
17	D10	37	Q4	57	Q17	77	$\overline{LD}$
18	D9	38	Q5	58	V_{CC}	78	$\overline{MRS}$
19	D8	39	GND	59	$\overline{OE}$	79	$\overline{PRS}$
20	V_{CC}	40	Q6	60	$\overline{RT}$	80	WCLK

FIGURE 2. Terminal connections.

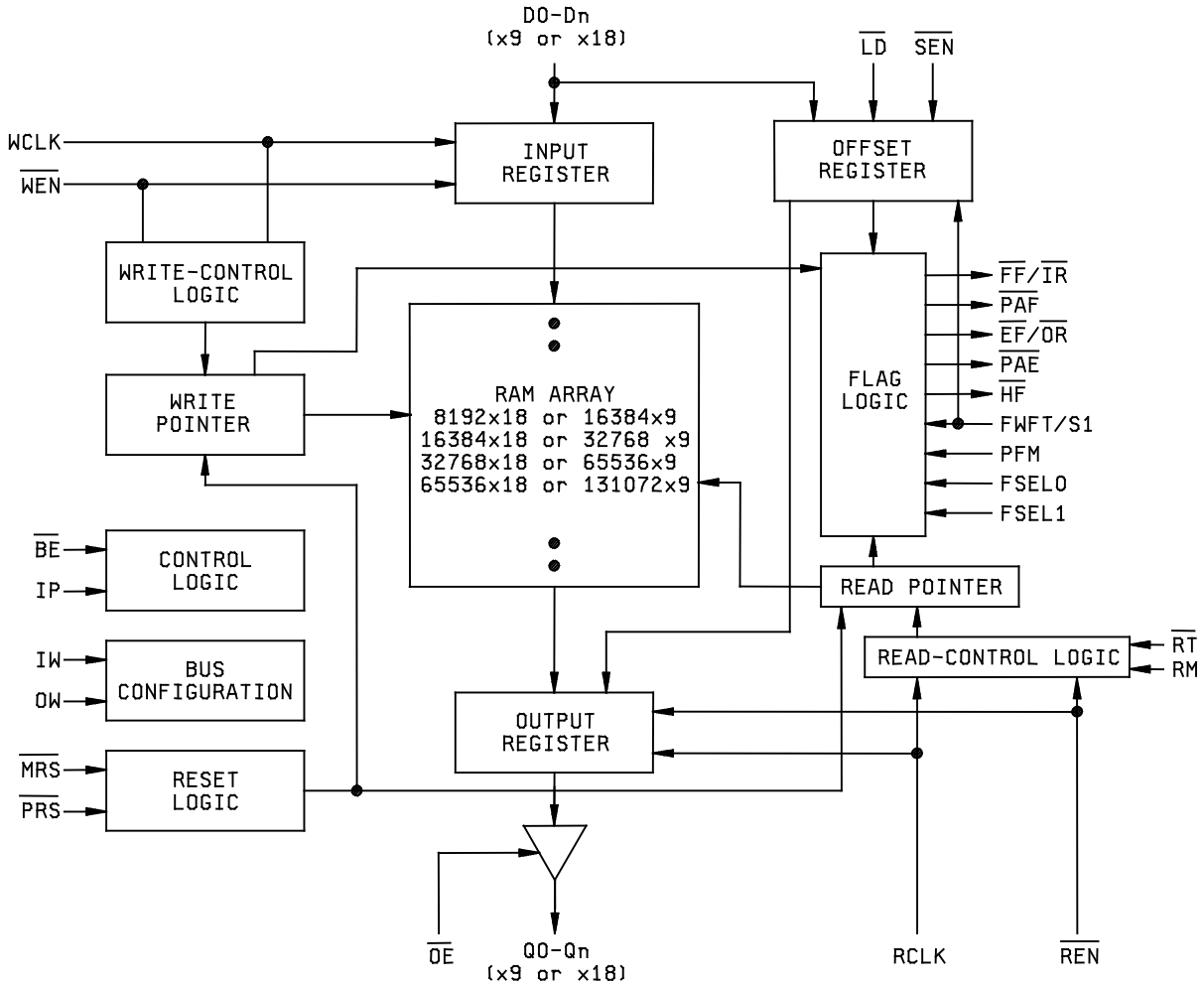
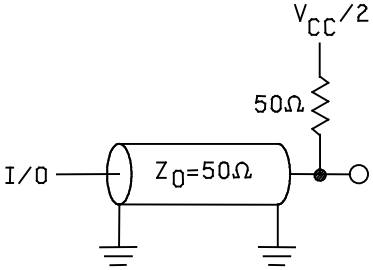
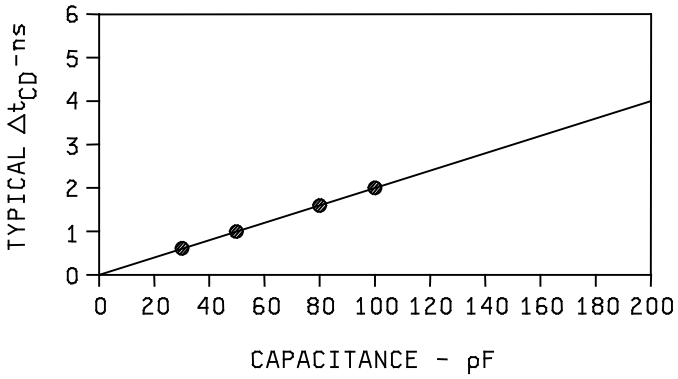


FIGURE 3. Block diagram.



A. AC TEST LOAD
FOR 7.5-SPEED GRADE



B. LUMPED CAPACITIVE LOAD, TYPICAL DERATING

AC test conditions

Input pulse levels	GND to 3.0 V
Input Rise/Fall time	3 ns 1/
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See A and B above

Notes:
1. For 133 MHz operation, input rise/fall times are 1.5 ns.
2. Includes probe and jig capacitance.

FIGURE 4. Load circuit.

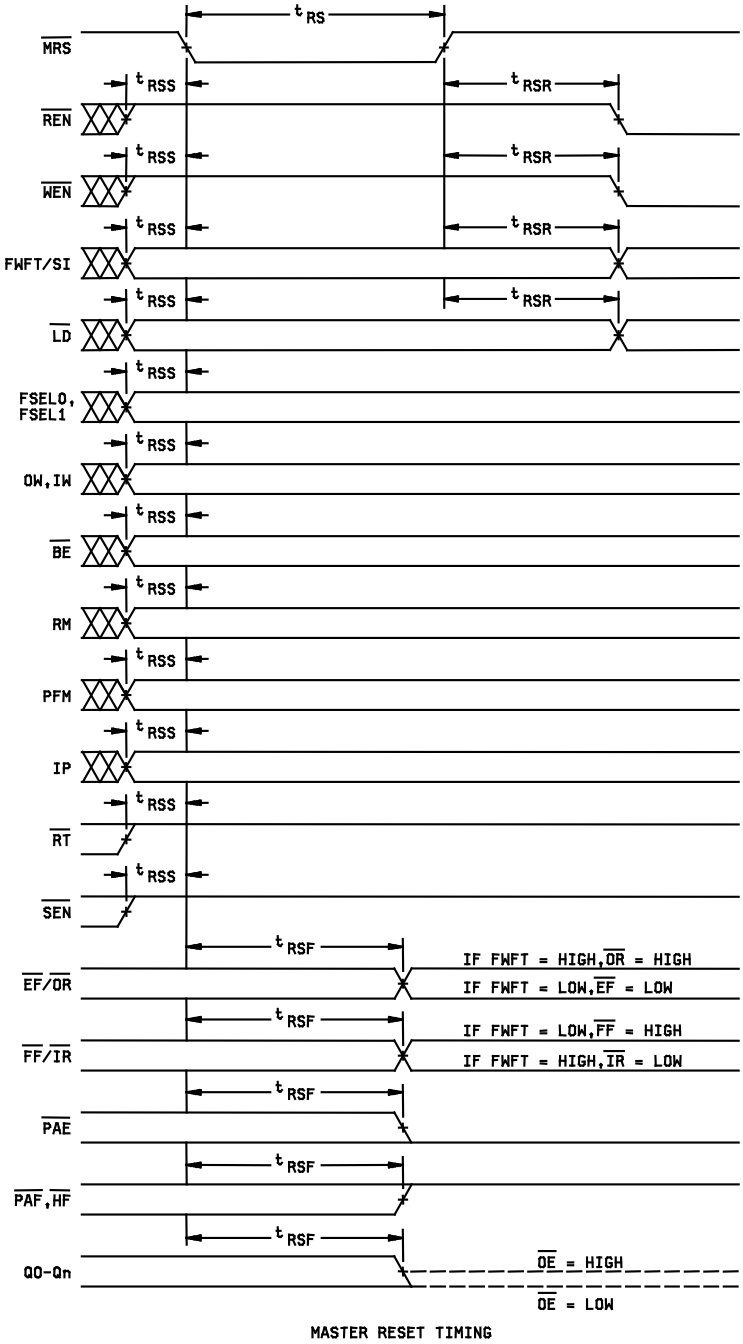


FIGURE 5. Timing waveforms.

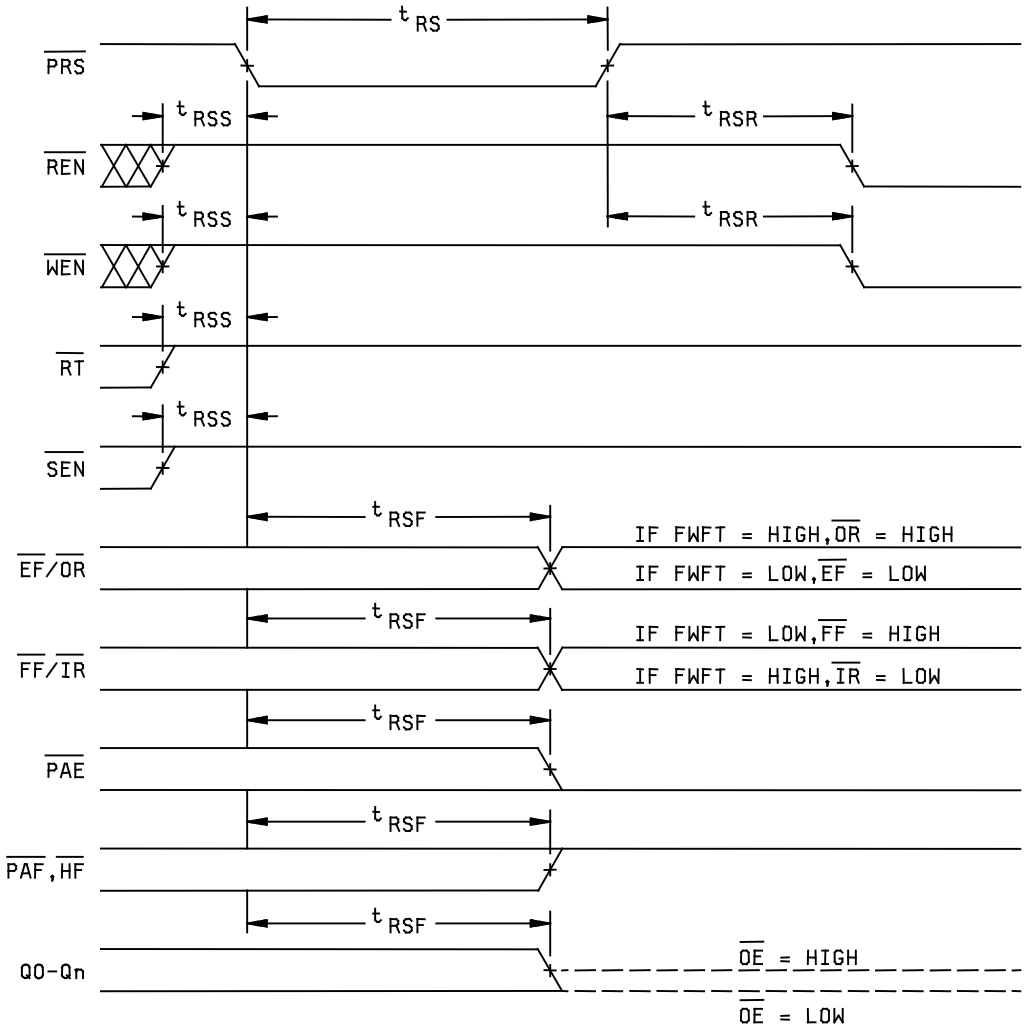
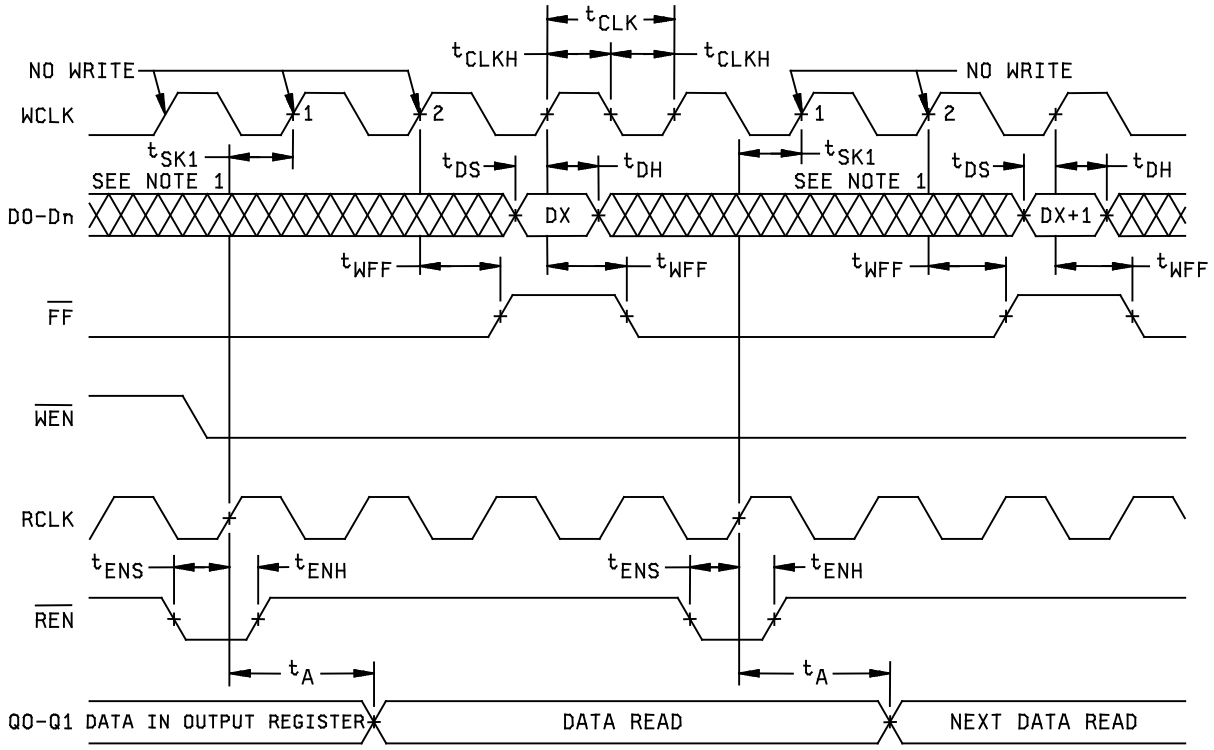


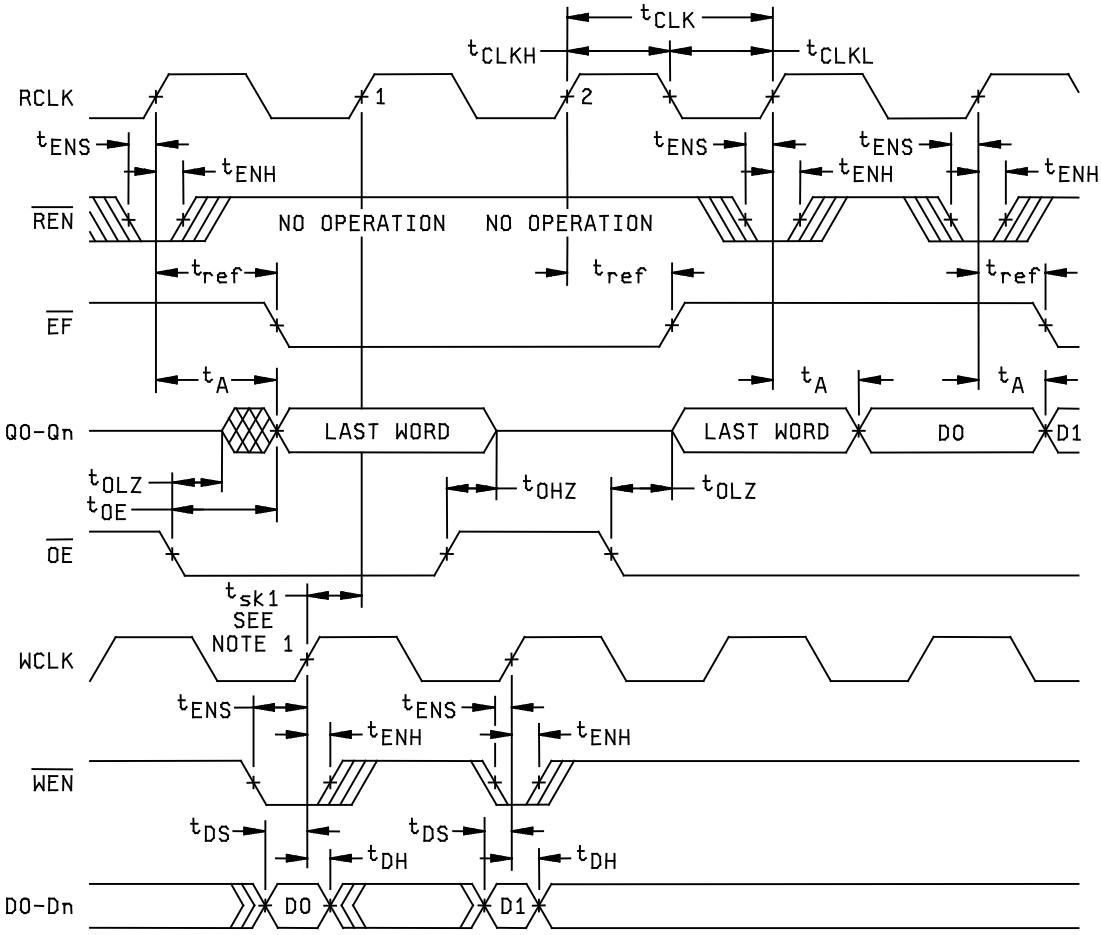
FIGURE 6. Timing waveforms.



Notes:

1. t_{sk1} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{FF}$ goes high (after one WCLK cycle + t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{sk1}, the $\overline{FF}$ deassertion can be delayed one additional WCLK cycle.
2. $\overline{LD}$ = high, $\overline{EF}$ = high.

FIGURE 7. Timing waveforms.

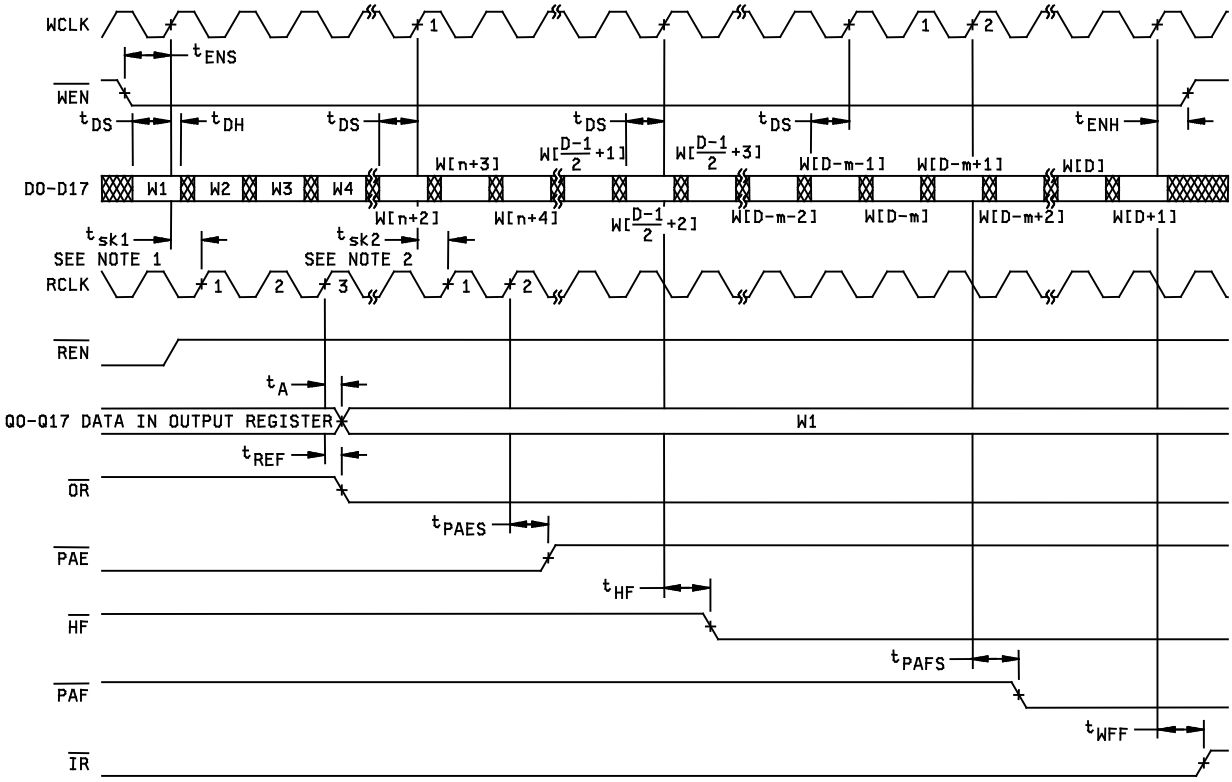


READ-CYCLE, EMPTY-FLAG,AND FIRST-DATA-WORD-LATENCY TIMING(STANDARD MODE)

Notes:

1. t_{sk1} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{EF}$ goes high (after one RCLK cycle + t_{ref}). If the time between the rising edge of WCLK and the rising edge of the RCLK is less than t_{sk1}, the $\overline{EF}$ deassertion can be delayed one additional WCLK cycle.
2. $\overline{LD}$ = high.
3. First data word latency: tsk1 + 1*t_{RCLK} + t_{REF}

FIGURE 8. Timing waveforms.

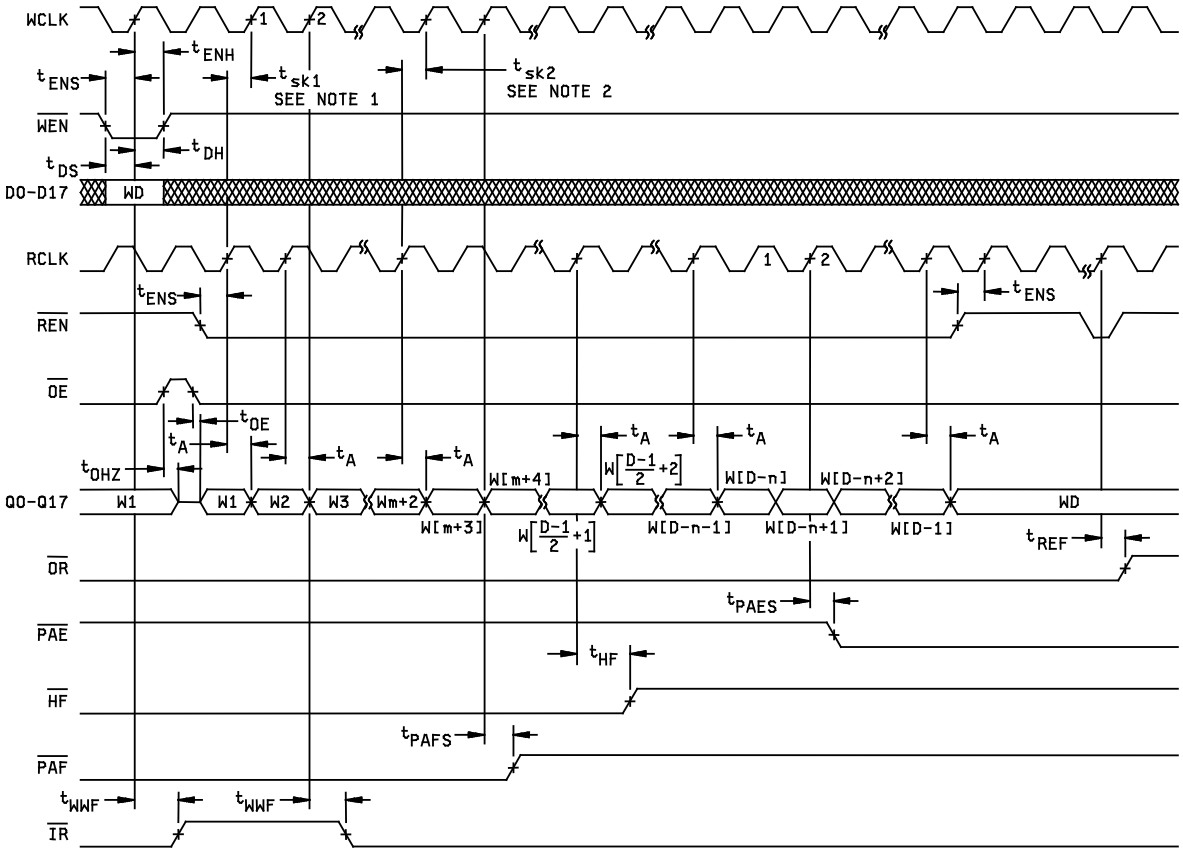


WRITE-CYCLE AND FIRST-DATA-WORD-LATENCY TIMING(FWFT MODE)

Notes:

1. t_{sk1} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{OR}$ goes low after two RCLK cycle + t_{REF}. If the time between the rising edge of WCLK and the rising edge of the RCLK is less than t_{sk1}, the $\overline{OR}$ deassertion might be delayed one additional RCLK cycle.
2. t_{sk2} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{PAE}$ goes high after one RCLK cycle + t_{PAES}. If the time between the rising edge of WCLK and the rising edge of the RCLK is less than t_{sk2}, $\overline{PAE}$ deassertion might be delayed one additional RCLK cycle.
3. $\overline{LD}$ = high., $\overline{OE}$ = low.
4. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset, D = maximum FIFO depth.
5. if x18 input or x18 output bus width is selected, D = 8193 for the SN74V263, D = 16385 for the SN74V273, D = 32769 for the SN74V283, and D = 65537 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16385 for the SN74V263, D = 32769 for the SN74V273, D = 65537 for the SN74V283, and D = 131073 for the SN74V293.
6. First data word latency: t_{sk1} + 2* t_{RCLK} = t_{REF}.

FIGURE 9. Timing waveforms.

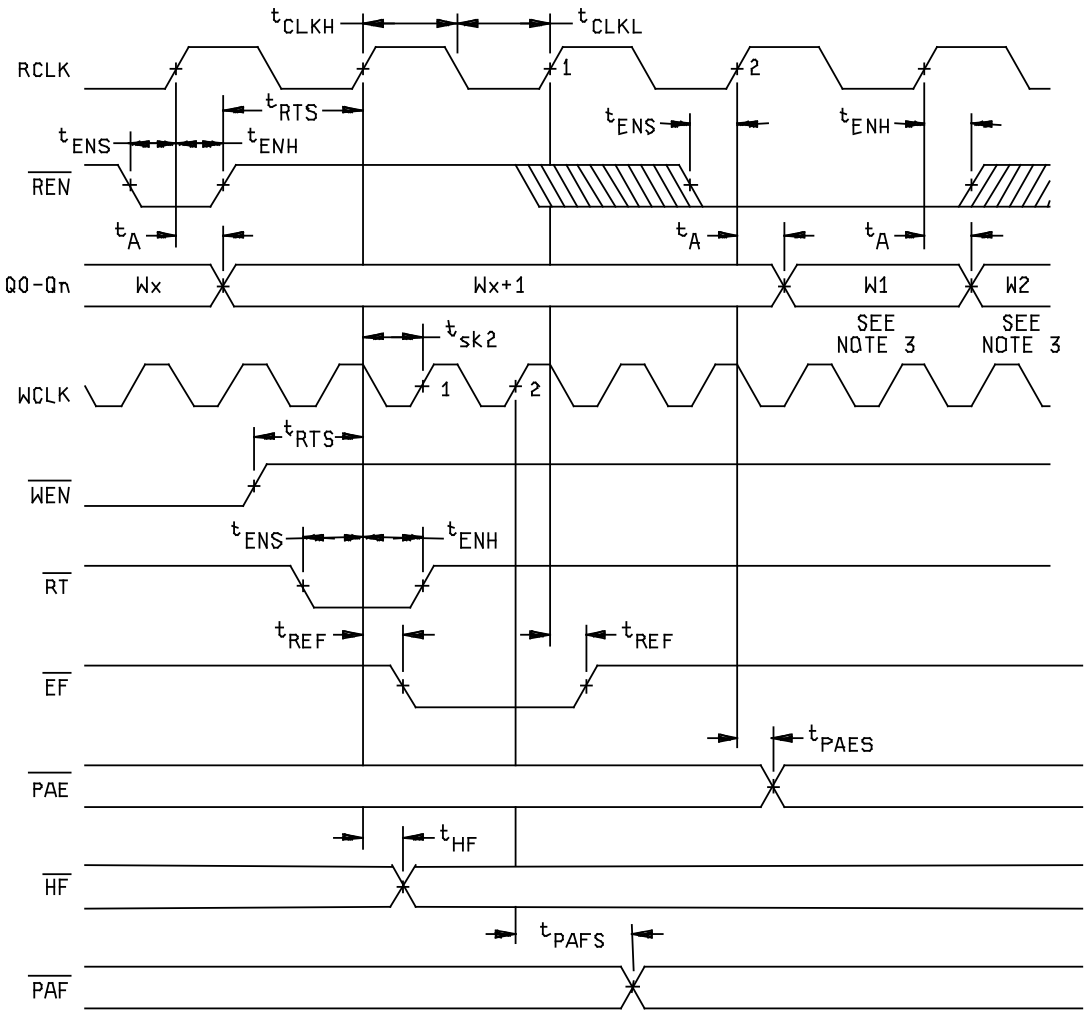


READ TIMING (FIRST-WORD FALL-THROUGH MODE)

Notes:

1. t_{sk1} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{IR}$ goes low after one WCLK cycle + t_{WFF}. If the time between the rising edge of RCLK and the rising edge of the WCLK is less than t_{sk1}, $\overline{IR}$ deassertion might be delayed an additional WCLK cycle.
2. t_{sk2} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{PAF}$ to go high after one WCLK cycle + t_{PAFS}. If the time between the rising edge of RCLK and the rising edge of the WCLK is less than t_{sk2}, $\overline{PAF}$ deassertion might be delayed one additional WCLK cycle.
3. $\overline{LD}$ = high.
4. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset, D = maximum FIFO depth.
5. if x18 input or x18 output bus width is selected, D = 8193 for the SN74V263, D = 16385 for the SN74V273, D = 32769 for the SN74V283, and D = 65537 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16385 for the SN74V263, D = 32769 for the SN74V273, D = 65537 for the SN74V283, and D = 131073 for the SN74V293.

FIGURE 10. Timing waveforms.

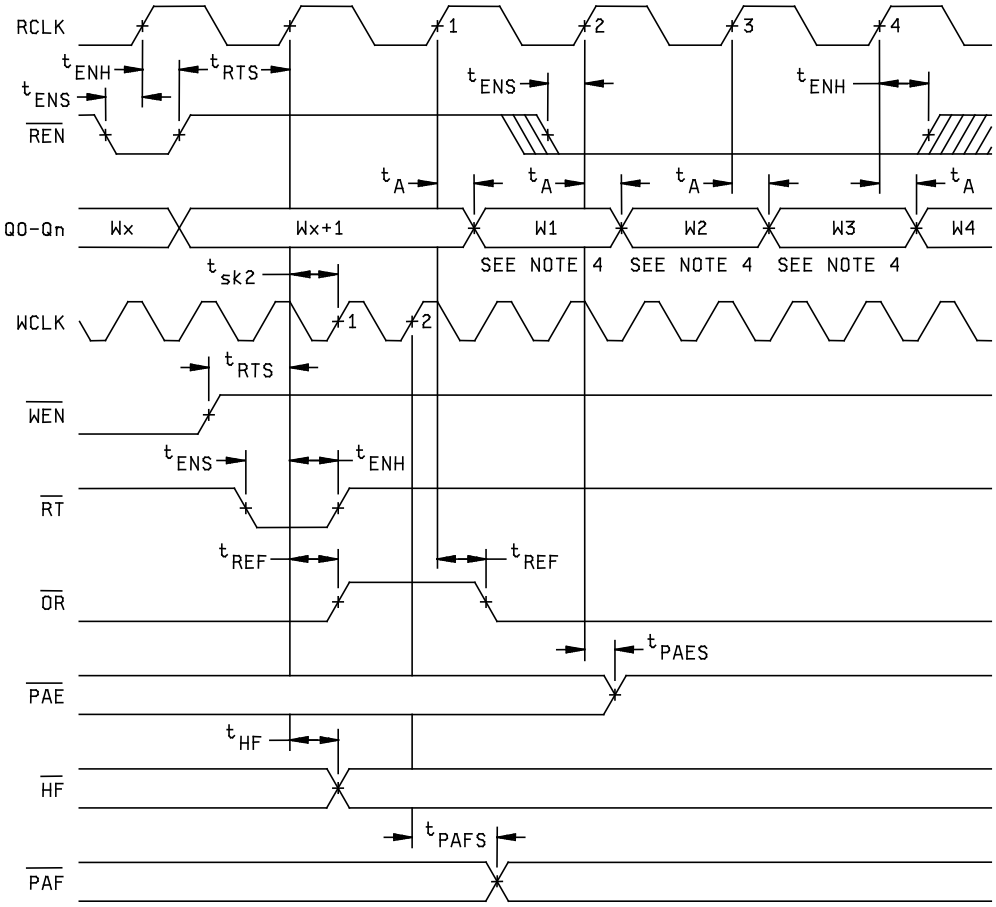


RETRANSMIT TIMING (STANDARD MODES)

Notes:

1. Retransmit setup is complete after $\overline{EF}$ returns high; only then can a read operation begin.
2. $\overline{OE}$ = low.
3. W1 = first word written to the FIFO after master reset, W2 = second word written to the FIFO after master reset.
4. No more than (D – 2) words may be written to the FIFO between reset (master or partial) and retransmit setup. Therefore, $\overline{FF}$ is high through the retransmit setup procedure. If x18 input or x18 output bus width is selected, D = 8192 for the SN74V263, D = 16384 for the SN74V273, D = 32768 for the SN74V283, and D = 65536 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16384 for the SN74V263, D = 32768 for the SN74V273, D = 65536 for the SN74V283, and D = 131072 for the SN74V293.
5. There must be at least two words written to and two words read from FIFO before a retransmit operation can be invoked.
6. RM is set high during $\overline{MRS}$.

FIGURE 11. Timing waveforms.

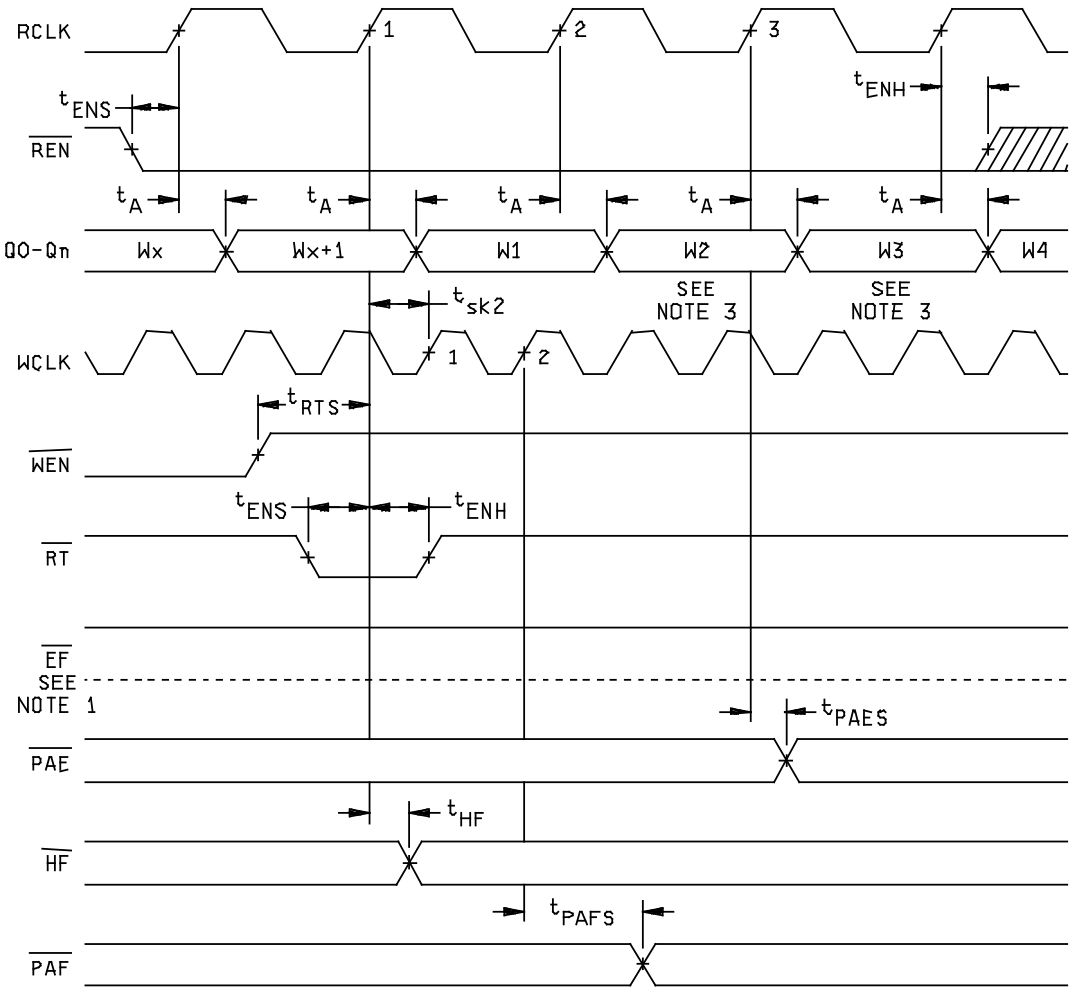


RETRANSMIT TIMING (FWFT MODE)

Notes:

1. Retransmit setup is complete after $\overline{OR}$ returns low.
2. No more than (D – 2) words may be written to the FIFO between reset (master or partial) and retransmit setup. Therefore, $\overline{IR}$ is low through the retransmit setup procedure. if x18 input or x18 output bus width is selected, D = 8193 for the SN74V263, D = 16385 for the SN74V273, D = 32769 for the SN74V283, and D = 65537 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16385 for the SN74V263, D = 32769 for the SN74V273, D = 65537 for the SN74V283, and D = 131073 for the SN74V293.
3. $\overline{OE}$ = low.
4. W1, W2, W3 = first, second, third words written to the FIFO after master reset.
5. There must be at lest two words written to the FIFO before a retransmit operation can be invoked.
6. RM is set high during $\overline{MRS}$.

FIGURE 12. Timing waveforms.

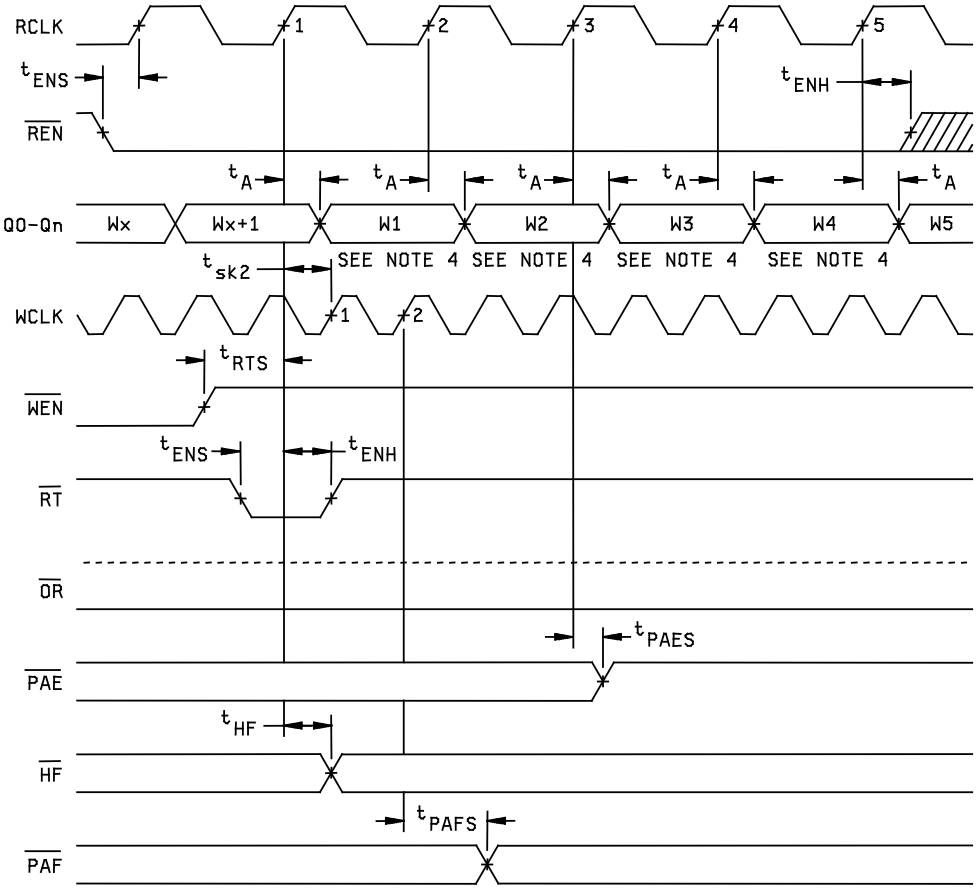


ZERO-LATENCY RETRANSMIT TIMING (STANDARD MODES)

Notes:

1. If the FIFO is empty at the point of retransmit, $\overline{EF}$ is updated based on RCLK (retransmit clock cycle). Valid data also appears on the output.
2. $\overline{OE}$ = low, enables data to be read on outputs Q0-Qn.
3. W_2 = second word written to the FIFO after master reset, W_3 = third word written to the FIFO after master reset.
4. No more than (D – 2) words may be written to the FIFO between reset (master or partial) and retransmit setup. Therefore, $\overline{FF}$ is high through the retransmit setup procedure. if x18 input or x18 output bus width is selected, D = 8192 for the SN74V263, D = 16384 for the SN74V273, D = 32768 for the SN74V283, and D = 65536 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16384 for the SN74V263, D = 32768 for the SN74V273, D = 65536 for the SN74V283, and D = 131072 for the SN74V293.
5. There must be at least two words written to and read from the FIFO before a retransmit operation can be invoked.
6. RM is set low during $\overline{MRS}$.

FIGURE 13. Timing waveforms.

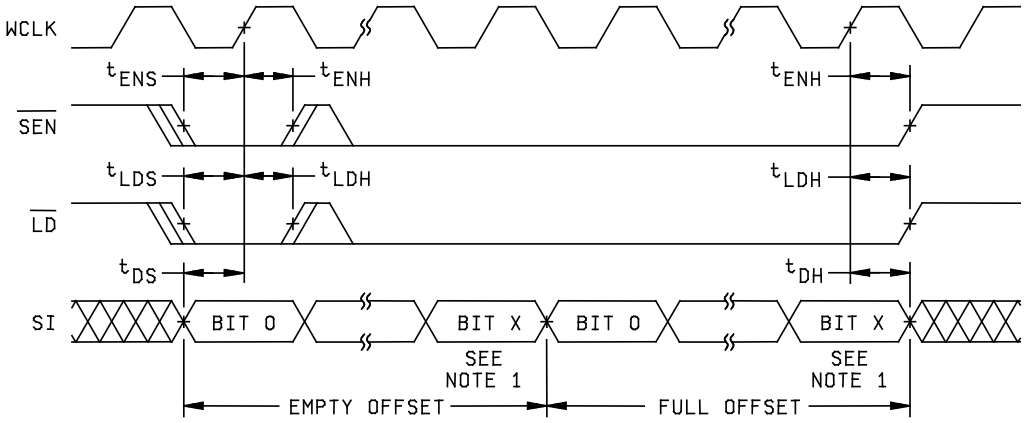


ZERO-LATENCY RETRANSMIT TIMING (FWFT MODE)

Notes:

1. If the part is empty at the point of retransmit, $\overline{OR}$ is updated based on RCLK (retransmit clock cycle). Valid data also appears on the output.
2. No more than (D – 2) words may be written to the FIFO between reset (master or partial) and retransmit setup. Therefore, $\overline{IR}$ is low through the retransmit setup procedure. if x18 input or x18 output bus width is selected, D = 8193 for the SN74V263, D = 16385 for the SN74V273, D = 32769 for the SN74V283, and D = 65537 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16385 for the SN74V263, D = 32769 for the SN74V273, D = 65537 for the SN74V283, and D = 131073 for the SN74V293.
3. $\overline{OR}$ = low.
4. W1, W2, W3 = first, second, and third words written to the FIFO after master reset.
5. There must be at least two words written to and read from the FIFO before a retransmit operation can be invoked
6. RM is set low during $\overline{MRS}$.

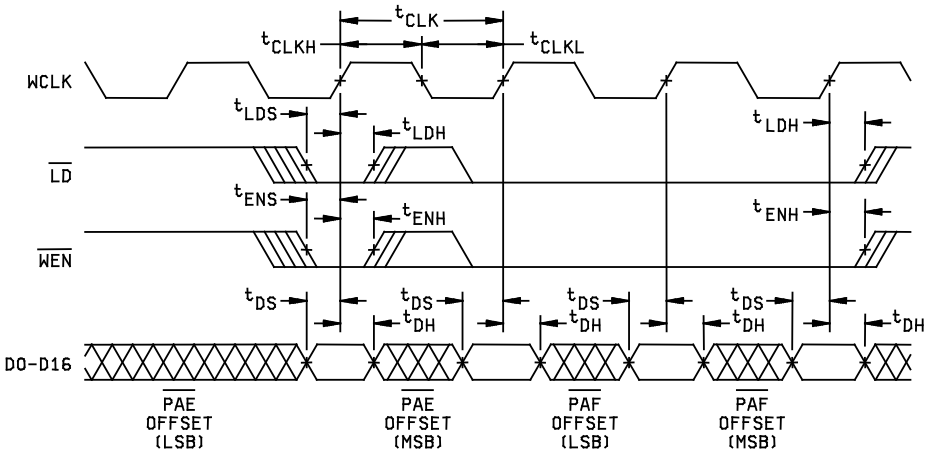
FIGURE 14. Timing waveforms.



SERIAL LOADING OF PROGRAMMABLE FLAG REGISTERS(FWFT AND STANDARD MODES)

Notes:

1. x9 to x9 mode: x = 13 for the SN74V263, x = 14 for the SN74V273, x = 15 for the SN74V283, and x = 16 for the SN74V293.
2. All other modes: x = 12 for the SN74V263, x = 13 for the SN74V273, x = 14 for the SN74V283, and x = 15 for the SN74V293.

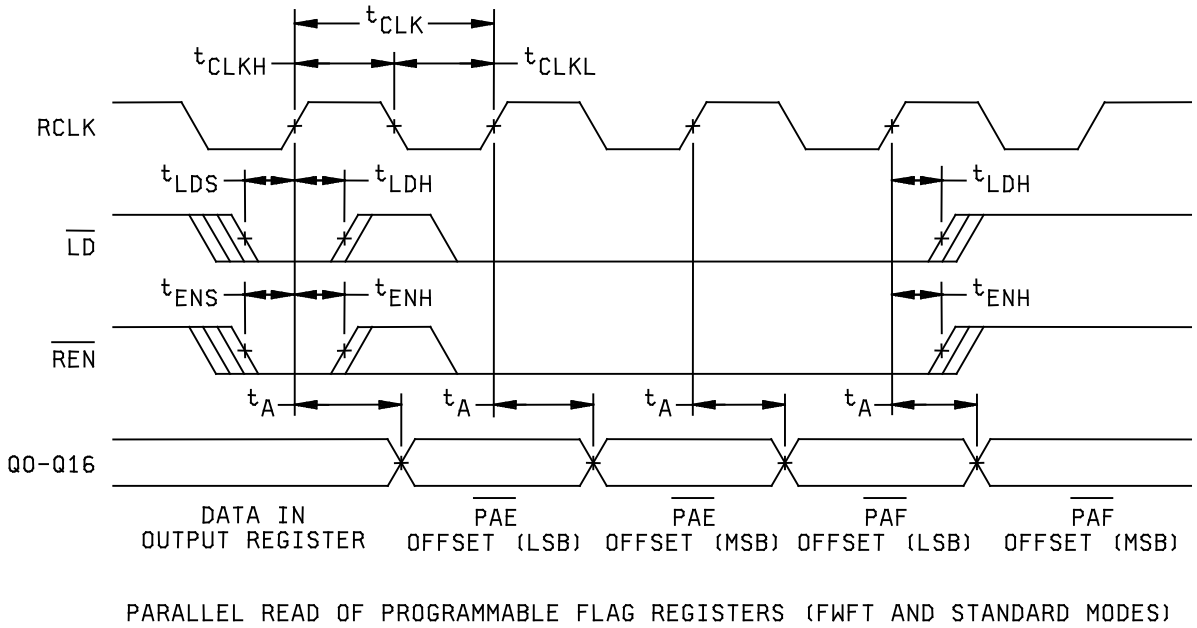


PARALLEL LOADING OF PROGRAMMABLE FLAG REGISTERS(FWFT AND STANDARD MODES)

Notes:

1. This diagram is based on programming the SN74V293x18 bus width. Add one cycle to both the $\overline{PAE}$ offset and $\overline{PAF}$ offset for x9 bus width.

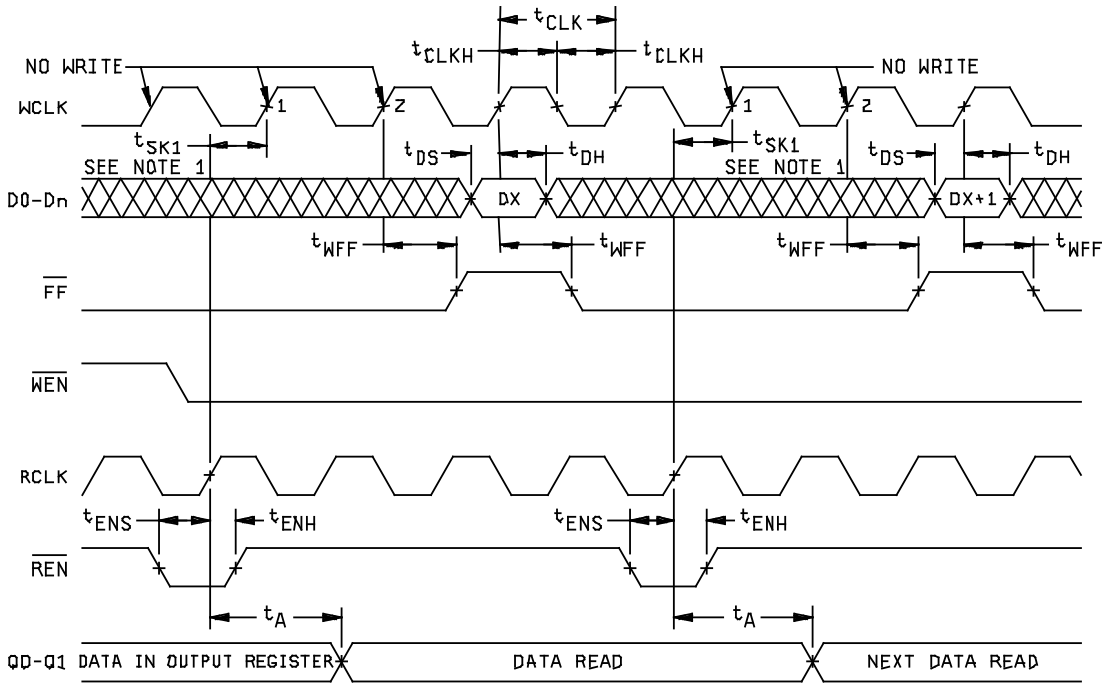
FIGURE 15. Timing waveforms.



Notes:

1. $\overline{OE}$ = low.
2. This diagram is based on programming the SN74V293x18 bus width. Add one cycle to both the $\overline{PAE}$ offset and $\overline{PAF}$ offset for x9 bus width.

FIGURE 16. Timing waveforms.

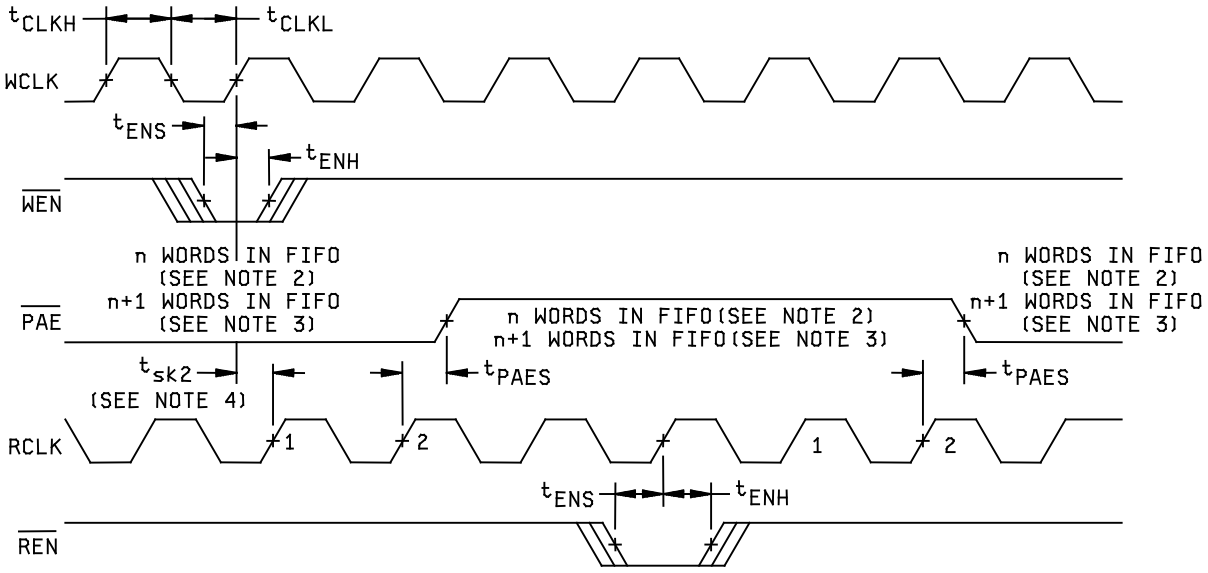


WRITE-CYCLE AND FULL-FLAG TIMING(STANDARD MODE)

Notes:

1. m = $\overline{PAF}$ offset
2. D = maximum FIFO depth.
   In FWFT mode: if x18 input or x18 output is selected, D = 8193 for the SN74V263, D = 16385 for the SN74V273, D = 32769 for the SN74V283, and D = 65537 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16385 for the SN74V263, D = 32769 for the SN74V273, D = 65537 for the SN74V283, and D = 131073 for the SN74V293.
   In standard mode: if x18 input or x18 output bus width is selected, D = 8192 for the SN74V263, D = 16384 for the SN74V273, D = 32768 for the SN74V283, and D = 65536 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16384 for the SN74V263, D = 32768 for the SN74V273, D = 65536 for the SN74V283, and D = 131072 for the SN74V293.
3. t_{sk2} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{PAF}$ goes high(after one WCLK cycle + t_{PAFS}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{sk2}, the $\overline{PAF}$ deassertion time may be delayed one additional WCLK cycle.
4. $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only.
5. Select this mode by setting PFM high during master reset.

FIGURE 17. Timing waveforms.

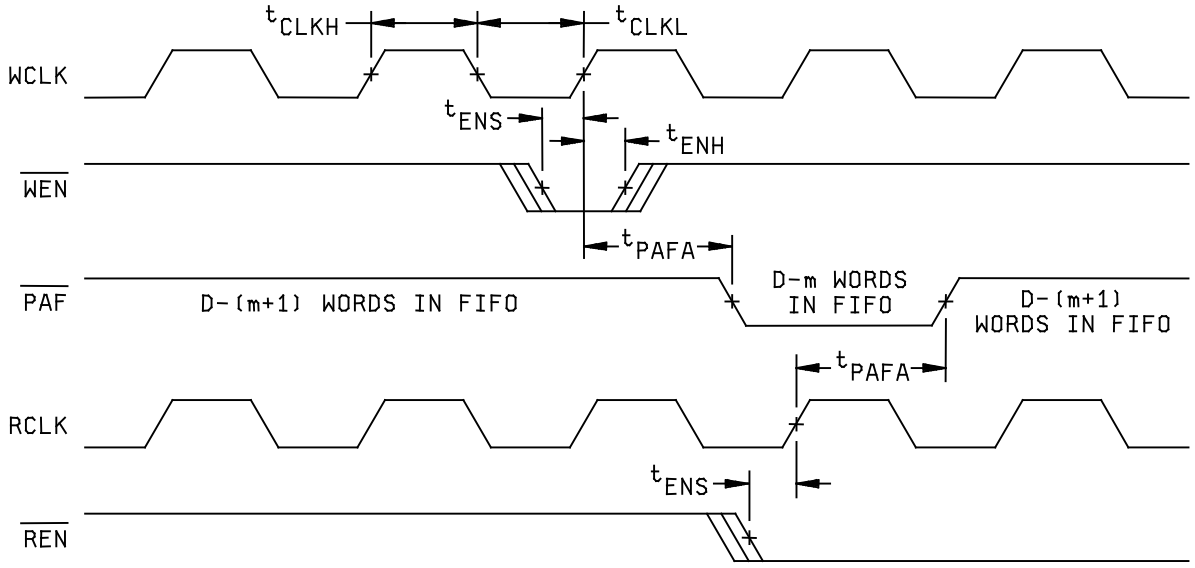


SYNCHRONOUS PROGRAMMABLE ALMOST-EMPTY FLAG TIMING(FWFT AND STANDARD MODE)

Notes:

1. n = $\overline{PAE}$ offset.
2. For standard mode.
3. For FWFT mode.
4. t_{sk2} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{PAE}$ goes high(after one RCLK cycle + t_{PAES}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{sk2}, the $\overline{PAE}$ deassertion time may be delayed one additional RCLK cycle.
5. $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only.
6. Select this mode by setting PFM high during master reset.

FIGURE 18. Timing waveforms.

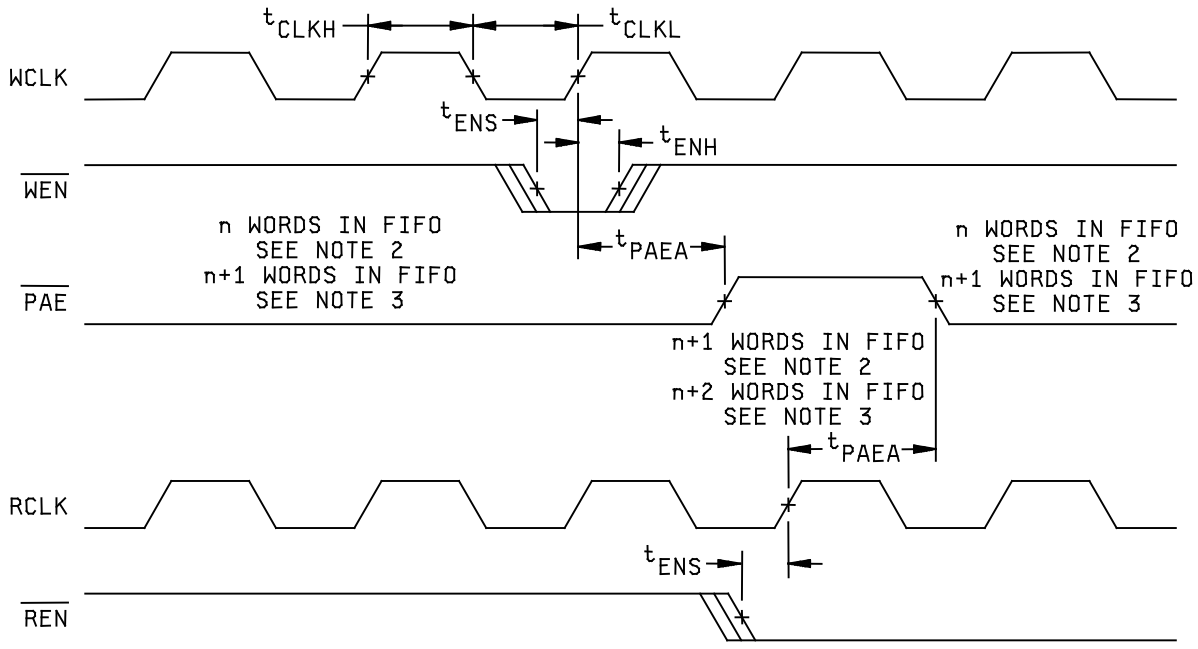


ASYNCHRONOUS PROGRAMMABLE ALMOST-FULL FLAG TIMING (FWFT AND STANDARD MODES)

Notes:

1. m = $\overline{PAF}$ offset
2. D = maximum FIFO depth.
   In FWFT mode: if x18 input or x18 output is selected, D = 8193 for the SN74V263, D = 16385 for the SN74V273, D = 32769 for the SN74V283, and D = 65537 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16385 for the SN74V263, D = 32769 for the SN74V273, D = 65537 for the SN74V283, and D = 131073 for the SN74V293.
   In standard mode: if x18 input or x18 output bus width is selected, D = 8192 for the SN74V263, D = 16384 for the SN74V273, D = 32768 for the SN74V283, and D = 65536 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16384 for the SN74V263, D = 32768 for the SN74V273, D = 65536 for the SN74V283, and D = 131072 for the SN74V293.
3. $\overline{PAF}$ is asserted to low on WCLK transition and reset to high on RCLK transaction.
4. Select this mode by setting PFM high during master reset.

FIGURE 19. Timing waveforms.

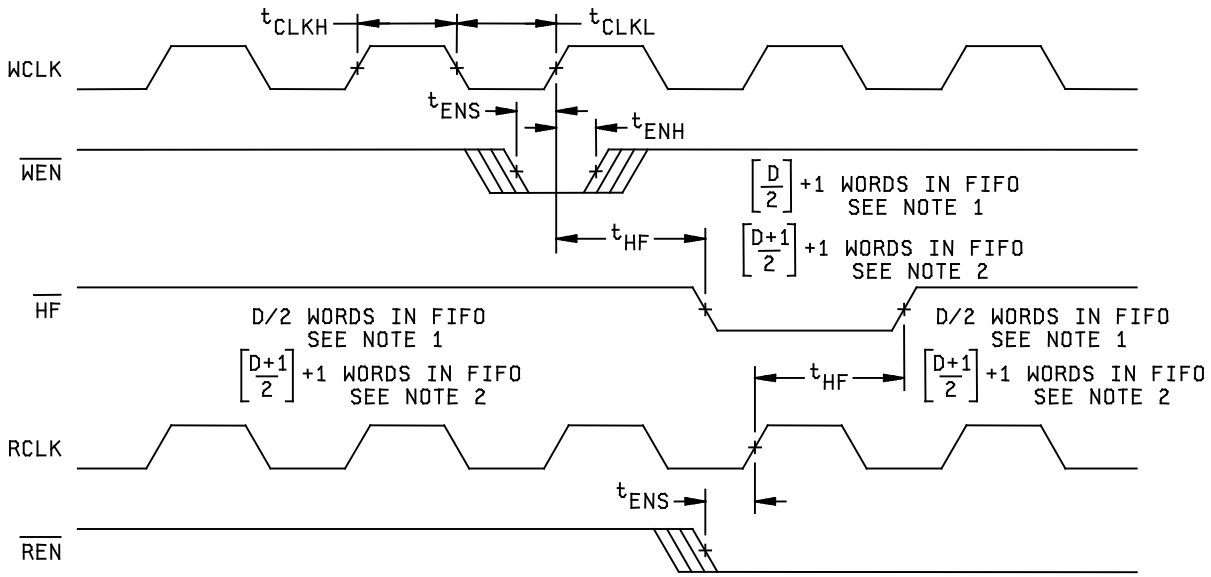


ASYNCHRONOUS PROGRAMMABLE ALMOST-EMPTY FLAG TIMING (FWFT AND STANDARD MODES)

Notes:

1. n = $\overline{PAE}$ offset.
2. For standard mode.
3. For FWFT mode.
4. $\overline{PAE}$ is asserted low on RCLK transition and reset to high on WCLK transition.
5. Select this mode by setting PFM low during master reset.

FIGURE 20. Timing waveforms.



HALF-FULL FLAG TIMING (FSFT AND STANDARD MODES)

Notes:

1. In standard mode: D = maximum FIFO depth. If x18 input or x18 output bus width is selected, D = 8192 for the SN74V263, D = 16384 for the SN74V273, D = 32768 for the SN74V283, and D = 65536 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16384 for the SN74V263, D = 32768 for the SN74V273, D = 65536 for the SN74V283, and D = 131072 for the SN74V293.
2. In FWFT mode: D = maximum FIFO depth. If x18 input or x18 output is selected, D = 8193 for the SN74V263, D = 16385 for the SN74V273, D = 32769 for the SN74V283, and D = 65537 for the SN74V293. If both x9 input and x9 output bus widths are selected, D = 16385 for the SN74V263, D = 32769 for the SN74V273, D = 65537 for the SN74V283, and D = 131073 for the SN74V293.

FIGURE 21. Timing waveforms.

4. QUALITY ASSURANCE PROVISIONS

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03639-01XE	01295	SN74V263PZAEP	V263EP
V62/03639-02XE	01295	SN74V273PZAEP	V273EP
V62/03639-03XE	01295	SN74V283PZAEP	V283EP
V62/03639-04XE	01295	SN74V293PZAEP	V293EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493