

1. SCOPE

1.1 Scope. This drawing documents the general requirements of an integrated 1394a-2000 OHCI PHY/link layer controller, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/03637</u> Drawing number	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
--	--	--	---

1.2.1 Device type(s).

<u>Device</u> 1/	<u>Generic</u>	<u>Circuit function</u>
01	TSB43AB21A-EP	Integrated 1394a-2000 OHCI PHY/Link-layer controller

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	128	JEDEC MO-136	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to these devices.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 2

1.3 Absolute maximum ratings. 1/

Supply voltage range:

REG18	-0.2 V to +2.2 V
AV _{DD}	-0.3 V to +4.0 V
DV _{DD}	-0.3 V to +4.0 V
PLL _{VDD}	-0.3 V to +4.0 V
V _{DDP}	-0.5 V to +5.5 V
Input voltage range for PCI, V _I , PHY, and miscellaneous	-0.5 V to V _{DD} +0.5 V
Output voltage range for PCI, V _O , PHY and miscellaneous	-0.5 V to V _{DD} +0.5 V
Input clamp current (I _{IK}) (V _I < 0 or V _I > V _{DD})	±20 mA 2/
Output clamp current (I _{OK}) (V _O < 0 or V _O > V _{DD})	±20 mA 3/
Electrostatic discharge	HBM: 2 kV, MM: 200 V 4/
Continuous total power dissipation	See dissipation rating table
Operating ambient temperature range (T _A): TSB43AB21AI	-40°C to +85°C
Storage temperature range (T _{STG})	-65°C to +150°C 5/
Lead temperature 1.6 mm (1/16 inch) from cage for 10 seconds	+260°C

Dissipation Rating Table

Case outline	T _A < 25°C Power rating	Derating Factor 7/ Above T _A = 25°C	T _A = 70°C Power Rating	T _A = 85°C Power Rating
X 6/	1.116W	0.013 W/°C	0.563 W	0.336 W
X 7/	0.967 W	0.009 W/°C	0.523 W	0.427 W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Applies to external input and bi-directional buffers. For 5-V tolerant use V_I > V_{DDI}. For PCI use V_I > V_{DDP}.

3/ Applies to external output and bi-directional buffers. For 5-V tolerant use V_O > V_{DDI}. For PCI use V_O > V_{DDP}.

4/HBM is human body model, MM is machine model.

5/ Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturers data for additional information on enhanced plastic packaging.

6/ Standard JEDEC high-K board.

7/ Standard JEDEC low-K board.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 3

1.4 Recommended operating conditions. 8/

		Test condition	Min	Max	Unit
REG 18			1.6	2.0	V
Core voltage, AV _{DD}			3.0	3.6	V
Core voltage, DV _{DD}			3.0	3.6	V
Core voltage, PLLV _{DD}			2.7	3.6	V
Output voltage, V _O	TTL and LVCMOS terminals		0	DV _{DD}	V
PCI I/O clamping voltage, V _{DDP}		V _{DDP} = 3.3 V	3.0	3.6	V
		V _{DDP} = 5.0 V	4.5	5.5	
High level input voltage, V _{IH} 9/	PCI	3.3 V	0.475 DV _{DD}	DV _{DD}	V
		5.0 V	2.0	V _{DDP}	
	PC(0-2)	0.7 DV _{DD}	DV _{DD}		
	$\overline{G_RST}$	0.6 DV _{DD}	DV _{DD}		
	Miscellaneous 10/		2.0	V _{DDP}	
Low level input voltage, V _{IL} 9/	PCI	3.3 V	0	0.325 DV _{DD}	V
		5.0 V	0	0.8	
	PC(0-2)	0	0.2 DV _{DD}		
	$\overline{G_RST}$	0	0.3 DV _{DD}		
	Miscellaneous 10/		0	0.8	
Input voltage, V _I	PCI	3.3 V	0	DV _{DD}	V
	Miscellaneous 10/		0	V _{DDP}	
Output voltage, V _O 11/	PCI	3.3 V	0	DV _{DD}	V
	Miscellaneous 10/		0	DV _{DD}	
Input transition time (t _r and t _f), t _t			0	6	ns
Operating ambient temperature, T _A	R _{θJA} = 70.82 °C/W		-40	85	°C
Output current, I _O	TPBIAS outputs		-5.6	1.3	mA
Differential input voltage, V _{ID}	Cable inputs, during data reception		118	260	mV
	Cable inputs, during arbitration		168	265	
Common-mode input voltage, V _{IC}	TPB cable inputs, source power node		0.4706	2.515	V
	TPB cable inputs, nonsource power node		0.4706	2.015 12/	
Maximum junction temperature, T _J	128-PDT high-K JEDEC board, R _{θJA} = 74.6 °C/W, P _D = 0.36 W	T _A = 85°C		111.9	°C
	128-PDT low-K JEDEC board, R _{θJA} = 101.3 °C/W, P _D = 0.36 W	T _A = 85°C		121.5	°C

See footnotes on next page.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 4

1.4 Recommended operating conditions - Continued. 8/

		Test condition	Min	Max	Unit
Power setup reset time, t_{pu}	$\overline{G_RST}$ input		2		ms
Receiver input jitter	TPA, TPB cable inputs, S100 operation			± 1.08	ns
	TPA, TPB cable inputs, S200 operation			± 0.5	
	TPA, TPB cable inputs, S400 operation			± 0.315	
Receiver input skew	Between TPA and TPB cable inputs, S100 operation			± 0.8	ns
	Between TPA and TPB cable inputs, S200 operation			± 0.55	
	Between TPA and TPB cable inputs, S400 operation			± 0.5	

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1394a-2000 - IEEE Standard for High Performance Serial Bus.

(Copies of these documents are available online at <http://www.ieee.org> or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331).

8/ Use of this product beyond the manufacturer design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

9/ Applies to external inputs and bi-directional buffers without hysteresis.

10/ Miscellaneous terminals are: GPIO2(90), GPIO3 (89), SDA (92), SCL (91).

11/ Applies to external output buffers.

12/ For a node that does not source power; see section 4.2.2.2 in IEEE Std 1394a-2000.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 5

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Block diagram. The block diagram shall be as specified on figure 3.

3.5.4 Timing diagram. The timing diagram shall be as specified on figure 4.

3.5.5 Test diagram. The test diagram shall be as specified on figure 5.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 6

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions Recommended operating conditions unless otherwise specified		Limits		Unit
				Min	Max	
High level output voltage	V _{OH}	PCI	I _{OH} = -0.5 mA	0.9 DV _{DD}		V
			I _{OH} = -2 mA	2.4		
		Miscellaneous 2/	I _{OH} = -4 mA	DV _{DD} - 0.6		
Low level output voltage	V _{OL}	PCI	I _{OL} = 1.5 mA		0.1 DV _{DD}	V
			I _{OL} = 6 mA		0.55	
		Miscellaneous 2/	I _{OL} = 4 mA		0.5	
Three-state output high impedance	I _{OZ}	Output pins	V _{DD} = 3.6 V, V _O = DV _{DD} or GND		±20	µA
Low level input current	I _{IL}	Input pins	V _{DD} = 3.6 V, V _I = GND		±20	µA
		I/O pins 3/	V _{DD} = 3.6 V, V _I = GND	±20		
High level input current	I _{IH}	PCI 3/	V _{DD} = 3.6 V, V _I = DV _{DD}		±20	µA
		Others 3/	V _{DD} = 3.6 V, V _I = DV _{DD}	±20		

Device

Supply current (internal voltage regulator enabled, REG_EN = L)	I _{DD}	4/	33 Typ	mA	
		5/	8.1 Typ		
Supply current (REG_EN = H, external 1.8 V supplied to REG18)	I _{DD}	4/	31.5 Typ	mA	
		5/	6.6 Typ		
Supply current – ultra low power mode (internal voltage regulator enabled, REG_EN = L)	I _{DD(ULP)}	Ports disabled, V _{DD} = 1.8 V (internal), T _A = 25°C	1.5 Typ	mA	
Supply current – ultra low power mode (internal voltage regulator disabled, REG_EN = H, REG18 = 1.8 V)	I _{DD(ULP)}	Ports disabled, V _{DD} = 1.8 V (external), T _A = 25°C	35 Typ	µA	
Power status threshold, CPS inputs 6/	V _{TH}	400 kΩ resistor 6/	4.7	7.5	V
TPBIAS output voltage	V _O	At rated I _O current.	1.665	2.015	V
Input current (PC0-PC2 inputs)	I _I	V _{DD} = 3.6 V		5	µA
Pullup current ($\overline{G_RST}$ input)	I _{IRST}	V _I = 1.5 V	-90	-20	µA
		V _I = 0 V	-90	-20	

Driver

Differential output voltage	V _{OD}	56 Ω, see figure 5.	172	265	mV
Driver difference current, TPA+, TPA-, TPB+, TPB-	I _{DIFF}	Drivers enabled, speed signaling off.	-1.05 7/	1.05 7/	mA
Common-mode speed signaling current, TPB+, TPB-	I _{SP200}	S200 speed signaling enabled.	-4.84 8/	-2.53 8/	mA
Common-mode speed signaling current, TPB+, TPB-	I _{SP400}	S400 speed signaling enabled.	-12.4 8/	-8.1 8/	mA
Off state differential voltage	V _{OFF}	Drivers disabled, see figure 5.		20	mV

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 7

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions Recommended operating conditions unless otherwise specified	Limits		Unit
			Min	Max	
Receiver					
Differential impedance	Z _{ID}	Drivers disabled	4		kΩ
				4	pF
Common mode impedance	Z _{IC}	Drivers disabled	20		kΩ
				24	pF
Receiver input threshold voltage	V _{TH-R}	Drivers disabled	-30	30	mV
Cable bias detect threshold, TPBx cable inputs	V _{TH-CB}	Drivers disabled	0.6	1	V
Positive arbitration comparator threshold voltage	V _{TH+}	Drivers disabled	89	168	MV
Negative arbitration comparator threshold voltage	V _{TH-}	Drivers disabled	-168	-89	mV
Speed signal threshold	V _{TH-SP200}	TPBIAS-TPA common mode voltage, drivers disabled	49	131	mV
Speed signal threshold	V _{TH-SP400}	TPBIAS-TPA common mode voltage, drivers disabled	314	396	mV
Thermal characteristics					
Rθ _{JA} , high K board	128-PDT	Board mounted, no air flow, JEDEC test board.		74.6	°C/W
Rθ _{JA} , low K-board	128-PDT			101.3	°C/W
Rθ _{JC}	128-PDT			18.7	°C/W
Switching characteristics for PHY port interface					
Jitter, transmit		Between TPA and TPB		±0.15	ns
Skew, transmit		Between TPA and TPB		±0.1	ns
TP differential rise time, transmit	t _r	10% to 90%, at 1394 connector	0.5	1.2	ns
TP differential fall time, transmit	t _f	90% to 10%, at 1394 connector	0.5	1.2	ns
Operating, timing, and switching characteristics of XI					
	V _{DD}		3.0	3.6	V(PLL V _{DD})
High level input voltage	V _{IH}		0.63 V _{DD} Typ		V
Low level input voltage	V _{IL}			0.33 V _{DD}	V
Input clock frequency			24.576 Typ		MHz
Input clock frequency tolerance				<100	PPM
Input slew rate			0.2	4	V/ns
Input clock duty cycle			40%	60%	

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 8

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions Recommended operating conditions unless otherwise specified	Limits		Unit
			Min	Max	
Switching characteristics for PCI interface <u>9/</u>					
Setup time for PCLK	t_{su}	-50% to 50%	7		ns
Hold time for PCLK	t_h	-50% to 50%	0		ns
Delay time, PCLK to data valid	t_{val}	-50% to 50%	2	11	ns
Cardbus PC card clock specifications					
CCLK cycle time <u>10/</u>	t_{cyc}		30	∞	ns
CCLK high time	t_{high}		12		ns
CCLK low time	t_{low}		12		ns
CCLK slew rate <u>11/</u>			1	4	V/ns
3.3 V timing parameters					
CCLK to signal valid delay <u>12/ 13/</u>	t_{val}		2	18	ns
Float to active delay <u>12/</u>	t_{on}		2		ns
Active to float delay <u>12/</u>	t_{off}			28	ns
Input set up time to CCLK <u>14/</u>	t_{su}		7		ns
Input hold time from CCLK <u>14/</u>	t_h		0		ns
Reset active time after power stable <u>15/</u>	t_{rst}		1		ms
Reset active time after CCLK stable <u>15/</u>	$t_{rst-clk}$		100		clocks
Reset active to output float delay <u>15/ 16/</u>	$t_{rst-off}$			40	ns
CSTSCHG remote wakeup pulse width <u>17/</u>	t_{pulse}		1		ms

See footnotes on next page.

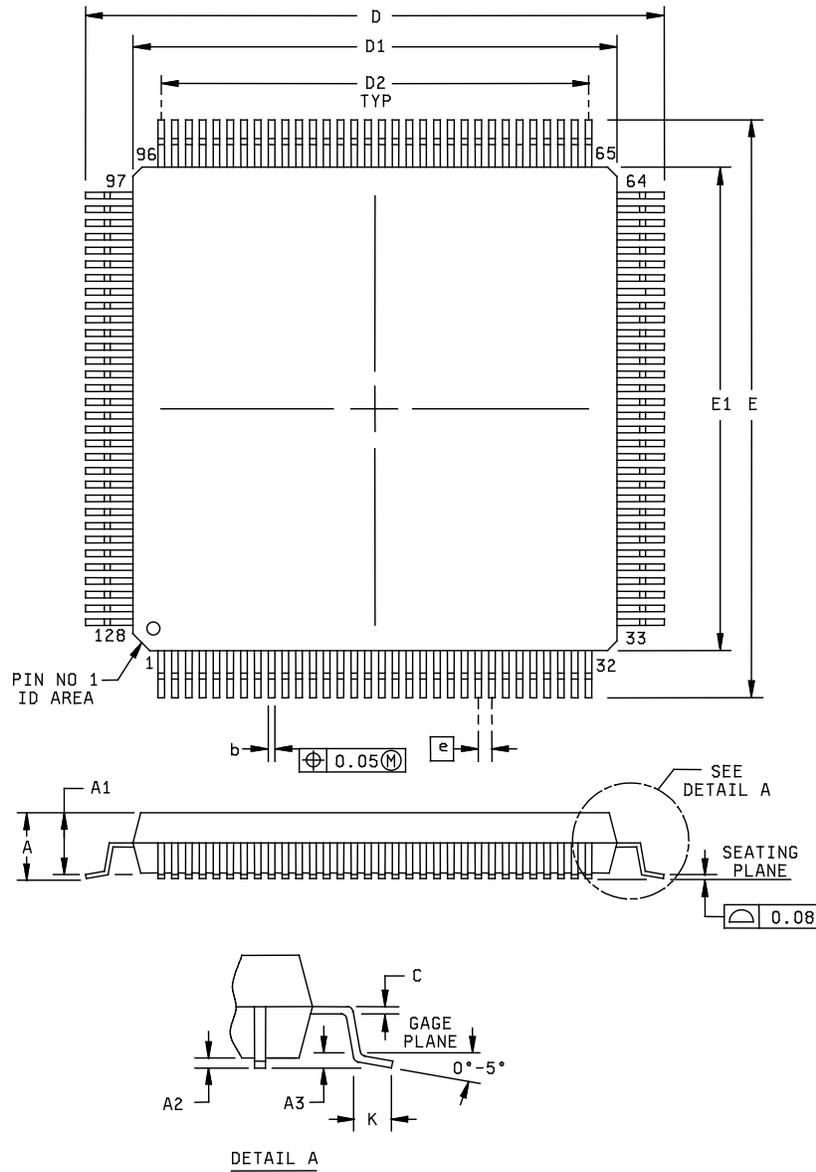
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 9

TABLE I. Electrical performance characteristics - Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Miscellaneous terminals are: GPIO2(90), GPIO3 (89), SDA (92), SCL (91).
- 3/ For I/o terminals, input leakage (I_{IL} and I_{IH}) includes I_{OZ} of the disabled output.
- 4/ Transmit (all port transmit, 100% bandwidth, S400), $V_{DD} = 3.3$ V, $T_A = 25^\circ\text{C}$.
- 5/ Idle (receive or transmit cycle start on the port), $V_{DD} = 3.3$ V, $T_A = 25^\circ\text{C}$.
- 6/ Measured at cable power side of resistor.
- 7/ Limits defined as algebraic sum of TPA+ and TPA- driver currents. Limits also apply to TPB+ and TPB- algebraic sum of driver currents.
- 8/ Limits defined as absolute limit of each of TPB+ and TPB- driver currents.
- 9/ These parameters are ensured by design.
- 10/ In general, all CardBus PC Card components must work with any clock frequency up to 33 MHz. The clock frequency may be changed at any time during the operation of the system so long as the clock edges remain clean (monotonic) and the minimum cycle and high and low times are not violated. If the clock is stopped, it must be in a low state. A variance on this specification is allowed for the CardBus PC Card adapter which may operate the CardBus PC Card interface at any single fixed frequency up to 33 MHz, and may enforce a policy of no frequency changes.
- 11/ Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform (see Figure 4).
- 12/ t_{val} includes the time to propagate data from internal registers to the output buffer and drive the output to a valid level. Minimum t_{val} is measured from CCLK crossing V_{test} to the signal crossing V_{IH} on falling edges and V_{IL} on rising edges. Maximum t_{val} is measured from CCLK crossing V_{test} to the signal's last transition out of the threshold region (V_{IL} for falling edges, V_{IH} for rising edges).
- 13/ Minimum times are specified with 0-pF equivalent load; maximum times are specified with 30-pF equivalent load. Actual test capacitance may vary, but results must be correlated to these specifications. Systems which exceed this capacitance, due to long traces between the socket and adaptor, must reduce the CCLK frequency appropriately.
- 14/ t_{su} and t_h are measured at V_{TH} for rising edges and V_{il} for falling edges.
- 15/ \overline{CRST} is asserted asynchronously and negated synchronously with respect to CCLK. CCLK stable means that V_{CC} is within tolerances and CCLK is meeting specifications.
- 16/ See PC Card Standard – Electrical Specification for the CardBus PC Card and adapter signals which must be in a high impedance state.
- 17/ This parameter only applies when signaling remote wakeup over CSTSCHG terminal. All other status change information must be signaled by asserting CSTSCHG until the resultant interrupt is serviced.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 10

Case X



Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-136

FIGURE 1. Case outline.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03637</p>
		<p>REV B</p>	<p>PAGE 11</p>

Case X

Symbol	Millimeters	
	Min	Max
A		1.20
A1	0.95	1.05
A2	0.05	
A3	0.25 Typ	
b	0.13	0.23
C	0.13 NOM	
D/E	15.90	16.10
D1/E1	13.95	14.05
D2	12.40 Typ	
e	0.40 Typ	
L	0.45	0.75

FIGURE 1. Case outline - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 12

Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name
1	AV _{DD}	33	DGND	65	PCI_AD13	97	PC2
2	AV _{DD}	34	PCI_C/ $\overline{\text{BE3}}$	66	PCI_AD12	98	PC1
3	FILTER0	35	V _{DDP}	67	PCI_AD11	99	PC0
4	FILTER1	36	PCI_IDSEL	68	DGND	10	DV _{DD}
5	X1	37	PCI_AD23	69	PCI_AD10	101	TEST3
6	X0	38	PCI_AD22	70	PCI_AD9	102	TEST2
7	PLL _{VDD}	39	DV _{DD}	71	PCI_AD8	103	DGND
8	PLL _{GND}	40	PCI_AD21	72	DV _{DD}	104	TEST1
9	$\overline{\text{REG_EN}}$	41	PCI_AD20	73	PCI_C/ $\overline{\text{BE0}}$	105	TEST0
10	TEST17	42	PCI_AD19	74	PCI_AD7	106	CPS
11	TEST16	43	PCI_AD18	75	DGND	107	AV _{DD}
12	$\overline{\text{PCI_CLKRUN}}$	44	DGND	76	PCI_AD6	108	AV _{DD}
13	$\overline{\text{PCI_INTA/CINT}}$	45	PCI_AD17	77	PCI_AD5	109	AGND
14	$\overline{\text{G_RST}}$	46	PCI_AD16	78	V _{DDP}	110	AGND
15	DV _{DD}	47	PCI_C/ $\overline{\text{BE2}}$	79	PCI_AD4	111	AGND
16	PCI_CLK	48	V _{DDP}	80	PCI_AD3	112	TPB0-
17	DGND	49	$\overline{\text{PCI_FRAME}}$	81	PCI_AD2	113	TPB0+
18	$\overline{\text{PCI_GNT}}$	50	$\overline{\text{PCI_IRDY}}$	82	PCI_AD1	114	TPA0-
19	$\overline{\text{PCI_REQ}}$	51	DV _{DD}	83	DGND	115	TPA0+
20	V _{DDP}	52	$\overline{\text{PCI_TRDY}}$	84	PCI_AD0	116	TPBIAS0
21	$\overline{\text{PCI_PME/CSTSCHG}}$	53	$\overline{\text{PCI_DEVSEL}}$	85	$\overline{\text{PCI_RST}}$	117	AGND
22	PCI_AD31	54	$\overline{\text{PCI_STOP}}$	86	$\overline{\text{CYCLEOUT/CARDBUS}}$	118	R0
23	DGND	55	DGND	87	CYCLEIN	119	R1
24	PCI_AD30	56	$\overline{\text{PCI_PERR}}$	88	DV _{DD}	120	AV _{DD}
25	PCI_AD29	57	$\overline{\text{PCI_SERR}}$	89	GPIO3	121	NC
26	PCI_AD28	58	PCI_PAR	90	GPIO2	122	NC
27	DV _{DD}	59	DV _{DD}	91	SCL	123	NC
28	PCI_AD27	60	PCI_C/ $\overline{\text{BE1}}$	92	SDA	124	NC
29	PCI_AD26	61	PCI_AD15	93	REG18	125	NC
30	REG18	62	DV _{DDP}	94	TEST9	126	AGND
31	PCI_AD25	63	PCI_AD14	95	TEST8	127	AGND
32	PCI_AD24	64	DGND	96	CNA	128	AGND

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 13

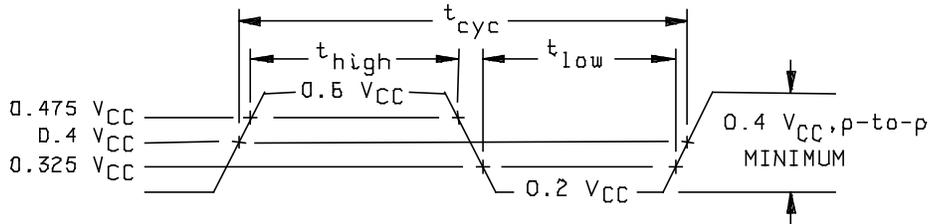


FIGURE 4. Timing diagram.

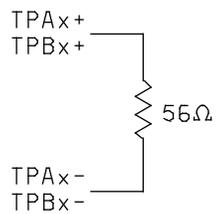


FIGURE 5. Test diagram.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 15

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/03637-01XE	01295	TSB43AB21AIPDTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03637
		REV B	PAGE 16