

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a fast-transient-response 2-A low dropout voltage regulators, with an operating temperature range of -40°C to +125°C and of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/03635</u> Drawing number	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s). 1/

<u>Device Type</u>	<u>Generic</u>	<u>Output voltage</u>	<u>Circuit function</u>
01	TPS75201-EP	+1.5 V to +5.0 V	Fast-transient-response 2-A low-dropout voltage regulator with <u>RESET</u> .
02	TPS75215-EP	+1.5 V	Fast-transient-response 2-A low-dropout voltage regulator with <u>RESET</u> .
03	TPS75218-EP	+1.8 V	Fast-transient-response 2-A low-dropout voltage regulator with <u>RESET</u> .
04	TPS75225-EP	+2.5 V	Fast-transient-response 2-A low-dropout voltage regulator with <u>RESET</u> .
05	TPS75233-EP	+3.3 V	Fast-transient-response 2-A low-dropout voltage regulator with <u>RESET</u> .
06	TPS75301-EP	+1.5 V to +5.0 V	Fast-transient-response 2-A low-dropout voltage regulator with power good.
07	TPS75315-EP	+1.5 V	Fast-transient-response 2-A low-dropout voltage regulator with power good.
08	TPS75318-EP	+1.8 V	Fast-transient-response 2-A low-dropout voltage regulator with power good.
09	TPS75325-EP	+2.5 V	Fast-transient-response 2-A low-dropout voltage regulator with power good.
10	TPS75333-EP	+3.3 V	Fast-transient-response 2-A low-dropout voltage regulator with power good.
11	TPS75201M-EP	+1.5 V to +5.0 V	Fast-transient-response 2-A low-dropout voltage regulator with <u>RESET</u> .

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 2/

Input voltage range (V _I).....	-0.3 V to +5.5 V <u>3/</u>
Voltage range at $\overline{\text{EN}}$	-0.3 V to +16.5 V
Maximum RESET voltage (device type 01-05)	+16.5 V
Maximum PG voltage (device type 06-10)	+16.5 V
Peak output current	Internally limited
Output voltage (V _O) (OUT, FB).....	+5.5 V
Continuous total power dissipation.....	See dissipation rating tables
Operating virtual junction temperature range (T _J):	
Device type 01 to 10	-40°C to +125°C
Device type 11	-55°C to +125°C
Storage temperature range (T _{STG}).....	-65°C to +150°C
ESD rating, (HBM)	2 kV

Dissipation Rating Table – Ambient Temperatures

Case outline	Air Flow (CFM)	T _A < 25°C Power rating	Derating Factor Above T _A = 25°C	T _A = 70°C Power Rating	T _A = 85°C Power Rating
X <u>4/</u>	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
X <u>5/</u>	0	3.0 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

1.4 Recommended operating conditions.

Input voltage range (V _I).....	+2.7 V to +5.0 V	<u>6/</u>
Output voltage (V _O)	+1.5 V to +5.0 V	
Output current (I _O).....	0 to 2.0 A	
Operating virtual junction temperature range (T _J):		
Device type 01 to 10	-40°C to +125°C	
Device type 11	-55°C to +125°C	

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to these devices.

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3/All voltage values are with respect to network terminal ground.

4/ This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5 in x 5 in PCB, 1 oz. copper, 2 in x 2 in coverage.

5/This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5 in x 2 in PCB, 1 oz. copper with layer 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to the manufacturer technical brief SLMA002.

6/To calculate the minimum input voltage for your maximum output current, use the following equation:

$$V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$$

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Block diagrams. The block diagrams shall be as specified on figure 3.

3.5.4 Timing diagram. The timing diagram shall be as specified on figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Test conditions $V_I = V_{O(TYP)} + 1\text{ V}$ $I_O = 1\text{ mA}$, $\overline{EN} = 0\text{ V}$ $C_O = 47\text{ }\mu\text{F}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ <u>2/</u> $-55^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ <u>3/</u> unless otherwise specified	Device type	Limits		Unit	
			Min	Max		
Output voltage <u>4/ 6/</u>	$1.5\text{ V} \leq V_O \leq 5.0\text{ V}$, $T_J = 25^\circ\text{C}$	01, 06, 11	V_O TYP		V	
	$1.5\text{ V} \leq V_O \leq 5.0\text{ V}$		$0.98 V_O$	$1.02 V_O$		
	$2.7\text{ V} < V_{IN} < 5.0\text{ V}$, $T_J = 25^\circ\text{C}$	02, 07	1.5 TYP			
	$2.7\text{ V} \leq V_{IN} \leq 5.0\text{ V}$		1.470	1.530		
	$2.8\text{ V} < V_{IN} < 5.0\text{ V}$, $T_J = 25^\circ\text{C}$	03, 08	1.8 TYP			
	$2.8\text{ V} \leq V_{IN} \leq 5.0\text{ V}$		1.764	1.836		
	$3.5\text{ V} < V_{IN} < 5.0\text{ V}$, $T_J = 25^\circ\text{C}$	04, 09	2.5 TYP			
	$3.5\text{ V} \leq V_{IN} \leq 5.0\text{ V}$		2.450	2.550		
	$4.3\text{ V} < V_{IN} < 5.0\text{ V}$, $T_J = 25^\circ\text{C}$	05, 10	3.3 TYP			
$4.3\text{ V} \leq V_{IN} \leq 5.0\text{ V}$	3.234		3.366			
Quiescent current (GND current) <u>4/</u>	$T_J = 25^\circ\text{C}$, <u>3/</u>	All	75 TYP		μA	
	<u>3/</u>	All		125		
Output voltage line regulation ($\Delta V_O/V_O$) <u>4/ 5/</u>	$V_O + 1\text{ V} < V_I \leq 5.0\text{ V}$, $T_J = 25^\circ\text{C}$	All	0.01 TYP		%V	
	$V_O + 1\text{ V} < V_I \leq 5.0\text{ V}$			0.1		
Load regulation <u>6/</u>		All	1 TYP		mV	
Output noise voltage	BW = 300 Hz to 50 kHz, $V_O = 1.5\text{ V}$, $C_O = 100\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$	04, 09, 11	60 TYP		μV_{rms}	
Output current limit	$V_O = 0\text{ V}$	All		4.5	A	
Thermal shutdown junction temperature		All	150 TYP		$^\circ\text{C}$	
Standby current	$\overline{EN} = V_I$, $T_J = 25^\circ\text{C}$,	All	1 TYP		μA	
	$\overline{EN} = V_I$			10		
FB input current	FB = 1.5 V	01, 06, 11	-1.0	1.0	μA	
High level enable input voltage		All	2.0		V	
Low level enable input voltage				0.7		V
Power supply ripple rejection <u>5/</u>	$f = 100\text{ Hz}$, $C_O = 100\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$, $I_O = 2.0\text{ A}$ <u>4/</u>			60 TYP		dB
Reset	Minimum input voltage for valid RESET	01-05, 11		1.3	V	
	Trip threshold voltage		V_O decreasing	92	98	$\%V_O$
	Hysteresis voltage		Measured at V_O	0.5 TYP		$\%V_O$
	Output low voltage		$V_I = 2.7\text{ V}$, $I_{O(RESET)} = 1\text{ mA}$		0.4	V
	Leakage current		$V_{(RESET)} = 5\text{ V}$		1.0	μA
	RESET time out delay			100 TYP		ms

See notes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test		Test conditions $V_I = V_{O(Typ)} + 1\text{ V}$ $I_O = 1\text{ mA}, \overline{EN} = 0\text{ V}$ $C_O = 47\text{ }\mu\text{F}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ <u>2/</u> $-55^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ <u>3/</u> unless otherwise specified	Device type	Limits		Unit
				Min	Max	
PG	Minimum input voltage for valid PG	$I_{O(PG)} = 300\text{ }\mu\text{A}, V_{(PG)} \leq 0.8\text{ V}$	06 - 10		1.3	V
	Trip threshold voltage	V_O decreasing		80	86	% V_O
	Hysteresis voltage	Measured at V_O		0.5 TYP		% V_O
	Output low voltage	$I_{O(PG)} = 1\text{ mA}$			0.4	V
	Leakage current	$V_{(PG)} = 5\text{ V}$			1	μA
Input current (\overline{EN})		$\overline{EN} = V_I$	All	-1	1	μA
		$\overline{EN} = 0\text{ V}$		-1	1	μA
High level \overline{EN} input voltage			All	2.0		V
Low level \overline{EN} input voltage			All		0.7	V
Dropout voltage (3.3 V Output) <u>7/</u>		$I_O = 2.0\text{ A}, V_I = 3.2\text{ V}, T_J = 25^\circ\text{C}$	All	210 TYP		mV
		$I_O = 2.0\text{ A}, V_I = 3.2\text{ V}$			400	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ For device type 01 to 10

3/ For device type 11.

4/ Minimum IN operating voltage is 2.7 V or $V_{O(Typ)} + 1\text{V}$, whichever is greater. Maximum IN voltage 5.0 V.

5/ If $V_O \leq 1.8\text{ V}$ then $V_{imin} = 2.7\text{ V}, V_{imax} = 5.0\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{imax} - 2.7V)}{100} \times 1000$$

If $V_O \geq 2.5\text{ V}$ then $V_{imin} = V_O + 1\text{ V}, V_{imax} = 5.0\text{ V}$.

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{imax} - (V_O + 1V))}{100} \times 1000$$

6/ $I_O = 1\text{ mA}$ to 2.0 A.

7/ IN voltage equals $V_{O(Typ)} - 100\text{ mV}$; Device type 02, 03, 04, 06, 07 and 08 dropout voltage limited by input voltage range limitations (i.e., device type 05 and 10 input voltage needs to drop to 3.2 V for purpose of this test).

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Case X

Symbol	Millimeters	
	Min	Max
A		1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 NOM	
D	6.40	6.60
E	4.30	4.500
E1	6.20	6.60
e	0.65 TYP	
L	0.50	0.75

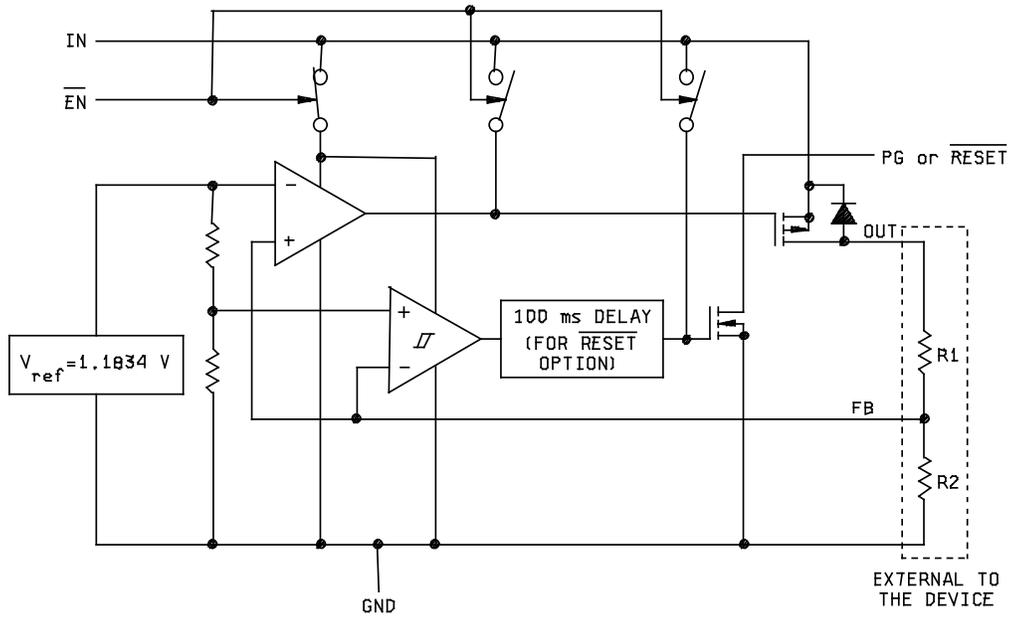
FIGURE 1. Case outline - Continued.

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND/HEATSINK	11	GND/HEATSINK
2	NC	12	NC
3	IN	13	NC
4	IN	14	NC
5	$\overline{\text{EN}}$	15	NC
6	$\overline{\text{RESET}}$ or PG <u>1/</u>	16	NC
7	FB/SENSE	17	GND
8	OUTPUT	18	NC
9	OUTPUT	19	NC
10	GND/HEASINK	20	GND/HEATSINK

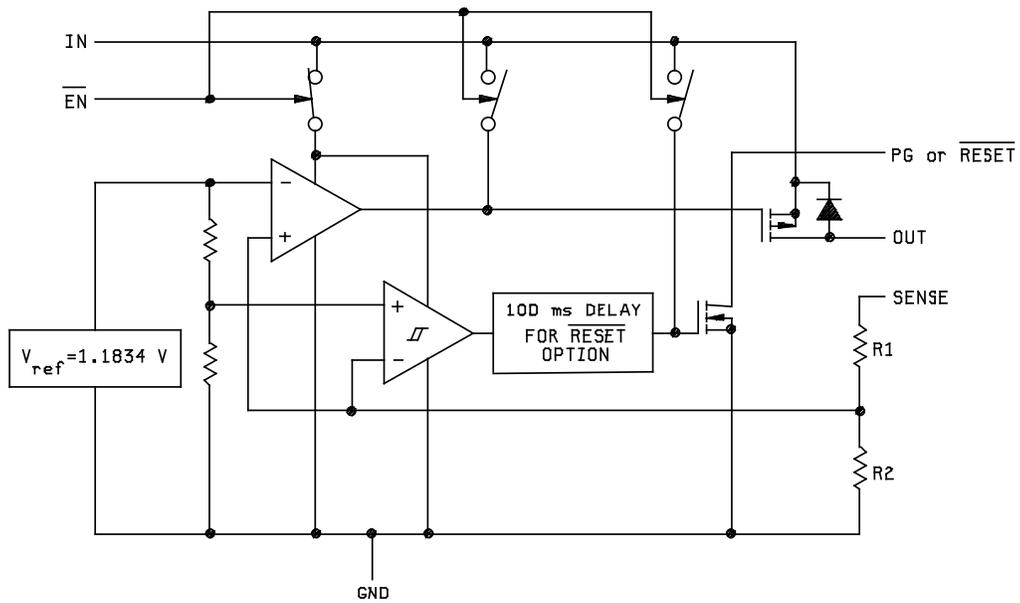
1/ PG is on the device types: 06-10 and $\overline{\text{RESET}}$ is on the device type 01-05.
 NC: No internal connection

FIGURE 2. Terminal connections.

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Functional block diagram – adjustable version

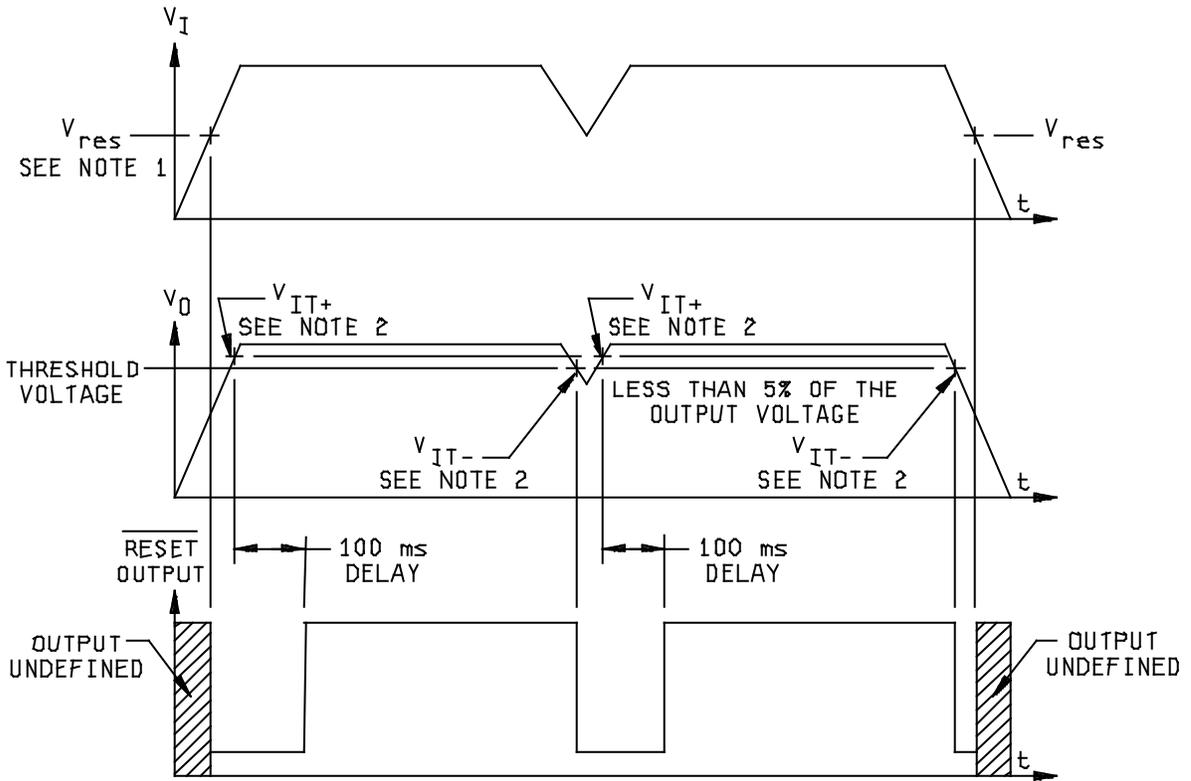


Functional block diagram – fixed voltage version

FIGURE 3. Block diagrams.

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RESET timing diagram



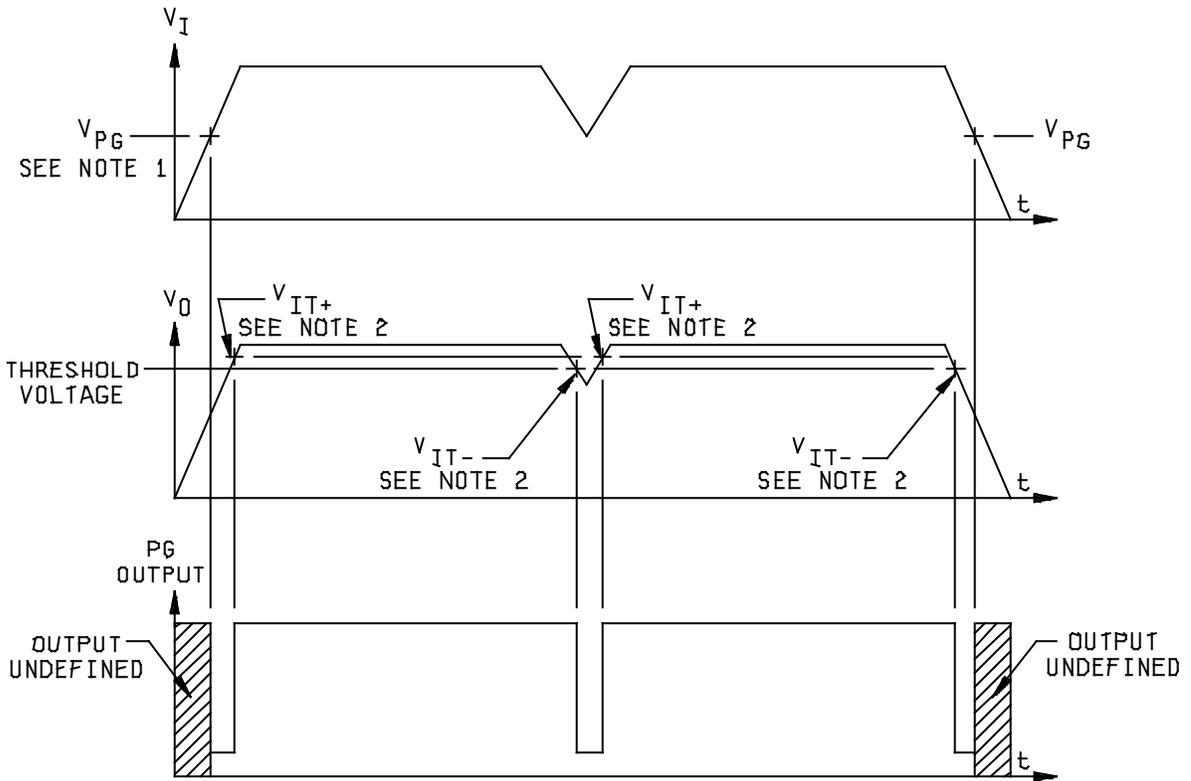
NOTES:

1. V_{res} is the minimum input voltage for a valid \overline{RESET} . The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.
2. V_{IT} - Trip voltage is typically 5% lower than the output voltage (95% V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

FIGURE 4. Timing diagram.

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PG timing diagram



Notes:

1. V_{PG} is the minimum input voltage for a valid PG. The symbol V_{PG} is not currently listed within EIA or JEDEC standards for semiconductor symbology.
2. V_{IT-} . Trip voltage is typically 17 % lower than the output voltage (83% V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

FIGURE 4. Timing diagram - Continued.

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4 VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number <u>2/</u>
V62/03635-01XE	01295	TPS75201QPWPEP <u>3/</u>
V62/03635-02XE	01295	TPS75215QPWPEP
V62/03635-03XE	01295	TPS75218QPWPEP
V62/03635-04XE	01295	TPS75225QPWPEP
V62/03635-05XE	01295	TPS75233QPWPEP
V62/03635-06XE	01295	TPS75301QPWPEP
V62/03635-07XE	01295	TPS75315QPWPEP
V62/03635-08XE	01295	TPS75318QPWPEP
V62/03635-09XE	01295	TPS75325QPWPEP
V62/03635-10XE	01295	TPS75333QPWPEP
V62/03635-11XE	01295	TPS75201MPWPREP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ The PWP package is available taped and reeled. Add an R suffix to the device type (e.g., TPS75201QPWPREP) to indicate tape and reel.
- 3/ This device is programmable using an external resistor divider (see manufacturer application information).
- 4/ This device is not available from an approved source of supplied.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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