REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update the boilerplate paragraphs. - ro	09-02-19	R. HEBER
B	Add footnote 1/ to Table I. Update document paragraphs to current requirements. - ro	15-02-05	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B	B							
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 03-05-27	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, LINEAR, PRECISION LOW DROPOUT CONTROLLER, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/03633**
	REV **B**	**PAGE** 1 **OF** 12

AMSC N/A

5962-V014-15

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance precision low dropout linear controller microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03633	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	UC2832-EP	Precision low dropout linear controller

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-013	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage (V_{IN}) ..... 40 V
Driver output current (sink or source) (I_O) ..... 450 mA
Driver sink to source voltage ..... 40 V
TRC pin voltage ..... -0.3 V to 3.2 V
Other input voltages ..... -0.3 V to supply voltage
Operating junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds ..... +300°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

1.4 Recommended operating conditions. 3/

Supply voltage (V_{IN}) ..... 15 V
Ambient operating temperature range (T_A) ..... -40°C to +105°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input supply section							
Supply current	I_{IN}	$+V_{IN}$ = 6 V	-40°C to +105°C	01		10	mA
		$+V_{IN}$ = 36 V				15	
		Logic disable = 2 V				10	
Reference section							
Output voltage	V_{OUT}	I_{DRIVER} = 10 mA	T_J = +25°C	01	1.98	2.02	V
			T_J = -40°C to +105°C		1.96	2.04	
Load regulation voltage	V_{LD}	I_{OUT} = 0 mA to 10 mA	-40°C to +105°C	01	-10	10	mV
Line regulation voltage	V_{LN}	$+V_{IN}$ = 4.5 V to 36 V, I_{DRIVER} = 10 mA	-40°C to +105°C	01		0.5	mV/V
Under-voltage lockout threshold	UVLO		-40°C to +105°C	01		4.5	V
Logic disable input section							
Threshold voltage	V_{TH}		-40°C to +105°C	01	1.3	1.5	V
Input bias current	I_{IB}	Logic disable pin = 0 V	-40°C to +105°C	01	-5.0	0.1	µA
Current sense section							
Comparator offset voltage	V_{OS}		T_J = +25°C	01	95	105	mV
			T_J = -40°C to +105°C		93	107	
Amplifier offset voltage	V_{OS}	V_{ADJ} = open	-40°C to +105°C	01	110	170	mV
		V_{ADJ} = 1 V			180	290	
		V_{ADJ} = 0 V			250	360	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Current sense section - continued							
Input bias current	I_{IB}	$V_{CM} = +V_{IN}$	-40°C to +105°C	01	65	135	µA
Input offset current	I_{IO}	$V_{CM} = +V_{IN}$	-40°C to +105°C	01	-10	10	µA
Amplifier CMRR		V_{CM} = 4.1 V to $+V_{IN}$ + 0.3 V	-40°C to +105°C	01	80 typical		dB
Transconductance		$I_{COMP} = \pm 100$ µA	-40°C to +105°C	01	65 typical		ms
V_{ADJ} input current		V_{ADJ} = 0 V	-40°C to +105°C	01	-10		µA
Timer section							
Inactive leakage current	I_{IL}	C/S(+) = C/S(-) = $+V_{IN}$, TRC pin = 2 V	-40°C to +105°C	01		1.0	µA
Active pullup current	I_{AP}	C/S(+) = $+V_{IN}$, C/S(-) = $+V_{IN}$ – 0.4 V, TRC pin = 0 V	-40°C to +105°C	01	-345	-175	µA
Duty ratio 3/		On time / period, R_T = 200 kΩ, C_T = 0.27 µF	-40°C to +105°C	01	4.8 typical		%
Period 3/ 4/		On time + off time, R_T = 200 kΩ, C_T = 0.27 µF	-40°C to +105°C	01	36 typical		ms
Upper trip threshold	V_U		-40°C to +105°C	01	1.8 typical		V
Lower trip threshold	V_L		-40°C to +105°C	01	0.9 typical		V
Trip threshold ratio		V_U / V_L	-40°C to +105°C	01	2.0 typical		V/V
Error amplifier section							
Input offset voltage	V_{IO}	$V_{CM} = V_{COMP}$ = 2 V	-40°C to +105°C	01	-8.0	8.0	mV
Input bias current	I_{IB}	$V_{CM} = V_{COMP}$ = 2 V	-40°C to +105°C	01	-4.5		µA
Input offset current	I_{IO}	$V_{CM} = V_{COMP}$ = 2 V	-40°C to +105°C	01	-1.5	1.5	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Error amplifier section – continued.							
Open loop voltage gain	A_{VOL}	V_{COMP} = 1 V to 13 V	-40°C to +105°C	01	50		dB
Common mode rejection ratio	CMRR	V_{CM} = 0 V to $+V_{IN}$ – 3 V	-40°C to +105°C	01	60		dB
Power supply rejection ratio	PSRR	V_{CM} = 2 V, $+V_{IN}$ = 4.5 V to 36 V	-40°C to +105°C	01	90 typical		dB
Transconductance		I_{COMP} = ±10 μA	-40°C to +105°C	01	4.3 typical		ms
High level output voltage	V_{OH}	I_{COMP} = 0, volts below $+V_{IN}$	-40°C to +105°C	01		1.3	V
Low level output voltage	V_{OL}	I_{COMP} = 0	-40°C to +105°C	01		0.7	V
Output high current	I_{OH}	V_{COMP} = 2 V	-40°C to +105°C	01	-700	-100	μA
Output low current	I_{OL}	V_{COMP} = 2 V, C/S(-) = $+V_{IN}$	-40°C to +105°C	01	100	700	μA
		V_{COMP} = 2 V, C/S(-) = $+V_{IN}$ – 0.4 V			2		mA
Driver section							
Maximum current	I_{MAX}	Driver limit and source pins common	T_J = +25°C	01	200	400	mA
			T_J = -40°C to +105°C		100	450	
Limiting voltage		Driver limit to source voltage at current limit, I_{SOURCE} = -10 mA 5/	T_J = +25°C	01	0.72 typical		V
Internal current sense resistance		5/	T_J = +25°C	01	2.4 typical		Ω

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver section – continued.							
Pull-up current at driver sink	I_{PU}	COMP/SHUTDOWN = 0.4 V, driver sink = $+V_{IN}$ – 1 V	-40°C to +105°C	01	-800	-100	µA
		COMP/SHUTDOWN = 0.4 V, $+V_{IN}$ = 36 V, driver sink = 35 V			-1000	-75	
Pull-down current at driver source	I_{PD}	COMP/SHUTDOWN = 0.4 V, driver source = 1 V	-40°C to +105°C	01	150	700	µA
Saturation voltage sink to source		Driver source = 0 V, driver current = 100 mA	-40°C to +105°C	01	1.5 typical		V
Maximum source voltage		Driver sink = $+V_{IN}$, volts below $+V_{IN}$, driver current = 100 mA	-40°C to +105°C	01	3 typical		V
Under voltage lock out sink leakage		$+V_{IN}$ = C/S(+) = C/S(-) = 2.5 V, driver sink = 15 V, driver source = 0 V	+25°C	01	25 typical		µA
Maximum reverse source voltage		COMP/SHUTDOWN = 0 V, I_{SOURCE} = 100 µA, (+)V_{IN} = 3 V	-40°C to +105°C	01	1.6 typical		V
Thermal shutdown			-40°C to +105°C	01	160 typical		°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, $+V_{IN}$ = 15 V, driver sink = $+V_{IN}$, C/S(+) voltage = $+V_{IN}$, and $T_A = T_J$.

3/ These parameters are first-order supply-independent, however, both may vary with supply for $+V_{IN}$ less than about 4 V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.

4/ With recommended R_T value of 200 kΩ, $T_{OFF} = R_T C_T * \ln(V_U / V_L)$ ±10 %.

5/ The internal current limiting voltage has a temperature dependence of approximately –2.0 mV / °C, or –2800 ppm / °C. The internal 2.4 Ω sense resistor has a temperature dependence of approximately +1500 ppm / °C.

Case X

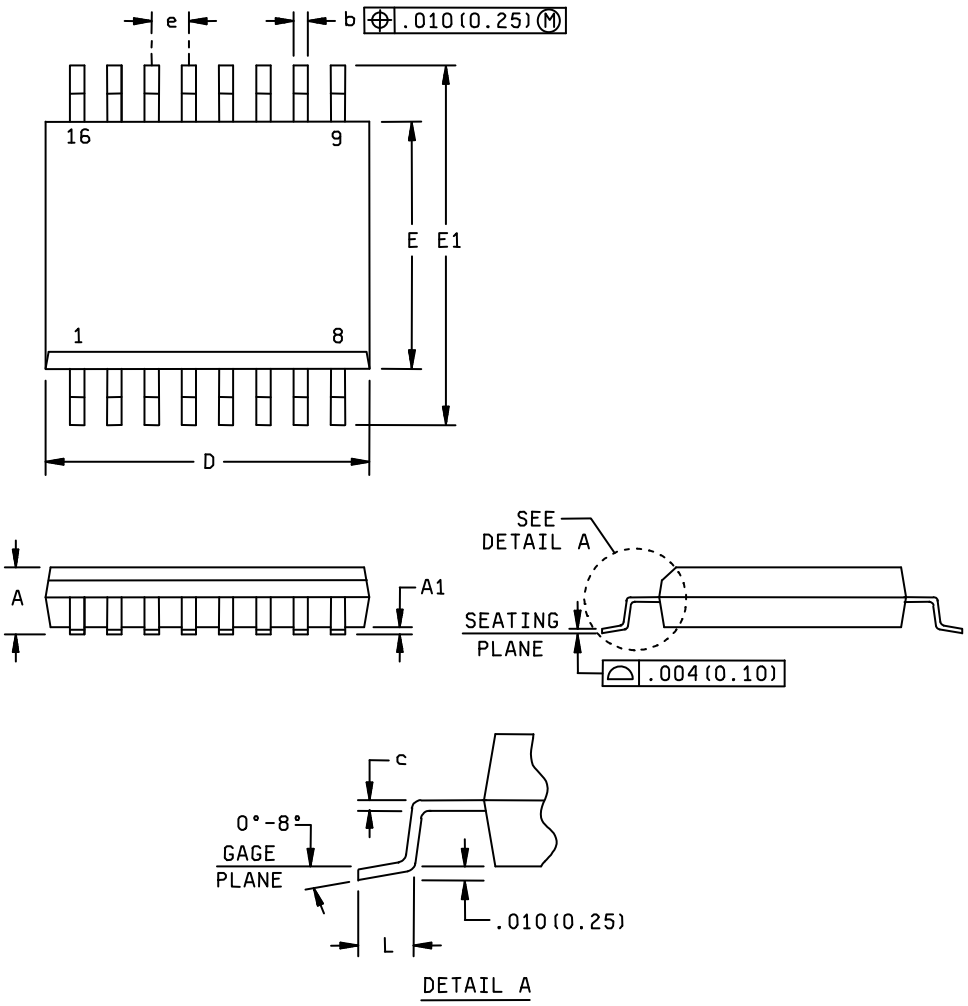

FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.104	---	2.65
A1	.004	.012	0.10	0.30
b	.014	.020	0.35	0.51
c	.010 nominal		0.25 nominal	
D	.400	.410	10.16	10.41
E	.291	.299	7.39	7.59
E1	.400	.419	10.15	10.65
e	.050 BSC		1.27 BSC	
L	.016	.050	0.40	1.27

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion, not to exceed .006 inches (0.15 mm).
3. Falls within JEDEC MS-013.

FIGURE 1. Case outline – continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	$+V_{IN}$
2	COMP / SHUTDOWN
3	E/A(+)
4	+2 V REF
5	GND
6	LOGIC DISABLE
7	LIMIT
8	SOURCE
9	E/A(-)
10	SINK
11	NC
12	V_{ADJ}
13	NC
14	TIMER RC
15	CURRENT SENSE (-) C/S(-)
16	CURRENT SENSE (+) C/S(+)

NC = No connection

FIGURE 2. Terminal connections.

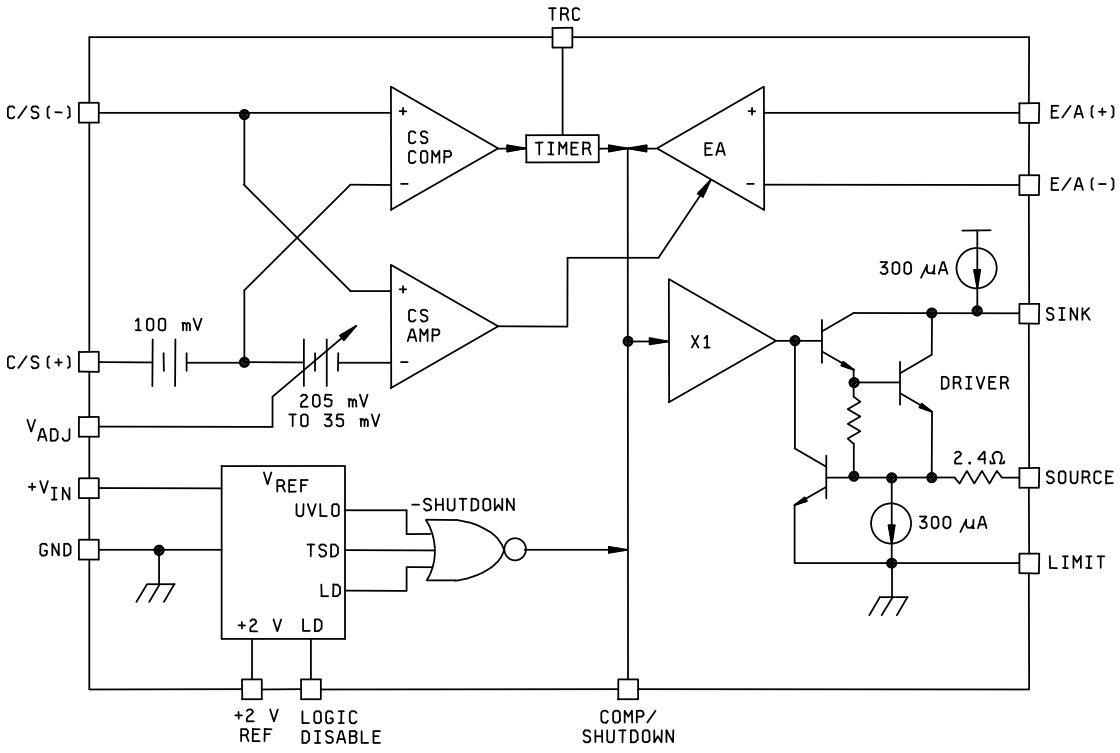

FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package	Top side marking	Vendor part number 2/
V62/03633-01XE	01295	Tape and reel	UC2832TEP	UC2832TDWREP
		Tube		UC2832TDWEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ The "R" designates in the vendor part number the part is supplied as tape and reel.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493