



1. SCOPE

1.1 Scope. This drawing documents the general requirements of an OHCI-Lynx PCI-Based IEEE 1394 host controller microcircuit, with an operating temperature range of -40°C to +110°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/03627</u>   Drawing number	<u>01</u>   Device type (See 1.2.1)	<u>X</u>   Case outline (See 1.2.2)	<u>E</u>   Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u> 1/	<u>Generic</u>	<u>Circuit function</u>
01	TSB12LV26-EP	OHCI-LYNX PCI Based IEEE 1394 host controller

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	100	JEDEC MS-026	Plastic quad flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/03627</b>
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1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V to +3.6 V
Supply voltage range ( $V_{CCP}$ ).....	-0.5 V to +5.5 V
Input voltage range for PCI ( $V_I$ ).....	-0.5 V to $V_{CCP} + 0.5V$
Input voltage range for miscellaneous and PHY interface ( $V_I$ ) .....	-0.5 V to $V_{CC1} + 0.5V$
Output voltage range for PCI ( $V_O$ ).....	-0.5 V to $V_{CCP} + 0.5V$
Output voltage range for miscellaneous and PHY interface ( $V_O$ ) .....	-0.5 V to $V_{CCP} + 0.5V$
Input clamp current ( $I_{IK}$ ) ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA <u>2/</u>
Output clamp current ( $I_{OK}$ ) ( $V_O < 0$ or $V_O > V_{CC}$ ).....	$\pm 20$ mA <u>3/</u>
Ambient operating temperature range ( $T_A$ ) .....	-40°C to +110°C
Storage temperature range ( $T_{STG}$ ).....	-65°C to +150°C

1.4 Recommended operating conditions. 4/

Supply voltage range ( $V_{CC}$ ):	
Core voltage (3.3 V operation) .....	+3.0 V to +3.6 V
Supply voltage range ( $V_{CCP}$ ):	
PCI I/O clamping voltage (3.3 V operation).....	+3.0 V to +3.6 V
PCI I/O clamping voltage (5V operation).....	+4.5 V to +5.5 V
High level input voltage ( $V_{IH}$ ): <u>5/</u>	
PCI (3.3 V operation) .....	+0.475 $V_{CCP}$ to $V_{CCP}$
PCI (5 V operation) .....	+2.0 V to +3.6 V
PHY interface.....	+2.0 V to +3.6 V
Miscellaneous .....	+2.0 V to $V_{CCP}$ <u>6/</u>
Low-level input voltage ( $V_{IL}$ ): <u>5/</u>	
PCI (3.3 V operation) .....	+0.0 V to +0.325 $V_{CCP}$
PCI (5 V operation) .....	+0.0 V to +0.8 V
PHY interface.....	+0.0 V to +0.8 V
Miscellaneous .....	+0.0 V to +0.8 V <u>6/</u>
Input voltage ( $V_I$ ):	
PCI (3.3 V operation) .....	+0.0 V to $V_{CCP}$
PHY interface.....	+0.0 V to +3.6 V
Miscellaneous .....	+0.0 V to $V_{CCP}$ <u>6/</u>
Output voltage ( $V_O$ ): <u>7/</u>	
PCI (3.3 V operation) .....	+0.0 V to $V_{CCP}$
PHY interface.....	+0.0 V to +3.6 V
Miscellaneous .....	+0.0 V to $V_{CCP}$ <u>6/</u>
Input transition time ( $t_f$ and $t_r$ ):	
PCI .....	0 to 6 ns
Ambient operating temperature range ( $T_A$ ) .....	-40°C to +110°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Applies to external input and bi-directional buffers.  $V_I > V_{CCP}$ .

3/ Applies to external output and bi-directional buffers.  $V_O > V_{CCP}$ .

4/ Use of this product beyond the manufacturer design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

5/ Applies for external inputs and bi-directional buffers without hysteresis.

6/ Miscellaneous terminals are: GPIO2 (2), GPIO3 (3), SDA (5), SCL (4), CYCLEOUT (77).

7/ Applies to external output buffers.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE 1394-1995 - (1394) Standard for High-Performance Serial Bus

(Copies of these documents are available online at <http://www.ieee.org> or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855–1331).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Block and logic diagrams. The block and logic diagrams shall be as specified on figure 3.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions -40°C ≤ T <sub>A</sub> ≤ +110°C +3.0 V ≤ V <sub>CC</sub> ≤ 3.6 V +3.0 V ≤ V <sub>CCP</sub> ≤ 3.6 V +4.5 V ≤ V <sub>CCP</sub> ≤ 5.5 V unless otherwise specified		Limits		Unit
				Min	Max	
High level output voltage	V <sub>OH</sub>	PCI	I <sub>OH</sub> = -0.5 mA	0.9 V <sub>CC</sub>		V
			I <sub>OH</sub> = -2 mA	2.4		
		PHY interface	I <sub>OH</sub> = -4 μA	2.8		
			I <sub>OH</sub> = -8 mA	V <sub>CC</sub> - 0.6		
		Miscellaneous <u>2/</u>	I <sub>OH</sub> = -4 mA	V <sub>CC</sub> - 0.6		
Low level output voltage <u>3/</u>	V <sub>OL</sub>	PCI	I <sub>OL</sub> = 1.5 mA		0.1 V <sub>CC</sub>	V
			I <sub>OL</sub> = 6 mA	0	0.55	
		PHY interface	I <sub>OL</sub> = 4 mA		0.4	
			I <sub>OL</sub> = 8 mA			
		Miscellaneous <u>2/</u>	I <sub>OL</sub> = 4 mA		0.5	
Three state output high impedance	I <sub>OZ</sub>	Output pins <u>4/</u>	V <sub>O</sub> = V <sub>CC</sub> or GND		±20	μA
Low level input current	I <sub>IL</sub>	Input pins <u>4/</u>	V <sub>I</sub> = GND <u>1/</u>		±20	μA
		I/O pins <u>3/ 4/</u>	V <sub>I</sub> = GND <u>1/</u>	±20		
High level input current	I <sub>IH</sub>	PCI <u>3/ 4/</u>	V <sub>I</sub> = GND <u>1/</u>		±20	μA
		Others <u>3/ 4/</u>	V <sub>I</sub> = GND <u>1/</u>	±20		

See footnotes at end of table.

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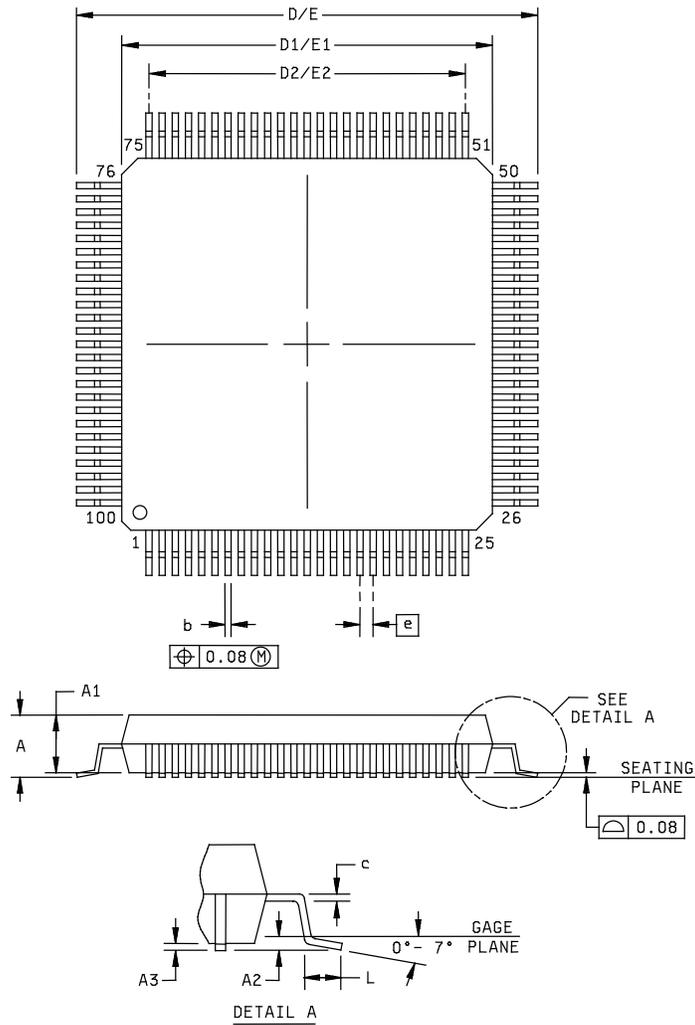
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions -40°C ≤ T <sub>A</sub> ≤ +110°C +3.0 V ≤ V <sub>CC</sub> ≤ 3.6 V +3.0 V ≤ V <sub>CCP</sub> ≤ 3.6 V +4.5 V ≤ V <sub>CCP</sub> ≤ 5.5 V unless otherwise specified	Limits		Unit
			Min	Max	
Switching characteristics for PCI interface <u>5/</u>					
Set up time before PCLK	t <sub>SU</sub> <u>6/</u>		7		ns
Hold time before PCLK	t <sub>H</sub> <u>6/</u>		0		
Delay time, PHY_CLK to data valid	t <sub>VAL</sub> <u>6/</u>		2	11	
Switching characteristics for PHY-Link interface <u>5/</u>					
Set up time, Dn, CTLn, LREQ to PHY_CLK	t <sub>SU</sub> <u>6/</u>		6		ns
Hold time, Dn, CTLn, LREQ before PHY_CLK	t <sub>H</sub> <u>6/</u>		0		
Delay time, PHY_CLK to Dn, CTLn	t <sub>D</sub> <u>6/</u>		2	11	

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Miscellaneous terminals are: GPIO2 (2), GPIO3 (3), SDA (5), SCL (4), CYCLEOUT (77).
- 3/ For I/O terminals, input leakage (I<sub>IL</sub> and I<sub>IH</sub>) includes I<sub>OZ</sub> of the disabled output.
- 4/ 3.6 V operations.
- 5/ These parameters are ensured by design.
- 6/ Measured -50% to 50%.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.60	D/E	15.80	16.20
A1	1.35	1.45	D1/E1	13.80	14.20
A2	0.25 TYP		D2/E2	12.0 TYP	
A3	0.05		e	0.50 TYP	
b	0.17	0.27	L	0.45	0.75
c	0.13 NOM				

Notes:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MS-026.

FIGURE 1. Case outline.

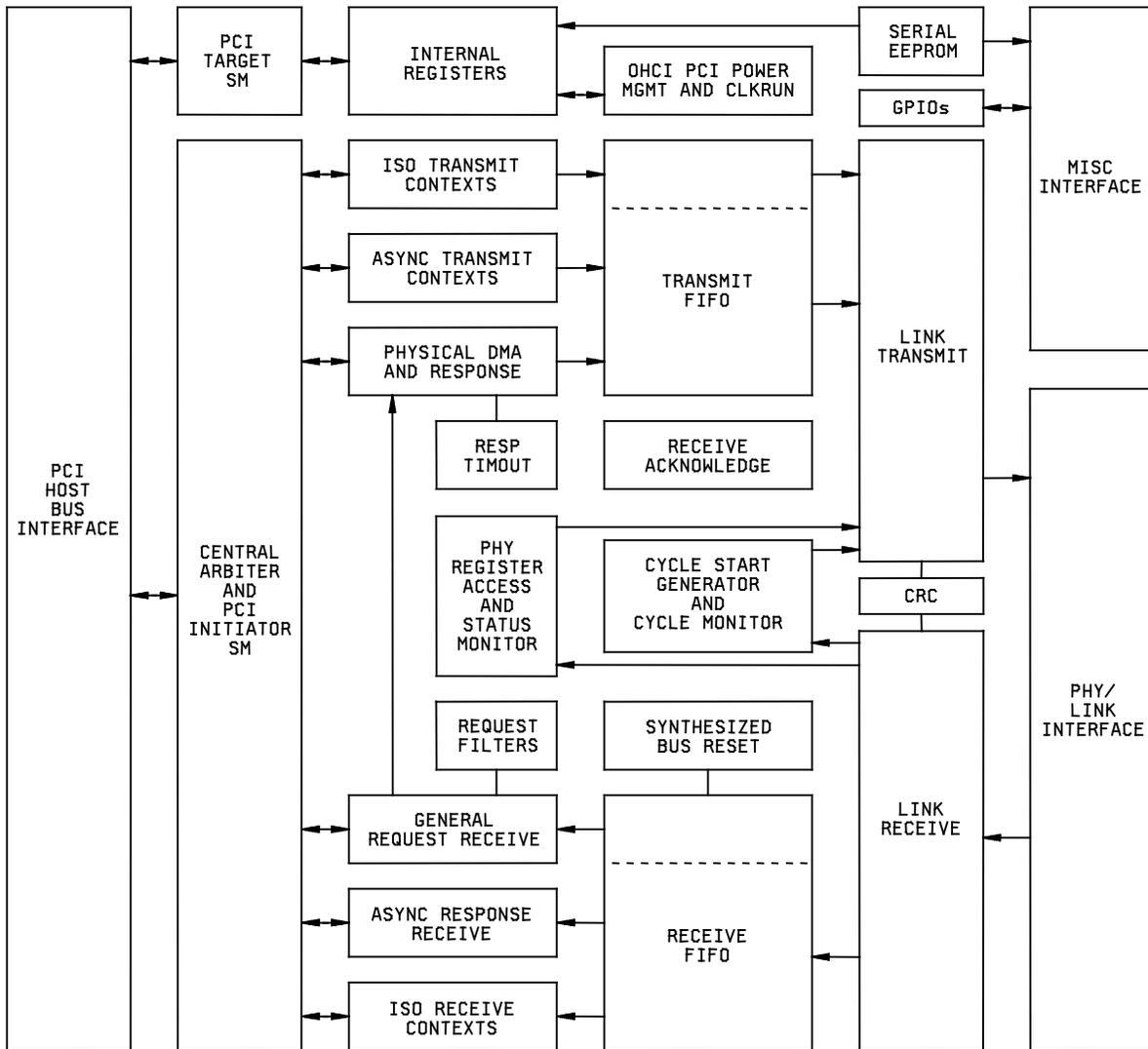
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C  
Case X

Terminal number	Terminal symbol						
1	GND	26	PCI_AD25	51	PCI_SERR	76	PCI_RST
2	GPIO2	27	PCI_AD24	52	PCI_PAR	77	CYCLEOUT
3	GPIO3	28	PCI_C/BE3	53	PCI_C/BE1	78	CYCLEIN
4	SCL	29	PCI_IDSEL	54	PCI_AD15	79	REG_EN
5	SDA	30	GND	55	3.3 V <sub>CC</sub>	80	3.3 V <sub>CC</sub>
6	V <sub>CCP</sub>	31	PCI_AD23	56	PCI_AD14	81	PHY_DATA7
7	PCI_CLKRUN	32	PCI_AD22	57	PCI_AD13	82	PHY_DATA6
8	PCI_INTA	33	PCI_AD21	58	PCI_AD12	83	GND
9	3.3 V <sub>CC</sub>	34	PCI_AD20	59	PCI_AD11	84	PHY_DATA5
10	G_RST	35	3.3 V <sub>CC</sub>	60	GND	85	PHY_DATA4
11	GND	36	PCI_AD19	61	PCI_AD10	86	PHY_DATA3
12	PCI_CLK	37	PCI_AD18	62	PCI_AD9	87	V <sub>CCP</sub>
13	3.3 V <sub>CC</sub>	38	PCI_AD17	63	V <sub>CCP</sub>	88	PHY_DATA2
14	PCI_GNT	39	V <sub>CCP</sub>	64	PCI_AD8	89	PHY_DATA1
15	PCI_REQ	40	PCI_AD16	65	PCI_C/BE0	90	PHY_DATA0
16	V <sub>CCP</sub>	41	PCI_C/BE2	66	PCI_AD7	91	3.3 V <sub>CC</sub>
17	PCI_PME	42	REG18	67	PCI_AD6	92	PHY_CTL1
18	PCI_AD31	43	PCI_FRAME	68	PCI_AD5	93	PHY_CTL0
19	PCI_AD30	44	PCI_IRDY	69	PCI_AD4	94	GND
20	3.3 V <sub>CC</sub>	45	PCI_TRDY	70	3.3 V <sub>CC</sub>	95	PHY_SCLK
21	PCI_AD29	46	3.3 V <sub>CC</sub>	71	PCI_AD3	96	3.3 V <sub>CC</sub>
22	PCI_AD28	47	PCI_DEVSEL	72	PCI_AD2	97	PHY_LREQ
23	PCI_AD27	48	PCI_STOP	73	PCI_AD1	98	PHY_LINKON
24	GND	49	PCI_PERR	74	PCI_AD0	99	PHY_LPS
25	PCI_AD26	50	GND	75	GND	100	REG18

FIGURE 2. Terminal connections.

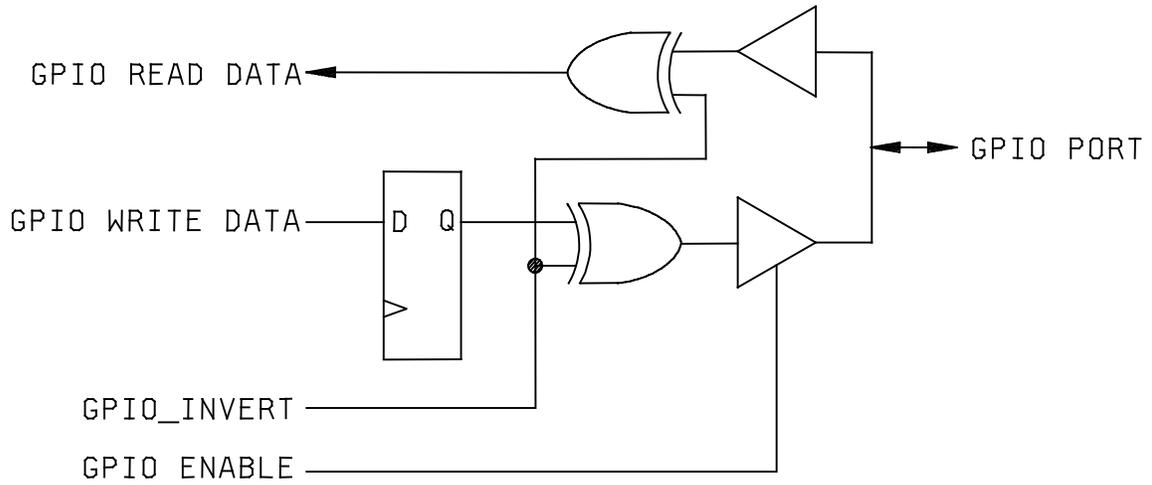
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TSB12LV26 BLOCK DIAGRAM

FIGURE 3. Block and logic diagrams.

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GPIO2 and GPIO3 LOGIC DIAGRAM

FIGURE 3. Block and logic diagrams – Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03627-01XE	01295	TSB12LV26TPZEP	TSB12LV26TEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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