REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate paragraphs to current requirements. - CFS	08-02-25	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-08-25	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	20-05-26	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C				
PAGE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35				
REV STATUS OF PAGES	**REV**			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 03-01-21	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/03616**
	REV **C**	**PAGE** 1 **OF** 35

AMSC N/A

5962-V051-20

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance floating-point digital signal processor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03616	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	320C32-50EP	Digital signal processor
02	320C32-60EP	Digital signal processor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	144	JEDEC MS-022	Plastic quad flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V to +7.0 V 2/
DC input voltage range (V_{IN})	-0.3 V to +7.0 V
DC output voltage range (V_O)	-0.3 V to +7.0 V
Continuous power dissipation (P_D)	1.95 W 3/
Operating case temperature range (T_C)	-55°C to +125°C
Storage temperature range (T_{STG})	-55°C to +150°C

1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (DV_{DD}, V_{DDL})	+4.75 V to +5.25 V
High-level input voltage range (V_{IH}):	
CLKIN	+2.6 V to V_{DD} + 0.3 V 6/
All other inputs	+2.0 V to V_{DD} + 0.3 V 6/
Low-level input voltage range (V_{IL})	-0.3 V to 0.8 V 6/
Maximum high-level output current (I_{OH})	-300 µA
Maximum low-level output current (I_{OL})	+2 mA
Case operating temperature range (T_C)	-55°C to +125°C 7/

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at https://www.jedec.org)

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values are with respect to V_{SS}.

3/ This value calculated for the C32-40. Actual operating power is less. This value was obtained under specially produced worst-case test conditions which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external bus at the maximum rate possible. See normal (I_{DD}) current specification in table I.

4/ All input and output voltage levels are TTL compatible.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

6/ Maximum V_{IH} and minimum V_{IL} are not production tested.

7/ T_C MAX at maximum rated operating conditions at any point on case. T_C MIN at initial (time zero) power-up.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Block diagram. The block diagram shall be as specified on figure 3.

3.5.4 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as specified on figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V_{DD}	Temperature, T_C	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	I_{OH} = -300 µA	5.0 V	25°C	All	3.0		V
			4.75 V	-55°C to +125°C		2.4		
Low level output voltage	V_{OL}	I_{OL} = 2 mA	5.0 V	25°C			0.3	V
			4.75 V	-55°C to +125°C			0.8	
High impedance state output current	I_{OZ}		5.25 V	-55°C to +125°C		-20	20	µA
Input current	I_I	V_I = 0 to V_{DD}	2/	-55°C to +125°C		-10	10	µA
Supply current	I_{DD}	f_X = 50 MHz	5.25 V	25°C			200	mA
				-55°C to +125°C			425	
		f_X = 60 MHz	5.25 V	25°C			225	
				-55°C to +125°C			475	
		Standby, IDLE2, CLKIN shut off	5.0 V	25°C			50	µA
Input capacitance	C_I	CLKIN	2/	-55°C to +125°C			25	pF
		All other inputs 3/					15	
Output capacitance	C_O	3/	2/	-55°C to +125°C			20	
Timing for CLKIN [Q=$t_{c(CI)}$]								
Fall time, CLKIN 3/ 4/	$t_{f(CI)}$	See figure 4, 1	2/	-55°C to +125°C	1		5	ns
					2		4	
Pulse duration, CLKIN low 4/	$t_{w(CIL)}$	See figure 4, 2 Q = min			1	7		ns
					2	6		
Pulse duration, CLKIN high 4/	$t_{w(CIH)}$	See figure 4, 3 Q = min			1	8		ns
					2	6		
Rise time, CLKIN 3/ 4/	$t_{r(CI)}$	See figure 4, 4			1		5	ns
					2		4	
Cycle time, CLKIN 4/	$t_{c(CI)}$	See figure 4, 5			1	20	303	ns
					2	16.67	303	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{DD}	Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Switching characteristics for H1 and H3 over recommended operating conditions (unless otherwise noted)								
Fall time, H1/H3	$t_{f(H)}$	See figure 4, 6	2/	-55°C to +125°C	1		3	ns
					2		3	
Pulse duration, H1/H3 low	$t_{w(HL)}$	See figure 4, 7			1	Q-5		ns
					2	Q-4		
Pulse duration, H1/H3 high	$t_{w(HH)}$	See figure 4, 8			1	Q-6		ns
					2	Q-5		
Rise time, H1/H3	$t_{r(H)}$	See figure 4, 9			1		3	ns
					2		3	
Delay time, H1/H3 low to H1/H3 high	$t_{d(HL-HH)}$	See figure 4, 9.1			1	0 3/	4	ns
					2	0 3/	4	
Cycle time, H1/H3	$t_{c(H)}$	See figure 4, 10			1	40	606	ns
					2	33.33	606	
Memory-read-cycle and memory-write-cycle timing ($\overline{\text{STRBx}}$)								
Delay time, H1 low to $\overline{\text{STRBx}}$ low	$t_{d(H1L-SL)}$	See figure 4, 11	2/	-55°C to +125°C	1	0 3/	9	ns
					2	0 3/	7	
Delay time, H1 low to $\overline{\text{STRBx}}$ high	$t_{d(H1L-SH)}$	See figure 4, 12			1	0 3/	9	ns
					2	0 3/	7	
Delay time, H1 high to R/$\overline{\text{W}}$ low (read)	$t_{d(H1H-RWL)}$	See figure 4, 13			1	0 3/	9	ns
					2	0 3/	8	
Delay time, H1 low to A valid	$t_{d(H1L-A)}$	See figure 4, 14			1	0 3/	9	ns
					2	0 3/	7	
Setup time, D valid before H1 low (read)	$t_{su(D)R}$	See figure 4, 15			1	10		ns
					2	10		
Hold time, D after H1 low (read)	$t_{h(D)R}$	See figure 4, 16			1	0		ns
					2	0		
Setup time, $\overline{\text{RDY}}$ before H1 low	$t_{d(RDY)}$	See figure 4, 17			1	19		ns
					2	17		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{DD}	Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Hold time, $\overline{RDY}$ after H1 low	$t_{h(RDY)}$	See figure 4, 18	2/	-55°C to +125°C	1	0		ns
					2	0		
Delay time, H1 high to R/$\overline{W}$ high (write)	$t_{d(H1H-RWH)}$	See figure 4, 19			1		9	ns
					2		8	
Valid time, D after H1 low (write)	$t_{v(D)W}$	See figure 4, 20			1		14	ns
					2		12	
Hold time, D after H1 high (write) 4/	$t_{h(D)W}$	See figure 4, 21			1	0 3/		ns
					2	0 3/		
Delay time, H1 high to A valid on back-to-back write cycles	$t_{d(H1H-A)}$	See figure 4, 22			1		9	ns
					2		8	
Memory-read-cycle timing using $\overline{IOSTRB}$								
Delay time, H3 low to $\overline{IOSTRB}$ low	$t_{d(H3L-IOSL)}$	See figure 4, 11.1	2/	-55°C to +125°C	1	0 3/	9	ns
					2	0 3/	8	
Delay time, H3 low to $\overline{IOSTRB}$ high	$t_{d(H3L-IOSH)}$	See figure 4, 12.1			1	0 3/	9	ns
					2	0 3/	8	
Delay time, H1 low to R/$\overline{W}$ high	$t_{d(H1L-RWL)}$	See figure 4, 13.1			1	0 3/	9	ns
					2	0 3/	8	
Delay time, H1 low to A valid	$t_{d(H1L-A)}$	See figure 4, 14.1			1	0 3/	9	ns
					2	0 3/	8	
Setup time, D before H1 high	$t_{su(D)R}$	See figure 4, 15.1			1	10		ns
					2	9		
Hold time, D after H1 high	$t_{h(D)R}$	See figure 4, 16.1			1	0		ns
					2	0		
Setup time, $\overline{RDY}$ before H1 high	$t_{su(RDY)}$	See figure 4, 17.1			1	8		ns
					2	7		
Hold time, $\overline{RDY}$ after H1 high	$t_{h(RDY)}$	See figure 4, 18.1			1	0		ns
					2	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{DD}	Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Memory-write-cycle timing using $\overline{\text{IOSTRB}}$								
Delay time, H1 low to R/$\overline{W}$ low	$t_{d(H1L-RWH)}$	See figure 4, 23	2/	-55°C to +125°C	1	0 3/	9	ns
					2	0 3/	8	
Valid time, D after H1 high	$t_{v(D)W}$	See figure 4, 24			1		14	ns
					2		12	
Hold time, D after H1 low	$t_{h(D)W}$	See figure 4, 25			1	0		ns
					2	0		
Timing for XF0 and XF1 when executing LDFI or LDII								
Delay time, H3 high to XF0 low	$t_{d(H3H-XF0L)}$	See figure 4, 38	2/	-55°C to +125°C	1		12	ns
					2		11	
Setup time, XF1 before H1 low	$t_{su(XF1)}$	See figure 4, 39			1	9		ns
					2	8		
Hold time, XF1 after H1 low	$t_{h(XF1)}$	See figure 4, 40			1	0		ns
					2	0		
Timing for XF0 when executing STFI or STII 5/								
Delay time, H3 high to XF0 high	$t_{d(H3H-XF0H)}$	See figure 4, 41	2/	-55°C to +125°C	1		12	ns
					2		11	
Timing for XF0 and XF1 when executing SIGI								
Delay time, H3 high to XF0 low	$t_{d(H3H-XF0L)}$	See figure 4, 41.1	2/	-55°C to +125°C	1		12	ns
					2		11	
Delay time, H3 high to XF0 high	$t_{d(H3H-XF0H)}$	See figure 4, 42			1		12	ns
					2		11	
Setup time, XF1 before H1 low	$t_{su(XF1)}$	See figure 4, 43			1	9		ns
					2	8		
Hold time, XF1 after H1 low	$t_{h(XF1)}$	See figure 4, 44			1	0		ns
					2	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{DD}	Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Timing for loading XF register when configured as an output pin								
Valid time, H3 high to XF valid	$t_{v(H3H-XF)}$	See figure 4, 45	2/	-55°C to +125°C	1		12	ns
					2		11	
Timing of XF changing from output to input mode								
Hold time, XF after H3 high 3/	$t_{h(H3H-XF01)}$	See figure 4, 46	2/	-55°C to +125°C	1		12	ns
					2		11	
Setup time, XF before H1 low	$t_{su(XF)}$	See figure 4, 47			1	9		ns
					2	8		
Hold time, XF after H1 low	$t_{h(XF)}$	See figure 4, 48			1	0		ns
					2	0		
Timing of XF changing from input to output mode								
Delay time, H3 high to XF switching from input to output	$t_{d(H3H-XFIO)}$	See figure 4, 49	2/	-55°C to +125°C	1		17	ns
					2		15	
Timing for $\overline{\text{RESET}}$ [Q = $t_{c(CI)}$]								
Setup time, $\overline{\text{RESET}}$ before CLKIN low	$t_{su(RESET)}$	See figure 4, 50	2/	-55°C to +125°C	1	10	Q 3/	ns
					2	7	Q 3/	
Delay time, CLKIN high to H1 high	$t_{d(CLKINH-H1H)}$	See figure 4, 51			1	2	10	ns
					2	2	10	
Delay time, CLKIN high to H1 low	$t_{d(CLKINH-H1L)}$	See figure 4, 52			1	2	10	ns
					2	2	10	
Setup time, $\overline{\text{RESET}}$ high before H1 low and after 10 H1 clock cycles	$t_{su(RESETH-H1L)}$	See figure 4, 53			1	7		ns
					2	6		
Delay time, CLKIN high to H3 low	$t_{d(CLKINH-H3L)}$	See figure 4, 54			1	2	10	ns
					2	2	10	
Delay time, CLKIN high to H3 high	$t_{d(CLKINH-H3H)}$	See figure 4, 55			1	2	10	ns
					2	2	10	
Disable time, H1 high to D in high-impedance state 3/	$t_{dis(H1H-D)}$	See figure 4, 56			1		12	ns
					2		11	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{DD}	Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Timing for $\overline{\text{RESET}}$ [Q = $t_{c(CI)}$] – Continued								
Disable time, H3 low to A in high-impedance state 3/	$t_{dis(H3HL-A)}$	See figure 4, 57	2/	-55°C to +125°C	1		9	ns
					2		9	
Delay time, H3 high to control signals high 3/	$t_{d(H3H-CONTROLH)}$	See figure 4, 58.1			1		8	ns
					2		7	
Delay time, H1 high to R/$\overline{W}$ high 3/	$t_{d(H1H-RWH)}$	See figure 4, 58.2			1		8	ns
					2		7	
Delay time, H1 high to $\overline{\text{IACK}}$ high 3/	$t_{d(H1H-IACKH)}$	See figure 4, 59			1		8	ns
					2		7	
Disable time, $\overline{\text{RESET}}$ low to asynchronously reset signals in high impedance 3/	$t_{dis(RESETL-ASYNCH)}$	See figure 4, 60			1		17	ns
					2		14	
Timing for $\overline{\text{INT3}}$ - $\overline{\text{INT0}}$ interrupt response [P = $t_{C(H)}$]								
Setup time, $\overline{\text{INT3}}$ - $\overline{\text{INT0}}$ before H1 low	$t_{su(INT)}$	See figure 4, 61	2/	-55°C to +125°C	1		10	ns
					2		8	
Pulse duration of interrupt to assure only one interrupt seen for level-triggered interrupts	$t_{w(INT)}$	See figure 4, 62.1			1	P	2P 3/	ns
					2	P	2P 3/	
Pulse duration, of interrupt for edge-triggered interrupts 3/	$t_{w(INT)}$	See figure 4, 62.2			1	P		ns
					2	P		
Timing for $\overline{\text{IACK}}$ 6/ 7/								
Delay time, H1 high to $\overline{\text{IACK}}$ low	$t_{d(H1H-IACKL)}$	See figure 4, 63	2/	-55°C to +125°C	1		7	ns
					2		6	
Delay time, H1 high to $\overline{\text{IACK}}$ high	$t_{d(H1H-IACKH)}$	See figure 4, 64			1		7	ns
					2		6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions		V_{DD}	Temperature, T_C	Device type	Limits		Unit
							Min	Max	
Serial port timing [P = $t_{c(H)}$]									
Delay time, H1 high to internal CLKX/R high/low	$t_{d(H1-SCK)}$	See figure 4, 65		2/	-55°C to +125°C	1		10	ns
						2		8	
Cycle time, CLKX/R	$t_{c(SCK)}$	See figure 4, 66	CLKX/R ext			1	2.6P		ns
						2	2.6P		
			CLKX/R int			1	2P	$(2^{32})P$	ns
						2	2P	$(2^{32})P$	
Pulse duration, CLKX/R high/low	$t_{w(SCK)}$	See figure 4, 67	CLKX/R ext			1	P+10		ns
						2	P+10		
			CLKX/R int			1	$[t_{c(SCK)}/2]$-5	$[t_{c(SCK)}/2]$+5	ns
						2	$[t_{c(SCK)}/2]$-5	$[t_{c(SCK)}/2]$+5	
Rise time, CLKX/R	$t_{r(SCK)}$	See figure 4, 68				1		6	ns
						2		5	
Fall time, CLKX/R	$t_{f(SCK)}$	See figure 4, 69				1		6	ns
						2		5	
Delay time, CLKX to DX valid	$t_{d(DX)}$	See figure 4, 70	CLKX ext			1		24	ns
						2		20	
			CLKX int			1		16	ns
						2		15	
Setup time, DR before CLKR low	$t_{su(DR)}$	See figure 4, 71	CLKR ext			1	9		ns
						2	8		
			CLKR int			1	17		ns
						2	15		
Hold time, DR from CLKR low	$t_{h(DR)}$	See figure 4, 72	CLKR ext			1	7		ns
						2	6		
			CLKR int			1	0		ns
						2	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions		V_{DD}	Temperature, T_C	Device type	Limits		Unit
							Min	Max	
Serial port timing [P = $t_{c(H)}$] - Continued									
Delay time, CLKX to internal FSX high/low	$t_{d(FSX)}$	See figure 4, 73	CLKX ext	2/	-55°C to +125°C	1		22	ns
						2		20	
			CLKX int			1		15	ns
						2		14	
Setup time, FSR before CLKR low	$t_{su(FSR)}$	See figure 4, 74	CLKR ext			1	7		ns
						2	6		
			CLKR int			1	7		ns
						2	6		
Hold time, FSX/R input from CLKX/R low	$t_{h(FS)}$	See figure 4, 75	CLKX/R ext			1	7		ns
						2	6		
			CLKX/R int			1	0		ns
						2	0		
Setup time, external FSX before CLKX 3/	$t_{su(FSX)}$	See figure 4, 76	CLKX ext			1	8-P	$[t_{c(SCK)}/2]$-10	ns
						2	8-P	$[t_{c(SCK)}/2]$-10	
			CLKX int			1	22-P	$t_{c(SCK)}/2$	ns
						2	22-P	$t_{c(SCK)}/2$	
Delay time, CLKX to first DX bit, FSX precedes CLKX high 3/	$t_{d(CH-DX)V}$	See figure 4, 77	CLKX ext			1		24	ns
						2		20	
			CLKX int			1		14	ns
						2		12	
Delay time, FSX to first DX bit, CLKX precedes FSX 3/	$t_{d(FSX-DX)V}$	See figure 4, 78				1		24	ns
						2		20	
Delay time, CLKX high to DX high impedance following last data bit 3/	$t_{d(DXZ)}$	See figure 4, 79				1		14	ns
						2		12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{DD}	Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Timing for $\overline{HOLD}$ / $\overline{HOLDA}$ [P = $t_{c(H)}$] 8/								
Setup time, $\overline{HOLD}$ before H1 low	$t_{su(HOLD)}$	See figure 4, 80	2/	-55°C to +125°C	1	10		ns
					2	8		
Valid time, $\overline{HOLDA}$ after H1 low	$t_{v(HOLDA)}$	See figure 4, 81			1	0 3/	7	ns
					2	0 3/	6	
Pulse duration, $\overline{HOLD}$ low	$t_{w(HOLD)}$	See figure 4, 82			1	2P		ns
					2	2P		
Pulse duration, $\overline{HOLDA}$ low 3/	$t_{w(HOLDA)}$	See figure 4, 83			1	P-5		ns
					2	P-5		
Delay time, H1 low to $\overline{STRBx}$ high for a $\overline{HOLD}$ 3/	$t_{d(H1L-SH)H}$	See figure 4, 84			1	0	7	ns
					2	0	6	
Delay time, H1 high to $\overline{IOSTRB}$ high for a $\overline{HOLD}$ 3/	$t_{d(H1H-IOS)H}$	See figure 4, 84.1			1	0	7	ns
					2	0	6	
Disable time, H1 low to $\overline{STRBx}$ or $\overline{IOSTRB}$ high impedance state 3/	$t_{dis(H1L-S)}$	See figure 4, 85			1	0	8	ns
					2	0	7	
Enable time, H1 low to $\overline{STRBx}$ or $\overline{IOSTRB}$ active 3/	$t_{en(H1L-S)}$	See figure 4, 86			1	0	7	ns
					2	0	6	
Disable time, H1 low to R/$\overline{W}$ in the high-impedance state 3/	$t_{dis(H1L-RW)}$	See figure 4, 87			1	0	8	ns
					2	0	7	
Enable time, H1 low to R/$\overline{W}$ (active) 3/	$t_{en(H1L-RW)}$	See figure 4, 88			1	0	7	ns
					2	0	6	
Disable time, H1 low to A high-impedance state 3/	$t_{dis(H1L-A)}$	See figure 4, 89			1	0	8	ns
					2	0	7	
Enable time, H1 low to A valid 3/	$t_{en(H1L-A)}$	See figure 4, 90			1	0	12	ns
					2	0	11	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V_{DD}	Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Timing for $\overline{HOLD}$ / $\overline{HOLDA}$ [P = $t_{c(H)}$] – Continued 8/								
Disable time, H1 high to D disabled in the high-impedance state 3/	$t_{dis(H1H-D)}$	See figure 4, 91	2/	-55°C to +125°C	1	0	8	ns
					2	0	7	
Timing for peripheral pin configured as general-purpose I/O								
Setup time, general-purpose input before H1 low	$t_{su(GPIOH1L)}$	See figure 4, 92	2/	-55°C to +125°C	1	9		ns
					2	8		
Hold time, general-purpose input after H1 low	$t_{h(GPIOH1L)}$	See figure 4, 93			1	0		ns
					2	0		
Delay time, general-purpose output after H1 high	$t_{d(GPIOH1H)}$	See figure 4, 94			1		10	ns
					2		8	
Timing for peripheral pin changing from general-purpose output to input mode								
Hold time, after H1 high 3/	$t_{h(H1H)}$	See figure 4, 95	2/	-55°C to +125°C	1		12	ns
					2		11	
Setup time, peripheral pin before H1 low	$t_{su(GPIOH1L)}$	See figure 4, 96			1	9		ns
					2	8		
Hold time, peripheral pin after H1 low	$t_{h(GPIOH1L)}$	See figure 4, 97			1	0		ns
					2	0		
Timing for peripheral pin changing from general-purpose input to output mode								
Delay time, H1 high to peripheral pin switching from input to output	$t_{d(GPIOH1H)}$	See figure 4, 98	2/	-55°C to +125°C	1		10	ns
					2		8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions		V_{DD}	Temperature, T_C	Device type	Limits		Unit
							Min	Max	
Timing for timer pin [P = $t_{c(H)}$]									
Setup time, TCLK external before H1 low 9/	$t_{su(TCLKH1L)}$	See figure 4, 99		2/	-55°C to +125°C	1	8		ns
						2	6		
Hold time, TCLK external after H1low 9/	$t_{h(TCLKH1L)}$	See figure 4, 100				1	0		ns
						2	0		
Delay time, H1 high to TCLK internal valid	$t_{d(TCLKH1H)}$	See figure 4, 101				1		9	ns
						2		8	
Cycle time, TCLK cycle time 10/	$t_{c(TCLK)}$	See figure 4, 102	TCLK external 3/			1	2.6P		ns
						2	2.6P		
			TCLK internal			1	2P	$(2^{32})P$ 3/	ns
						2	2P	$(2^{32})P$ 3/	
Pulse duration, TCLK high/low 10/	$t_{w(TCLK)}$	See figure 4, 103	TCLK external 3/			1	P+10		ns
						2	P+10		
			TCLK internal			1	$[t_{c(TCLK)}/2]$-5	$[t_{c(TCLK)}/2]$+5	ns
						2	$[t_{c(TCLK)}/2]$-5	$[t_{c(TCLK)}/2]$+5	
Timing for $\overline{SHZ}$ pin [Q = $t_{c(CI)}$]									
Disable time, $\overline{SHZ}$ low to all O, I/O pins in the high-impedance state 3/	$t_{dis(SHZ)}$	See figure 4, 104		2/	-55°C to +125°C	1	0	2Q	ns
						2	0	2Q	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ $4.75\ V \leq V_{DD} \leq 5.25\ V$

3/ This value is not production tested.

4/ Minimum CLKIN high pulse duration at 3.3 MHz is 10ns.

5/ XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store is not driven until the store can execute.

6/ The $\overline{\text{IACK}}$ output is active for the entire duration of the bus cycle and is extended if the bus cycle utilizes wait states.

7/ The $\overline{\text{IACK}}$ output goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction. Because of pipeline conflicts, $\overline{\text{IACK}}$ remains low for one cycle even if the decode phase of the IACK instruction is extended.

8/ $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur. The NOHOLD bit of the primary-bit-control register overwrites the $\overline{\text{HOLD}}$ signal.

9/ This timing parameter is applicable for a synchronous input clock.

10/ This timing parameter is applicable for an asynchronous input clock.

Case X

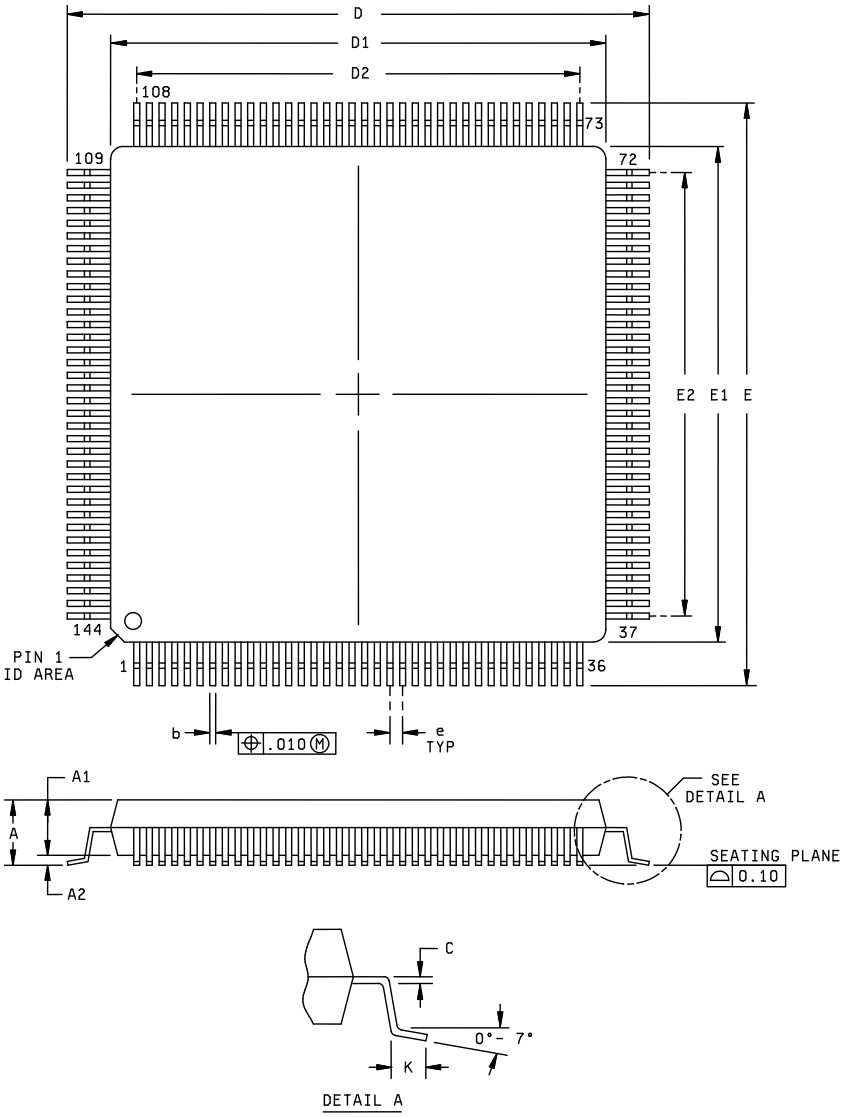


FIGURE 1. Case outlines.

Case X

	Millimeters	
Dimension	Min	Max
A		4.10
A1	3.20	3.60
A2	0.25	
b	0.22	0.38
C	0.16	
D/E	30.95	31.45
D1/E1	27.80	28.20
D2/E2	22.75	
e	0.65	
K	0.73	1.03

FIGURE 1. Case outlines - Continued.

Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DR0	30	A17	59	DV_{DD}	88	IV_{SS}	117	$\overline{RDY}$
2	DV_{DD}	31	A16	60	D31	89	D11	118	IV_{SS}
3	FSR0	32	A15	61	D30	90	DV_{DD}	119	$\overline{IOSTRB}$
4	CLKR0	33	A14	62	D29	91	D10	120	$\overline{STRB0\_B3}$ /A_{-1}
5	CLKX0	34	A13	63	D28	92	CV_{SS}	121	$\overline{STRB0\_B2}$ /A_{-2}
6	FSX0	35	CV_{SS}	64	D27	93	DV_{SS}	122	$\overline{STRB0\_B1}$
7	DX0	36	DV_{SS}	65	D26	94	V_{SSL}	123	$\overline{STRB0\_B0}$
8	IV_{SS}	37	NC	66	IV_{SS}	95	V_{SSL}	124	V_{DDL}
9	$\overline{SHZ}$	38	A12	67	D25	96	D9	125	V_{DDL}
10	TCLK0	39	DV_{DD}	68	DV_{DD}	97	D8	126	$\overline{STRB1\_B3}$ /A_{-1}
11	TCLK1	40	A11	69	D24	98	D7	127	V_{SSL}
12	DV_{DD}	41	A10	70	D23	99	D6	128	$\overline{STRB1\_B2}$ /A_{-2}
13	EMU3	42	A9	71	D22	100	D5	129	DV_{DD}
14	EMU2	43	A8	72	NC	101	D4	130	$\overline{STRB1\_B1}$
15	V_{DDL}	44	A7	73	CV_{SS}	102	DV_{DD}	131	$\overline{STRB1\_B0}$
16	V_{DDL}	45	A6	74	DV_{SS}	103	D3	132	R/$\overline{W}$
17	EMU1	46	DV_{DD}	75	D21	104	D2	133	PRGW
18	EMU2	47	A5	76	D20	105	D1	134	$\overline{RESET}$
19	V_{SSL}	48	A4	77	D19	106	D0	135	CV_{SS}
20	MCBL/$\overline{MP}$	49	A3	78	D18	107	H1	136	DV_{SS}
21	CV_{SS}	50	V_{DDL}	79	DV_{DD}	108	H3	137	XF0
22	DV_{SS}	51	V_{DDL}	80	D17	109	NC	138	XF1
23	A23	52	A2	81	D16	110	V_{SUBS}	139	$\overline{IACK}$
24	A22	53	CV_{SS}	82	D15	111	CV_{SS}	140	$\overline{INT0}$
25	A21	54	DV_{SS}	83	D14	112	DV_{SS}	141	$\overline{INT1}$
26	A20	55	A1	84	D13	113	CLKIN	142	$\overline{INT2}$
27	A19	56	V_{SSL}	85	V_{DDL}	114	$\overline{HOLDA}$	143	$\overline{INT3}$
28	A18	57	V_{SSL}	86	V_{DDL}	115	$\overline{HOLD}$	144	NC
29	DV_{DD}	58	A0	87	D12	116	DV_{DD}		

FIGURE 2. Terminal connections.

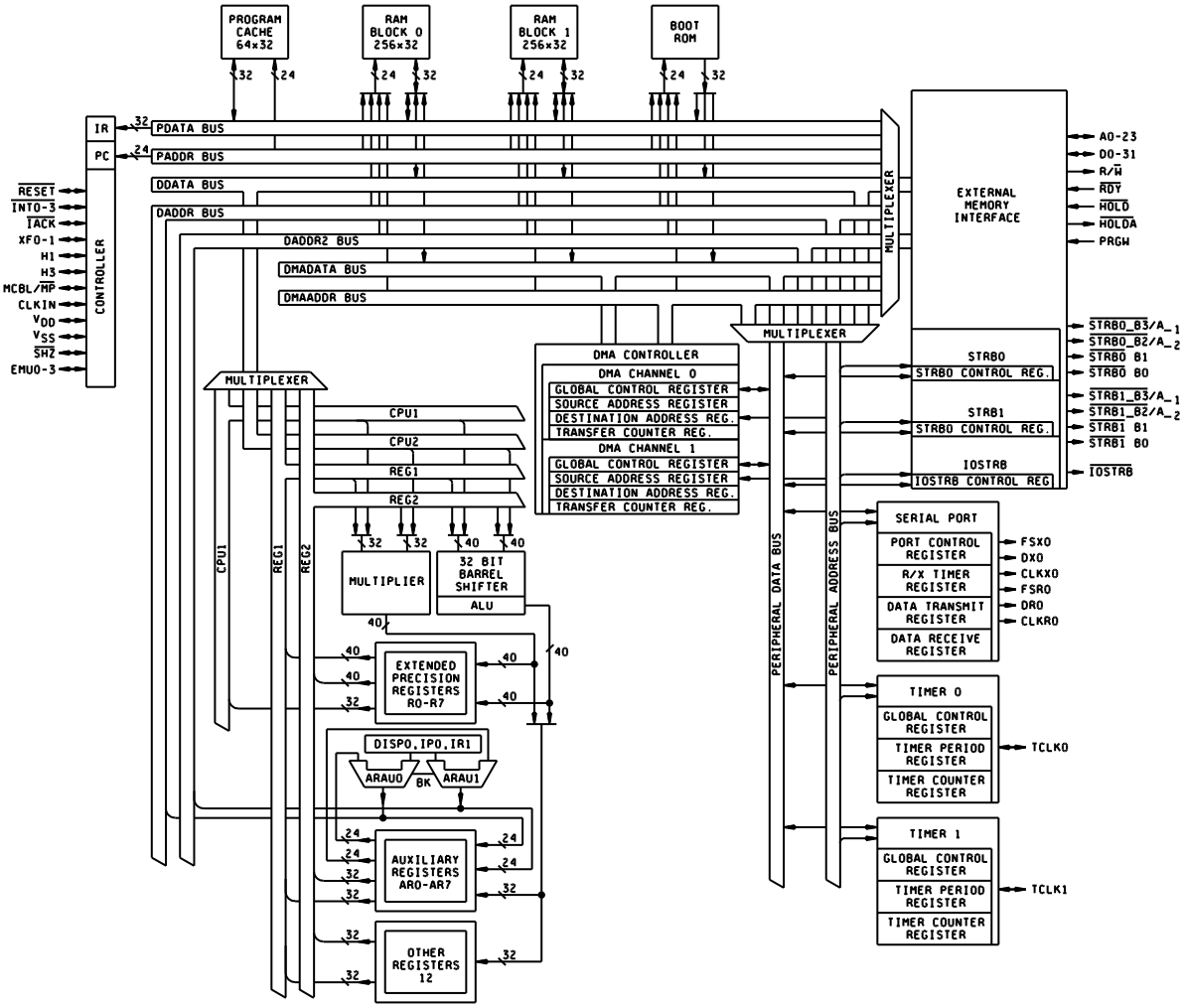


FIGURE 3. Block diagram.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
		REV C	PAGE 20

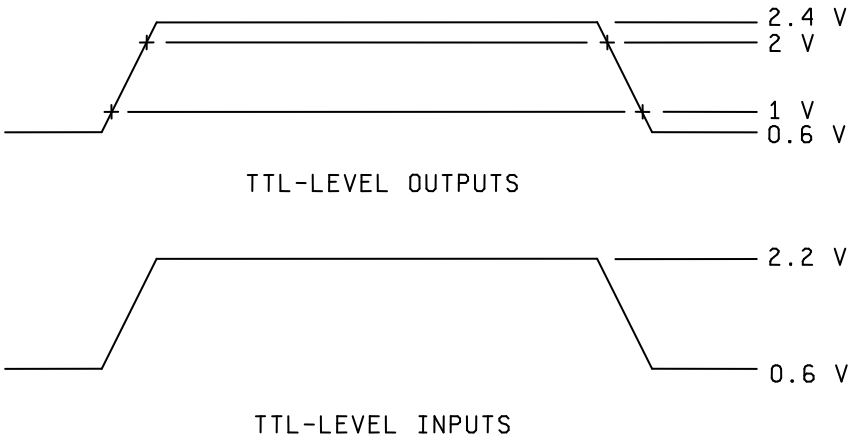
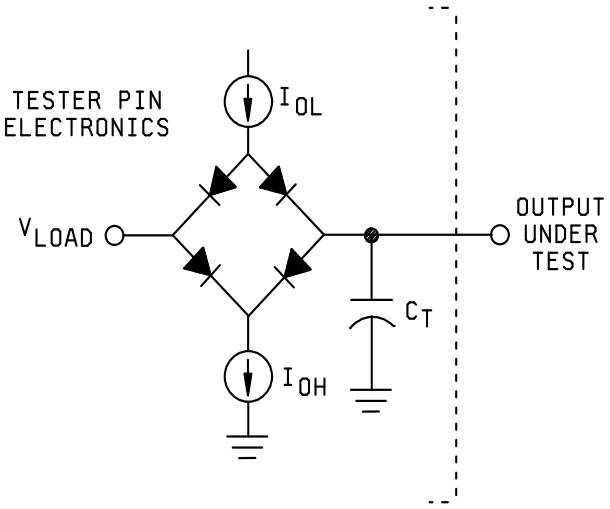
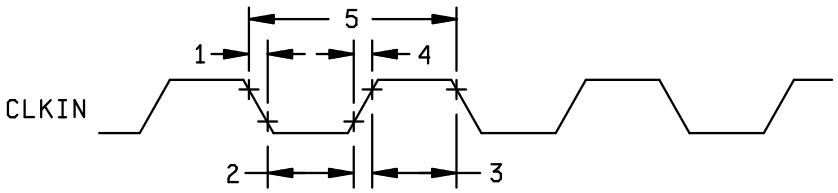


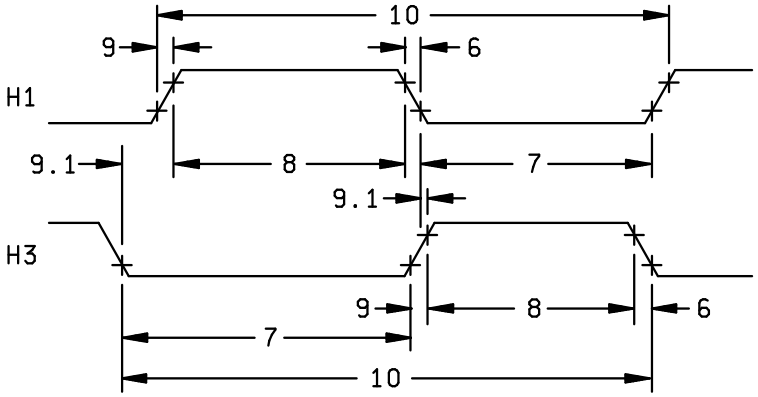
FIGURE 4. Load circuit and timing waveforms.



TEST LOAD CIRCUIT

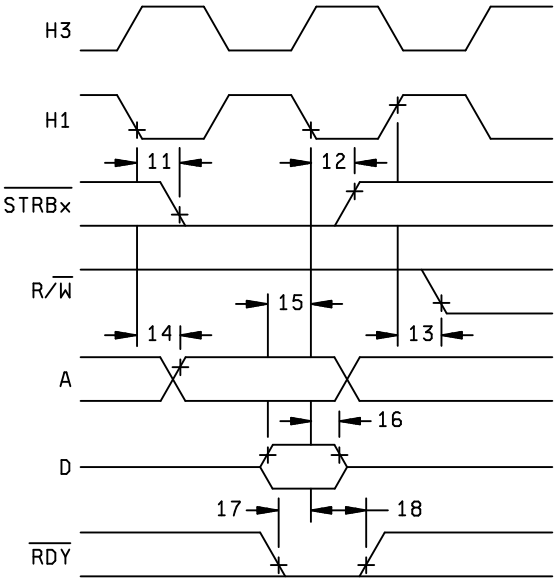


CLKIN TIMING

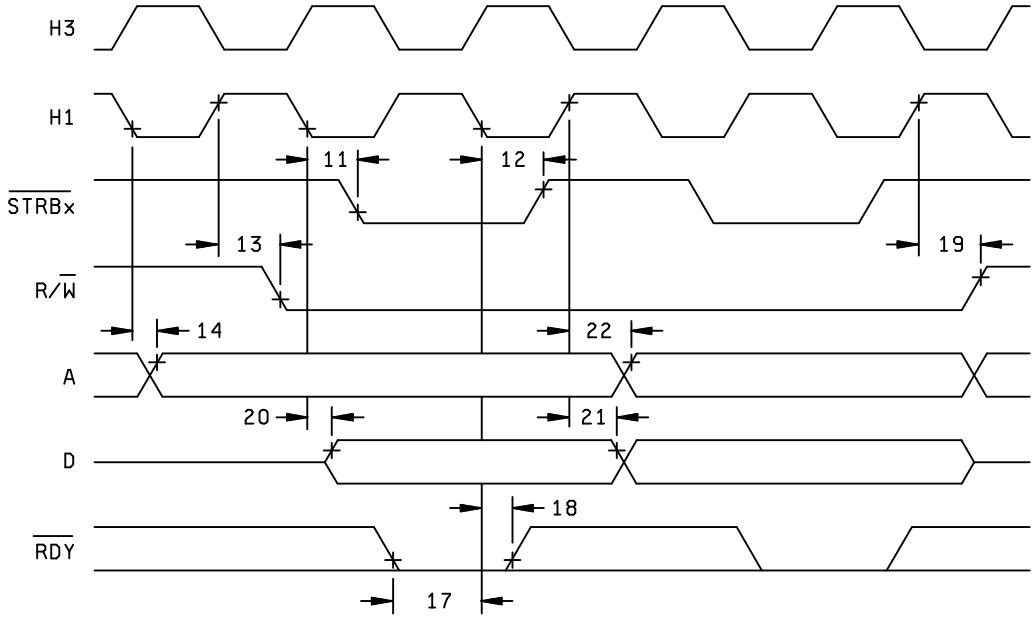


H1/H3 TIMING

FIGURE 4. Load circuit and timing waveforms - Continued.

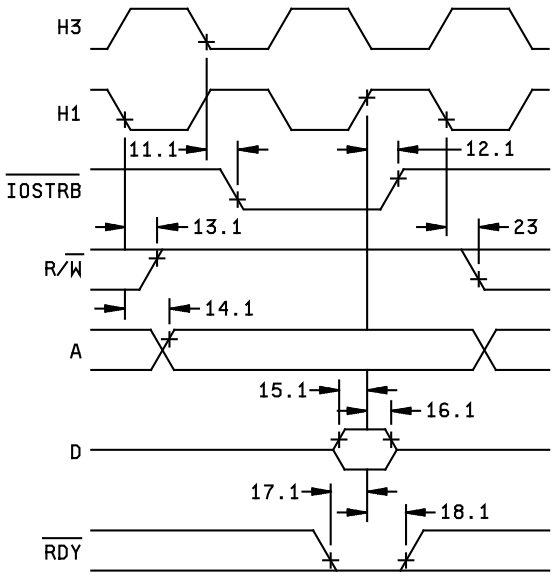


MEMORY-READ-CYCLE TIMING

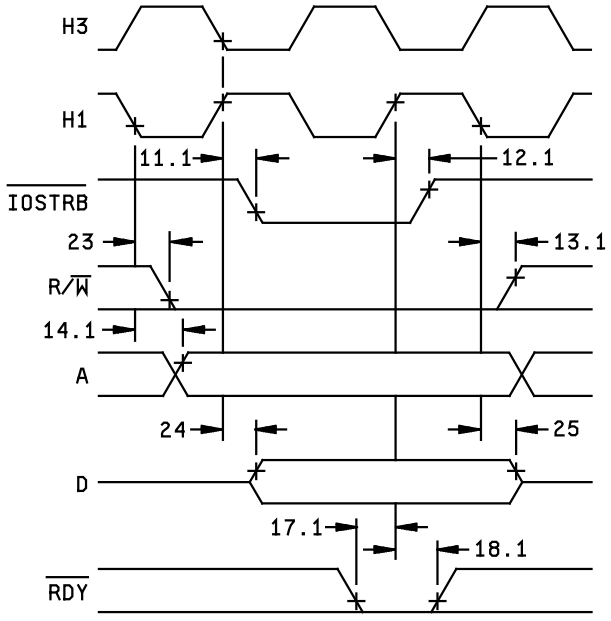


MEMORY-WRITE-CYCLE TIMING

FIGURE 4. Load circuit and timing waveforms - Continued.

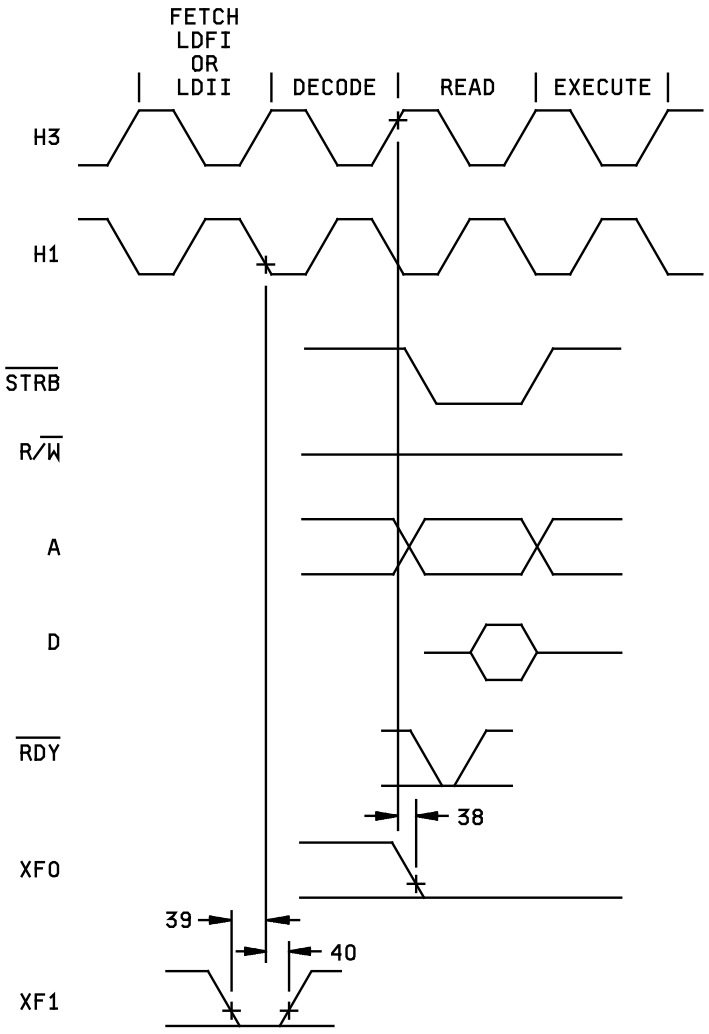


MEMORY-READ-CYCLE TIMING USING IOSTRB



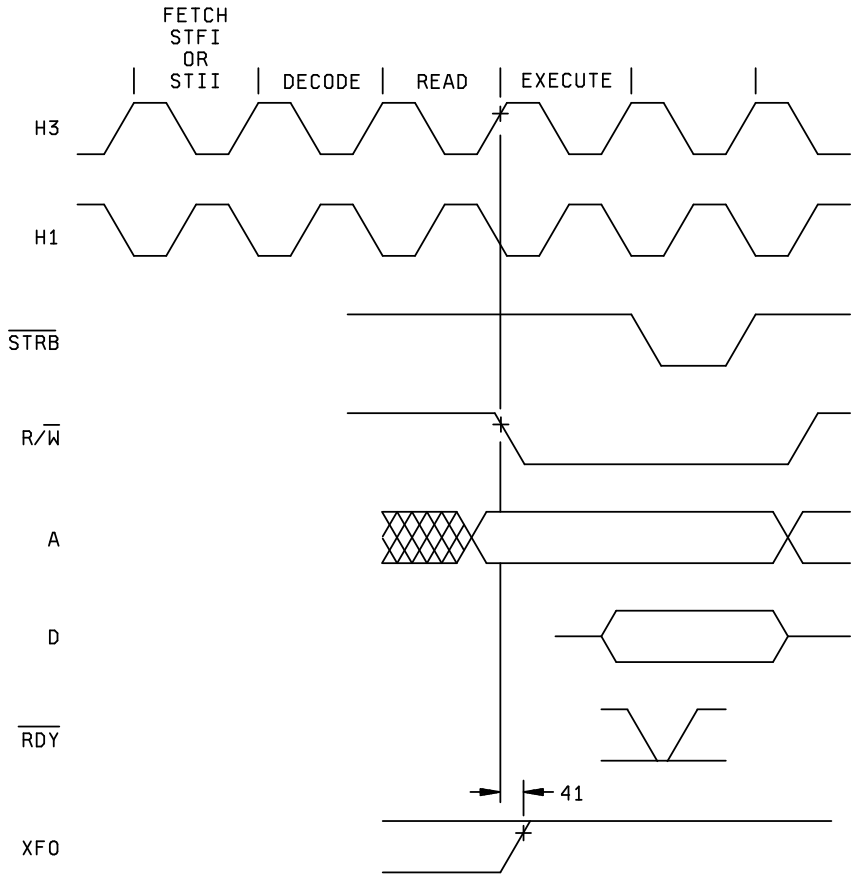
MEMORY-WRITE-CYCLE TIMING USING IOSTRB

FIGURE 4. Load circuit and timing waveforms - Continued.



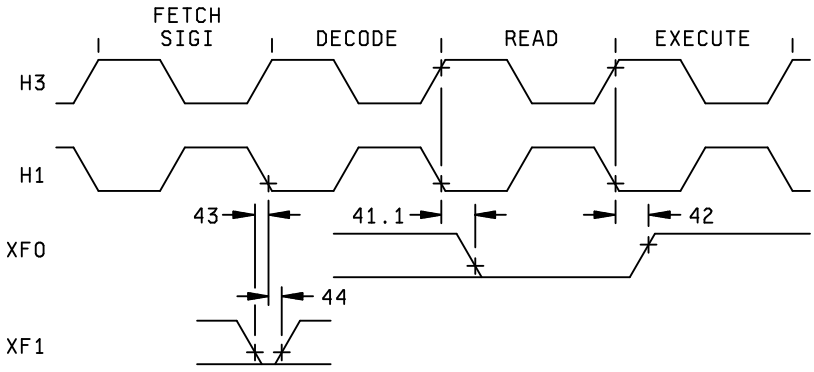
XFO AND XF1 WHEN EXECUTING LDFI OR LDII

FIGURE 4. Load circuit and timing waveforms - Continued.

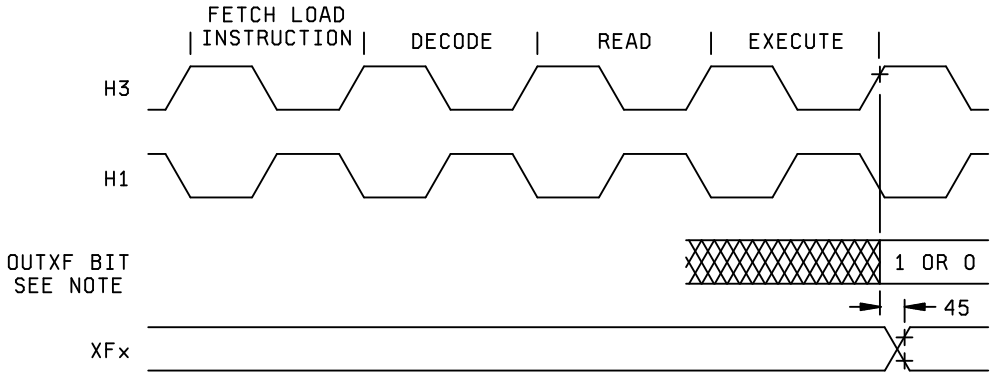


XFO WHEN EXECUTING A STFI OR STII

FIGURE 4. Load circuit and timing waveforms - Continued.



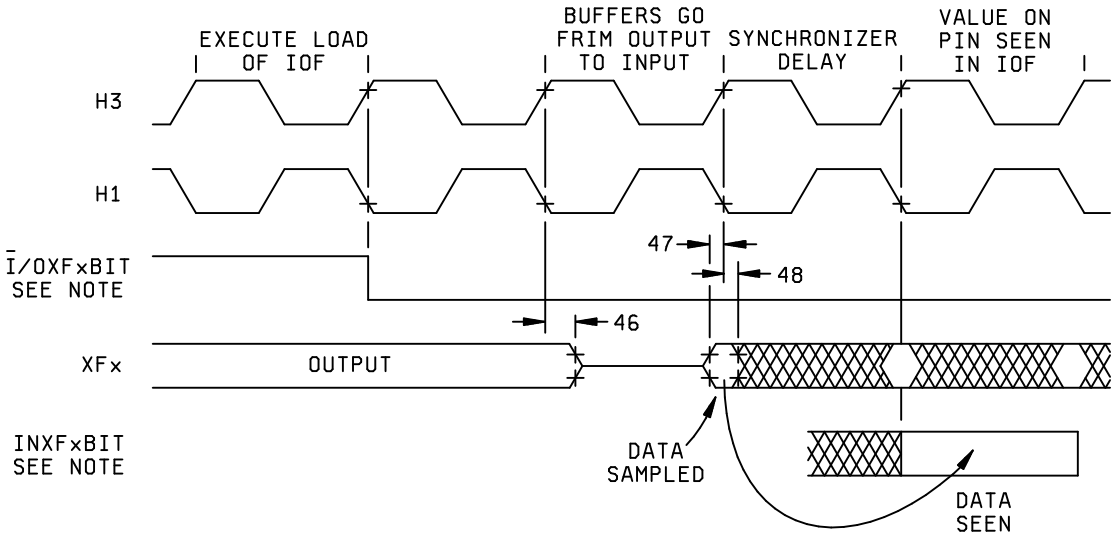
XFO AND XF1 WHEN EXECUTING SIGI



LOADING XF REGISTER WHEN CONFIGURED AS AN OUTPUT PIN

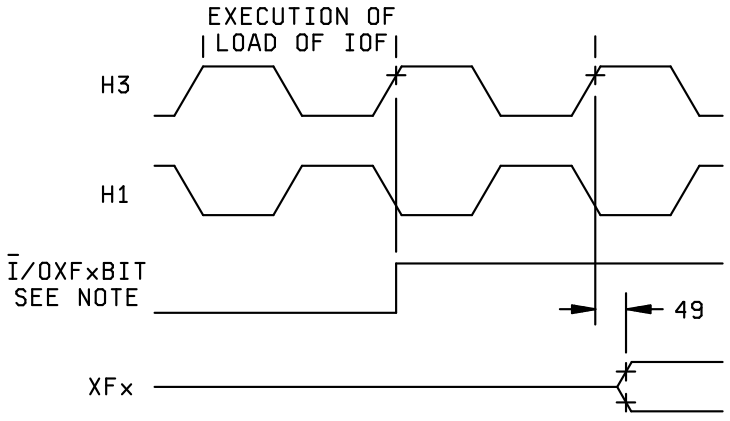
NOTE: OUTXFx represents either bit 2 or bit 6 of the IOF register.

FIGURE 4. Load circuit and timing waveforms - Continued.



CHANGE OF XF FROM OUTPUT TO INPUT MODE

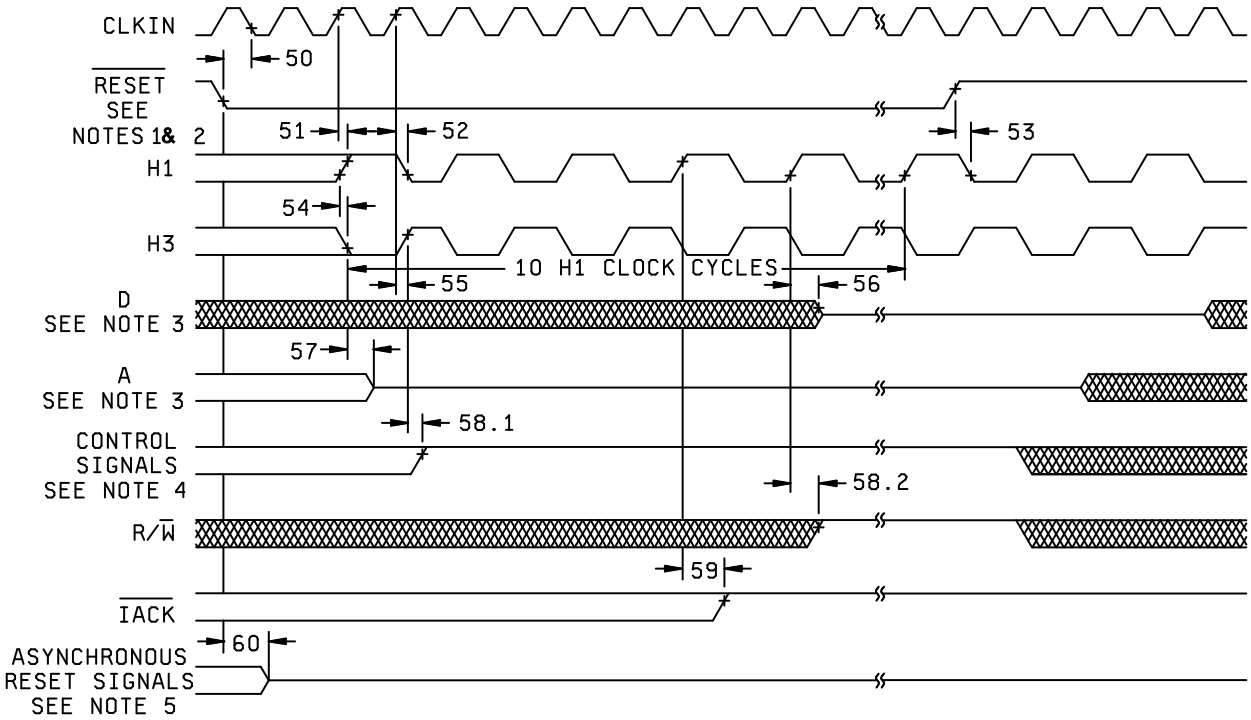
NOTE: Ī/OXFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register.



CHANGE OF XF FROM INPUT TO OUTPUT MODE

NOTE: Ī/OXFx represents either bit 1 or bit 5 of the IOF register.

FIGURE 4. Load circuit and timing waveforms - Continued.

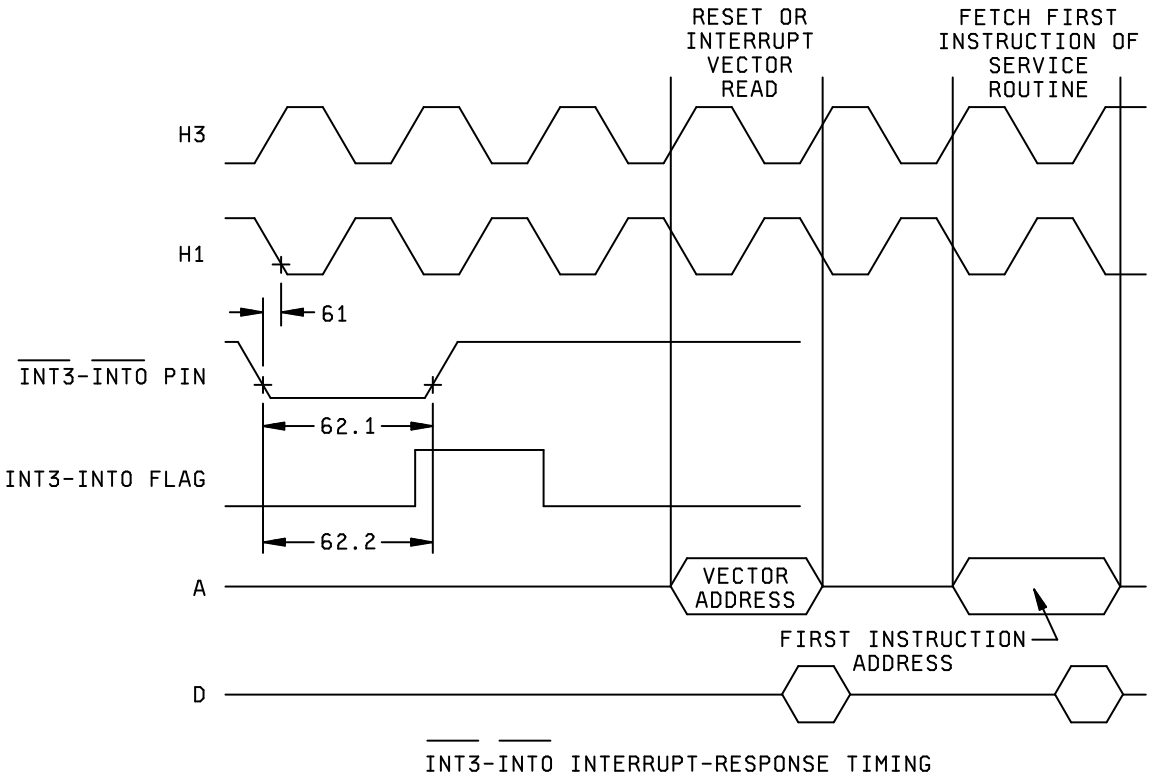


RESET TIMING

NOTES:

1. RESET is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.
2. The R/W output is placed in the high-impedance state during reset. It can be pulled high with a resistive pullup of 18-20 kΩ to prevent spurious writes.
3. In microprocessor mode (MCBL/MP = 0), reset vector is fetched twice with seven software wait states each. In microcomputer mode (MCBL/MP = 1), the reset vector is fetched two times, with no software wait states.
4. Control signals include STRBx and IOSTRB.
5. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLKx.

FIGURE 4. Load circuit and timing waveforms - Continued.



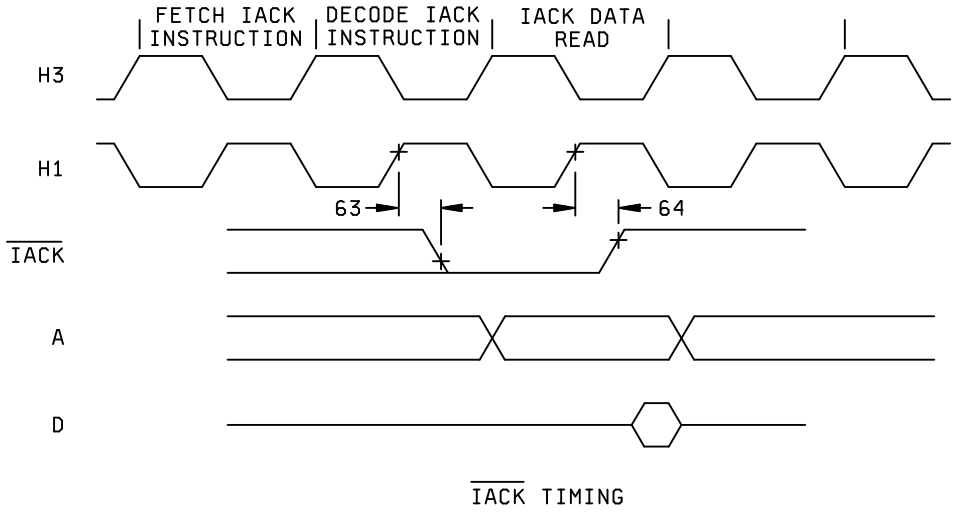
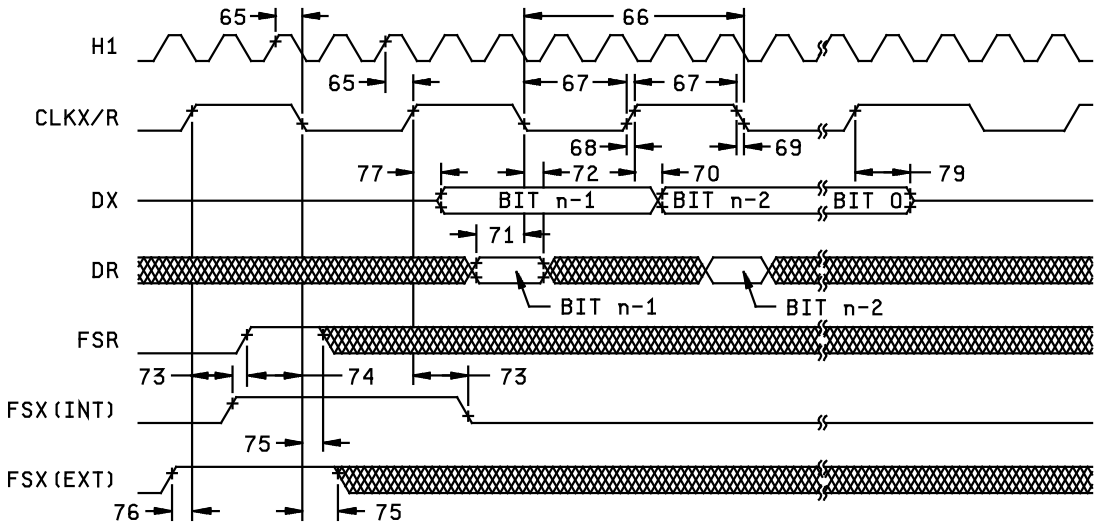
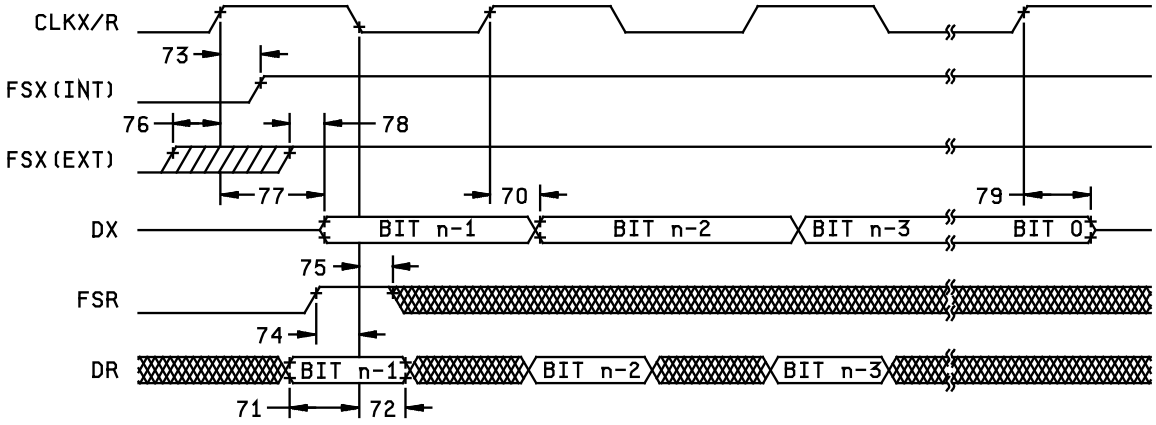


FIGURE 4. Load circuit and timing waveforms - Continued.



FIXED DATA-RATE-MODE TIMING

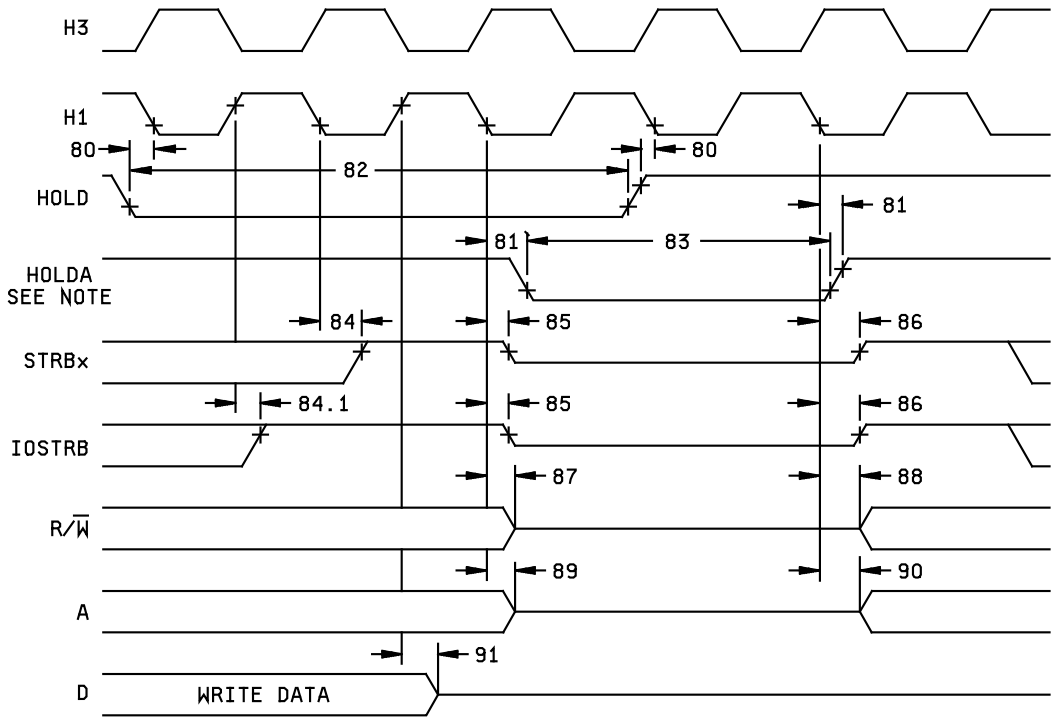
NOTES:
1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
2. Timing diagrams depend upon the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.



VARIABLE DATA-RATE-MODE TIMING

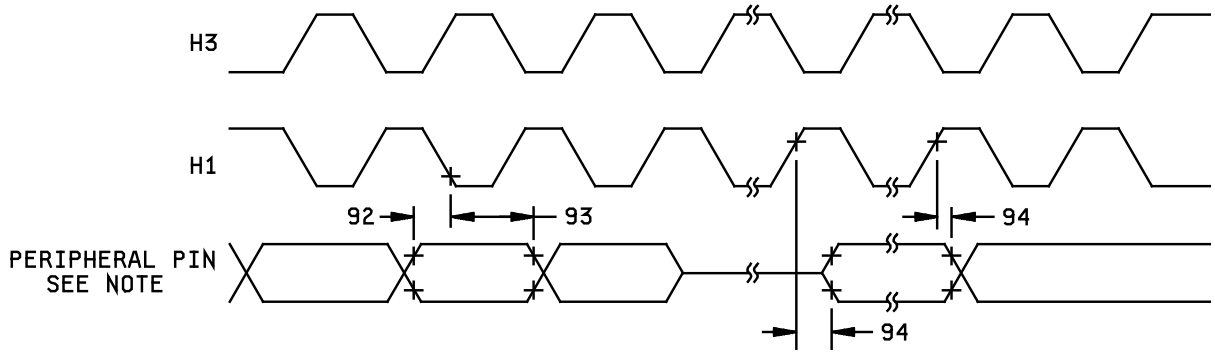
NOTES:
1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
2. Timing diagrams depend upon the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
3. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

FIGURE 4. Load circuit and timing waveforms - Continued.



$\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ TIMING

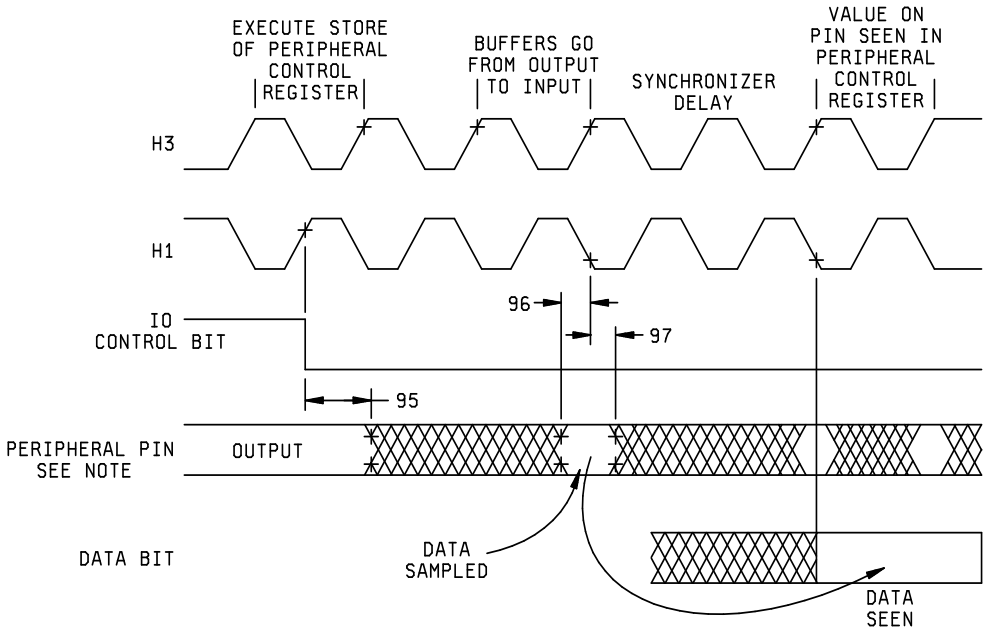
NOTE: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.



PERIPHERAL-PIN GENERAL-PURPOSE I/O TIMING

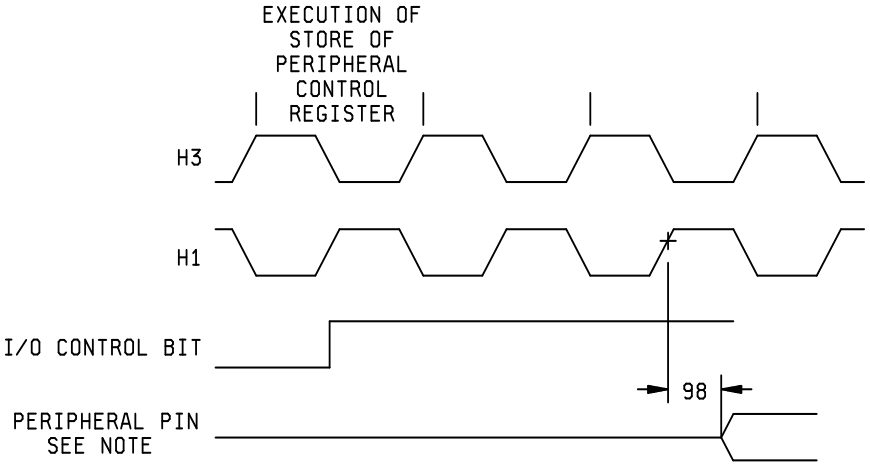
NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLKx. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

FIGURE 4. Load circuit and timing waveforms - Continued.



CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE OUTPUT TO INPUT-MODE TIMING

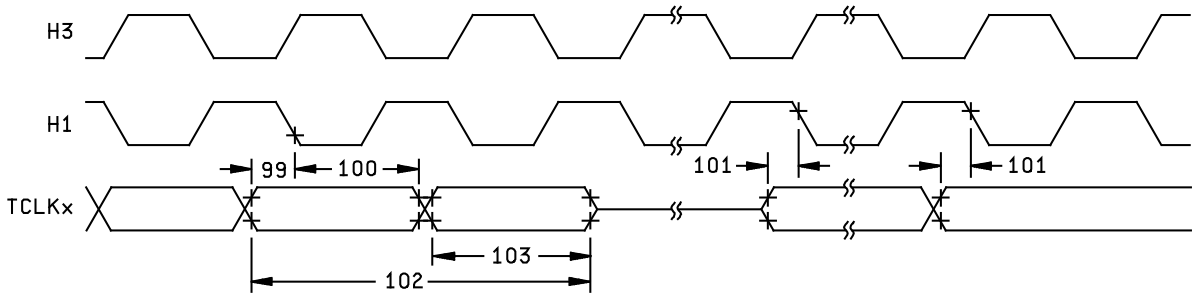
NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLKx. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.



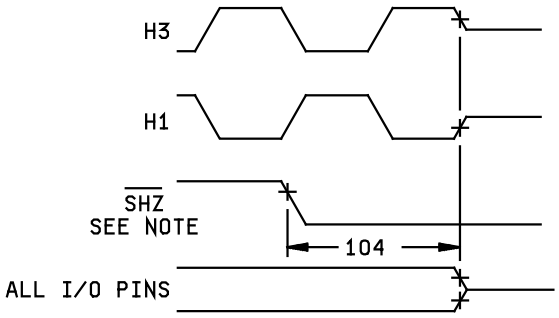
CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE INPUT TO OUTPUT-MODE TIMING

NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLKx. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

FIGURE 4. Load circuit and timing waveforms - Continued.



TIMING FOR TIMER PIN



$\overline{SHZ}$ PIN TIMING

NOTE: Enabling $\overline{SHZ}$ destroys the device register and memory contents. Assert $\overline{SHZ}$ = 1 and reset the device to restore it to a known condition.

FIGURE 4. Load circuit and timing waveforms - Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03616-01XE	01295	SM320C32PCMM50EP	SM320C32-50EP
V62/03616-02XE	01295	SM320C32PCMM60EP	SM320C32-60EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243