REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	Add device 02. Add case outline Y. Update boilerplate to current revision. - CFS	07-02-22	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	12-06-04	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-06-25	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES			**REV**		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
			PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	**PREPARED BY** RICK OFFICER		**DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 03-01-09	**CHECKED BY** TOM HESS		**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 12-BIT ANALOG-TO-DIGITAL CONVERTER WITH SERIAL CONTROL AND 11 ANALOG INPUTS, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN		
	SIZE A	**CODE IDENT. NO.** 16236	**DWG NO.** **V62/03614**
	REV	C	**PAGE** 1 **OF** 17

AMSC N/A

5962-V088-18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 12-bit analog-to-digital converter microcircuit, with an operating temperature range of -40°C to +125°C for device type 01, and an operating temperature range of -55°C to +125°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03614	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TLC2543-EP	12 bit analog-to-digital converter with serial control and 11 analog inputs
02	TLC2543-EP	12 bit analog-to-digital converter with serial control and 11 analog inputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MS-013	Plastic small-outline
Y	20	MO-150	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC})	-0.5 V dc to +6.5 V dc 2/
Input voltage range (V_{IN})(any input)	-0.3 V dc to V_{CC} +0.3 V dc
Output voltage (V_{OUT})	-0.3 V dc to V_{CC} +0.3 V dc
Positive reference voltage, (V_{ref+})	V_{CC} +0.1 V dc
Negative reference voltage, (V_{ref-})	-0.1 V dc
Peak input current (I_{IN}) (any input)	±20 mA
Peak total input current (I_{IN}) (all inputs)	±30 mA
Operating free-air temperature range (T_A):	
Device type 01	-40°C to +125°C
Device type 02	-55°C to +125°C
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	29.8°C/W
Case Y	21.9°C/W

1.4 Recommended operating conditions. 3/

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Positive reference voltage, (V_{ref+})	V_{CC} nominal 3/
Negative reference voltage, (V_{ref-})	0.0 V nominal 3/
Differential reference voltage, V_{ref+} - V_{ref-}	+2.5 V dc to V_{CC} +0.1 V dc 3/
Analog input voltage	0.0 V to V_{CC} 3/
High-level control input voltage, V_{IH} (V_{CC} = 4.5 V to 5.5 V)	2.0 V dc minimum
Low-level control input voltage, V_{IL} (V_{CC} = 4.5 V to 5.5 V)	0.8 V dc maximum
Clock frequency at I/O CLOCK	0.0 MHz to 4.1 MHz
Setup time, Address bits at DATA INPUT before I/O CLOCK$\uparrow$, $t_{su(A)}$	100 ns minimum
Hold time, address bits after I/O CLOCK$\uparrow$, $t_{h(A)}$	0.0 ns minimum
Hold time, $\overline{CS}$ low after last I/O CLOCK$\downarrow$, $t_{h(CS)}$	0.0 ns minimum
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$	1.425 µs 4/
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$	120 ns minimum
Pulse duration I/O CLOCK low, $t_{wL(I/O)}$	120 ns minimum
Transition time, I/O CLOCK, high to low, $t_{t(I/O)}$	1 µs maximum 5/
Transition time, DATA INPUT and $\overline{CS}$, $t_{t(CS)}$	10 µs maximum
Operating free-air temperature range (T_A):	
Device type 01	-40°C to +125°C
Device type 02	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “ recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values are with respect to ground terminal with REF- and GND wired together (unless otherwise noted).

3/ Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000).

4/ To minimize errors caused by noise at $\overline{CS}$ input, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

5/ This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices of Microelectronic Components

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at https://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Block diagram. The block diagram shall be as shown in figure 4.

3.5.5 Load circuit. The load circuit shall be as shown in figure 5.

3.5.6 Timing waveforms and test circuit. The timing waveforms shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = -1.6 mA, V_{CC} = 4.5 V	All	2.4		V
		I_{OH} = -20 µA, V_{CC} = 4.5 V to 5.5 V		V_{CC} – 0.1		
Low level output voltage	V_{OL}	I_{OL} = 1.6 mA, V_{CC} = 4.5 V			0.4	V
		I_{OL} = 20 µA, V_{CC} = 4.5 V to 5.5 V			0.1	
High impedance off-stat output current	I_{OZ}	V_O = V_{CC}, $\overline{CS}$ at V_{CC}			2.5	µA
		V_O = 0, $\overline{CS}$ at V_{CC}			-2.5	
High level input current	I_{IH}	V_I = V_{CC}			10	µA
Low level input current	I_{IL}	V_I = 0 V			-10	µA
Operating supply current	I_{CC}	$\overline{CS}$ at 0 V			2.5	mA
Power down current	$I_{CC(PD)}$	For all digital inputs, $0 \leq V_I \leq 0.5$ V or $V_I \geq V_{CC} - 0.5$ V			25	µA
Selected channe leakage current		Selected channel at V_{CC}, unselected channel at 0 V			10	µA
		Selected channel at 0 V, unselected channel at V_{CC}			-10	
Maximum static analog reference current into REF+		V_{ref+} = V_{CC}, V_{ref-} = GND			2.5	µA
Input capacitance	C_I	Analog inputs			60	pF
		Control inputs			15	
Linearity error	E_L	See figure 5. 3/			±1	LSB
Differential linearity error	E_D	See figure 5.			±1	LSB
Offset error	E_O	See figure 5. 4/ 5/			±1.5	LSB
Gain error	E_G	See figure 5. 4/ 5/			±1	LSB
Total unadjusted error	E_T	6/			±1.75	LSB
Self test output code		DATA INPUT = 1011, See figure 3 7/		2048 TYP		
		DATA INPUT = 1100, See figure 3 7/		0 TYP		
		DATA INPUT = 1101, See figure 3 7/		4095 TYP		
Conversion time	$t_{(conv)}$	See figure 6.			10	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions 2/	Device type	Limits		Unit
				Min	Max	
Total cycle time (access, sample, and conversion)	t_C	See figure 6. 8/	All		10 + total I/O CLOCK periods + $t_{d(I/O – EOC)}$	µs
Channel acquisition Time (sample)	t_{acq}	See figure 6. 8/		4	12	I/O CLOCK periods
Valid time, DATA OUT remains valid after I/O CLOCK ↓	t_v	See figure 6.		10		ns
Delay time, I/O CLOCK ↓ to DATA OUT valid	$t_{d(I/O\ DATA)}$	See figure 6.			150	ns
Delay time, last I/O CLOCK ↓ to EOC ↓	$t_{d\ (I/O\ EOC)}$	See figure 6.			2.2	µs
Delay time, EOC ↑ to DATA OUT (MSB/LSB)	$t_{d(EOC\ DATA)}$	See figure 6.			100	ns
Enable time, $\overline{CS}$ ↓ to DATA OUT (MSB/LSB driven)	t_{PZH}, t_{PZL}	See figure 6.			1.3	µs
Disable time, $\overline{CS}$ ↑ to DATA OUT (high impedance)	t_{PHZ}, t_{PLZ}	See figure 6.			150	ns
Rise time, EOC	$t_{r(EOC)}$	See figure 6.			50	ns
Fall time, EOC	$t_{f(EOC)}$	See figure 6.			50	ns
Rise time, data bus	$t_{r(bus)}$	See figure 6.			50	ns
Fall time, data bus	$t_{f(bus)}$	See figure 6.			50	ns
Delay time, last I/O CLOCK ↓ to $\overline{CS}$ ↓ to abort conversion	$t_{d(I/O-CS)}$	9/			5	µs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Device type 01operated at -40°C to +125°C and device type 02 operated at -55°C to +125°C ; $V_{CC} = V_{ref+}$ = 4.5 V to 5.5 V and $f_{(I/O\ CLOCK)}$ = 4.1 MHz unless otherwise specified.

3/ Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristic.

4/ Analog input voltages greater than applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000).

5/ Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep at the offset point.

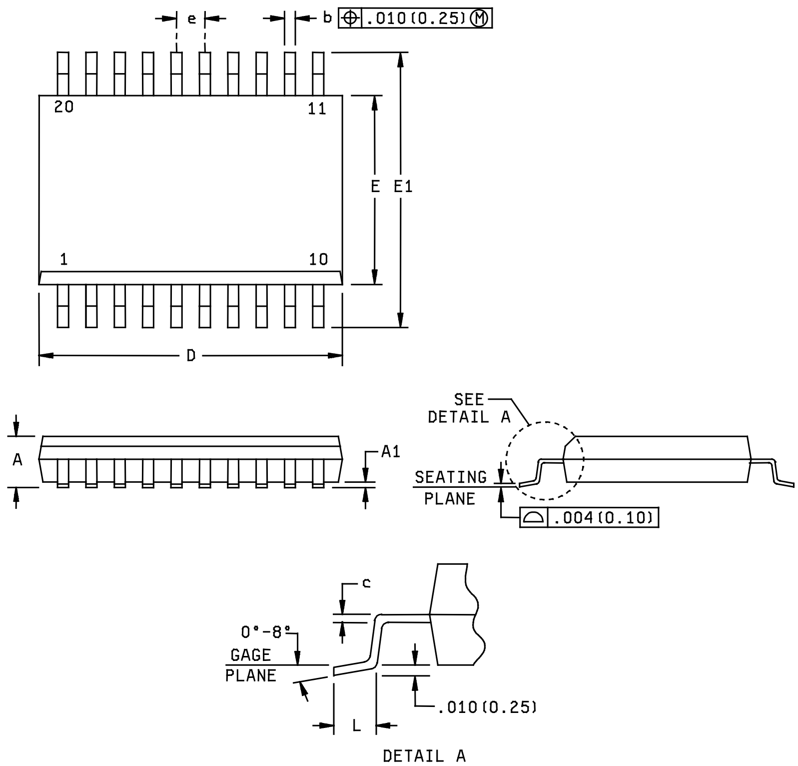
6/ Total unadjusted error comprises linearity, zero-scale, and full-scale errors.

7/ T_A = +25°C. Both the input address and the output codes and expressed in positive logic.

8/ I/O CLOCK period = 1/(I/O CLOCK frequency). See figure 6.

9/ Any transitions of $\overline{CS}$ are recognized as valid only if the levels is maintained for a setup time. $\overline{CS}$ must be taken low at ≤ 5 µs of the tenth I/O CLOCK falling edge to ensure a conversion is aborted. Between 5 µs and 10 µs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

Case X

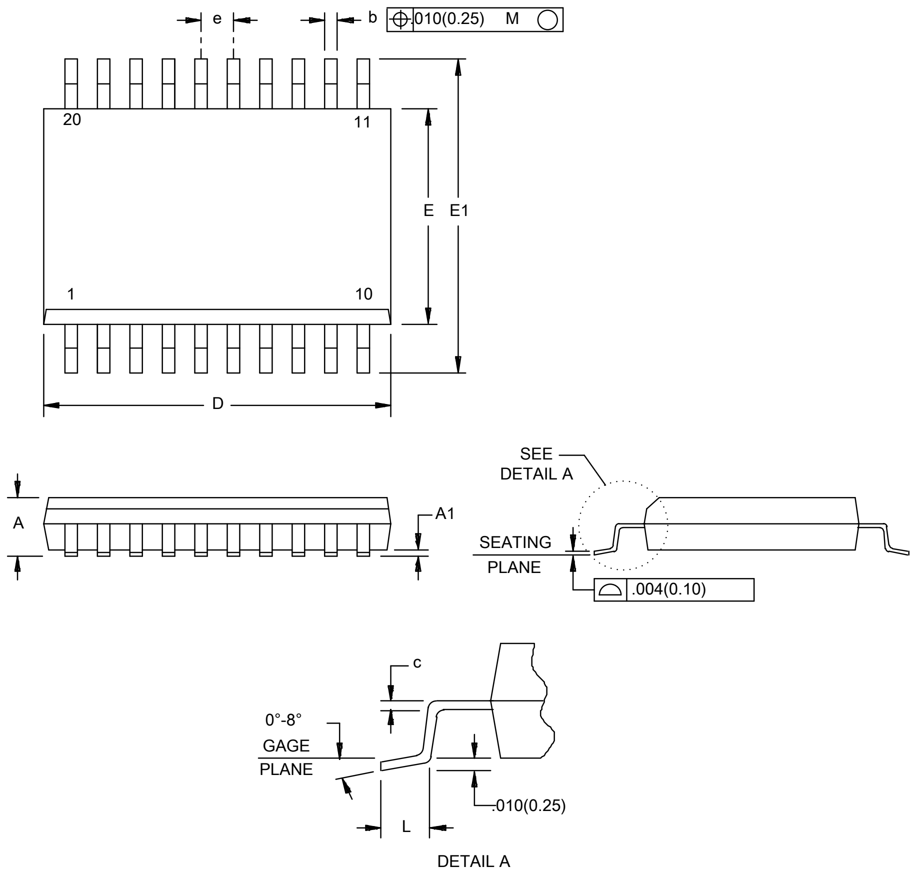


Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		0.104		2.65	E	0.293	0.299	7.45	7.59
A1	0.004	0.012	0.10	0.30	E1	0.400	0.419	10.15	10.65
b	0.014	0.020	0.35	0.51	e	0.050		1.27	
c	0.010 NOM		0.25 NOM		L	0.016	0.050	0.40	1.27
D	0.500	0.510	12.70	12.95					

NOTE:
1. All linear dimensions are in inches (millimeters). Millimeters equivalents are shown for reference only.
2. Body dimensions do not include mold flash or protrusion.
3. This drawing is subject to change without notice.
4. Falls within JEDEC MS-013 variation AC.

FIGURE 1. Case outlines.

Case Y



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	2.00	---	0.079	E	5.00	5.60	0.197	0.220
A1	0.05	---	0.002	---	E1	7.40	8.20	0.291	0.323
b	0.22	0.38	0.009	0.015	e	0.65 BSC		0.026 BSC	
c	0.09	0.25	0.004	0.010	L	0.55	0.95	0.022	0.037
D	6.90	7.50	0.272	0.295					

NOTE:
1. All linear dimensions are in millimeters (inches). Inches equivalents are shown for reference only.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15 millimeters (0.006 inches).
4. Falls within JEDEC MO-150.

FIGURE 1. Case outlines - continued.

Device types	01 and 02
Case outlines	X and Y
Terminal number	Terminal symbol
1	AIN0
2	AIN1
3	AIN2
4	AIN3
5	AIN4
6	AIN5
7	AIN6
8	AIN7
9	AIN8
10	GND
11	AIN9
12	AIN10
13	REF-
14	REF+
15	$\overline{CS}$
16	DATA OUT
17	DATA INPUT
18	I/O CLOCK
19	EOC
20	V_{CC}

Pin description	
Terminal symbol	Description
AINn (n = 0 to 10)	Analog signal inputs
$\overline{CS}$	Chip select
DATA INPUT	Serial data input
DATA OUT	Serial data output
EOC	End of conversion
GND	Ground
I/O CLOCK	Input / Output clock
REF+	Positive reference voltage
REF-	Negative reference voltage
V_{CC}	Positive supply voltage

FIGURE 2. Terminal connections.

Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO DATA INPUT	
	Binary	Hex
AIN0	0000	0
AIN1	0001	1
AIN2	0010	2
AIN3	0011	3
AIN4	0100	4
AIN5	0101	5
AIN6	0110	6
AIN7	0111	7
AIN8	1000	8
AIN9	1001	9
AIN10	1010	A

Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED 1/	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX) 2/
	BINARY	HEX	
$(V_{ref+} - V_{ref-}) / 2$	1011	B	800
V_{ref-}	1100	C	000
V_{ref+}	1101	D	FFF

1/ V_{ref+} is the voltage supplied to REF+, and V_{ref-} is the voltage applied to REF-.
2/ The output results shown are the ideal values and may vary with the reference stability and with internal offsets.

Power-Down-Select Address

INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \leq 25\ \mu A$

FIGURE 3. Truth table.

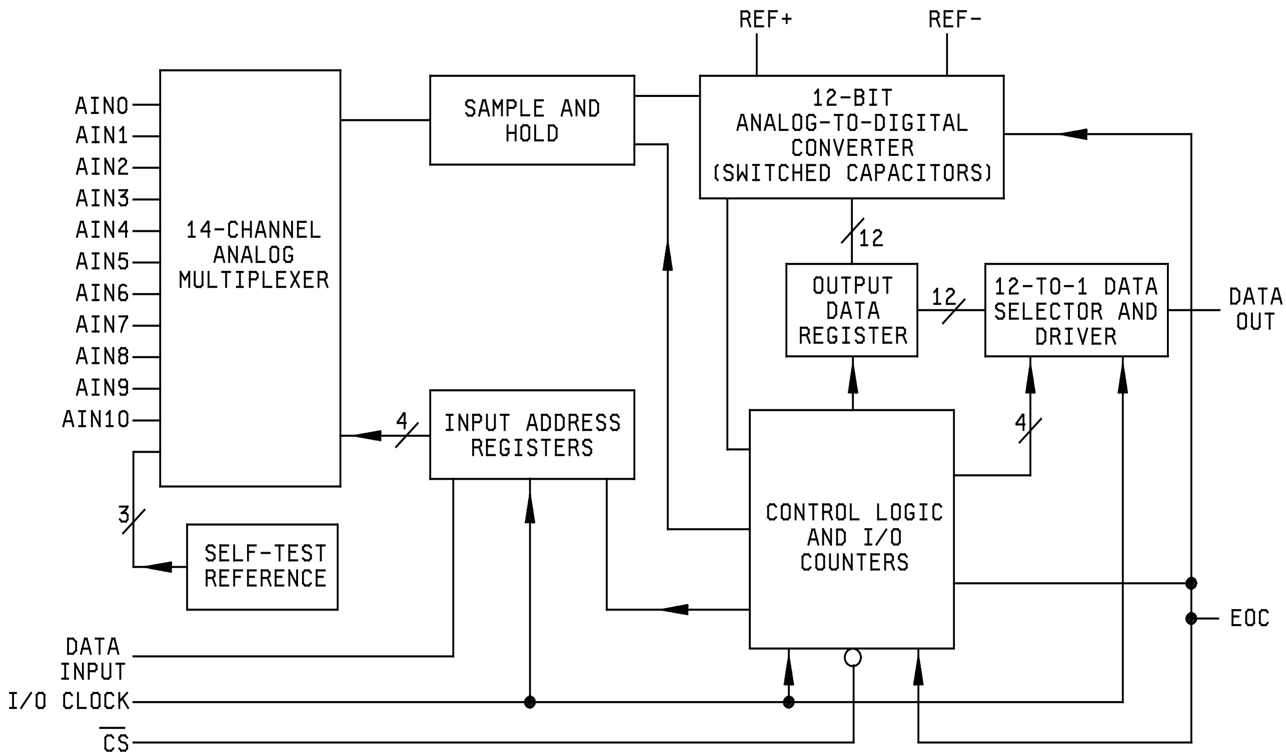
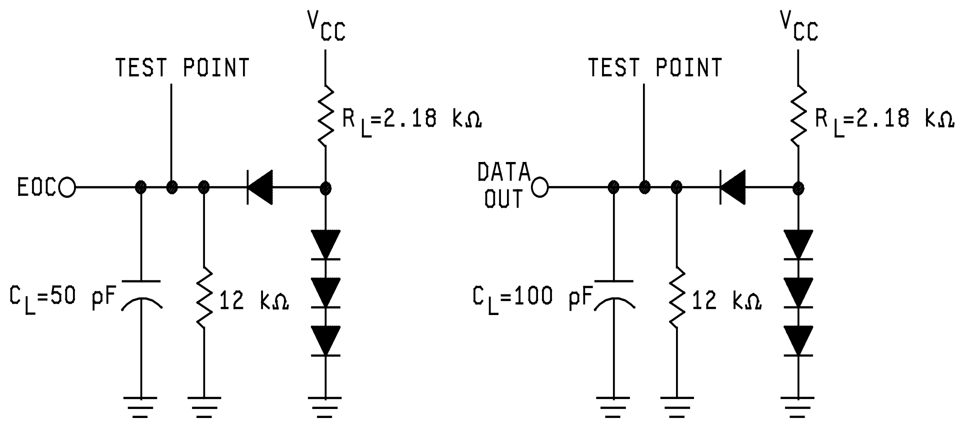
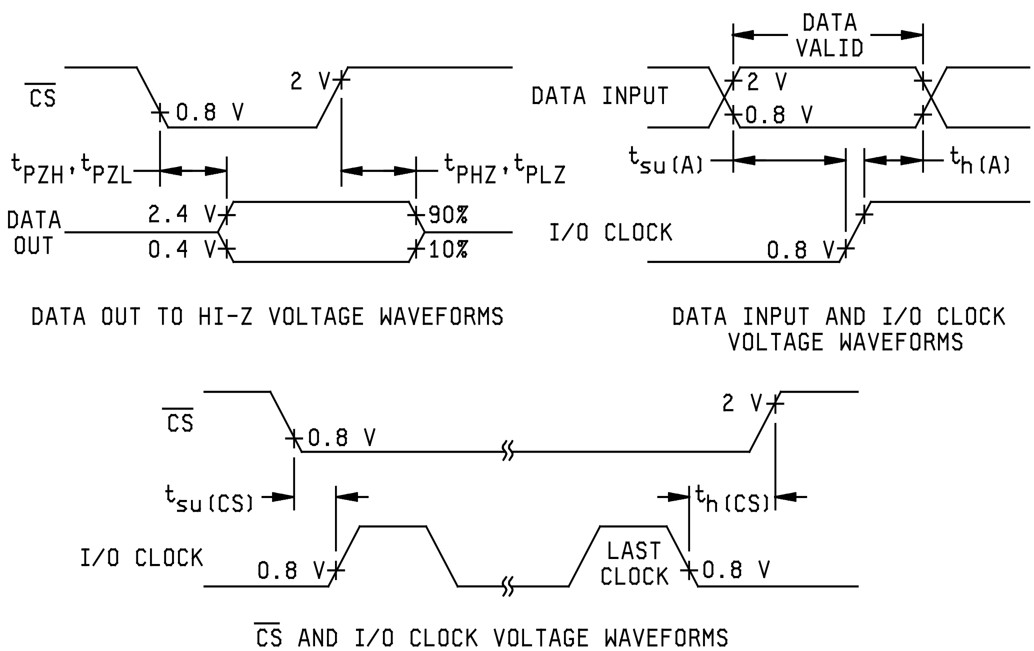


FIGURE 4. <u>Block diagram</u>.



LOAD CIRCUITS

FIGURE 5. Load circuits.



NOTE: To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

FIGURE 6. Timing waveforms.

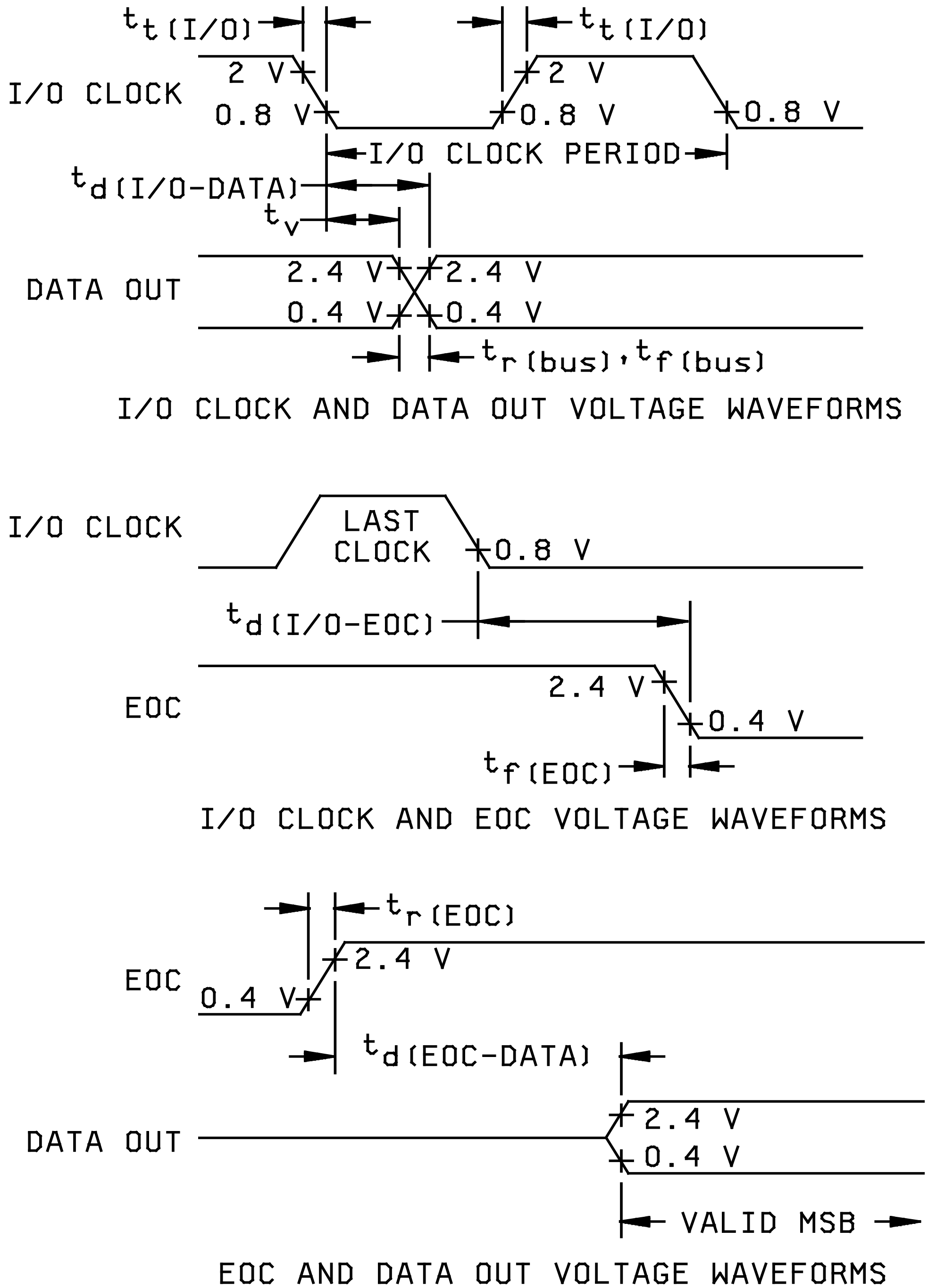
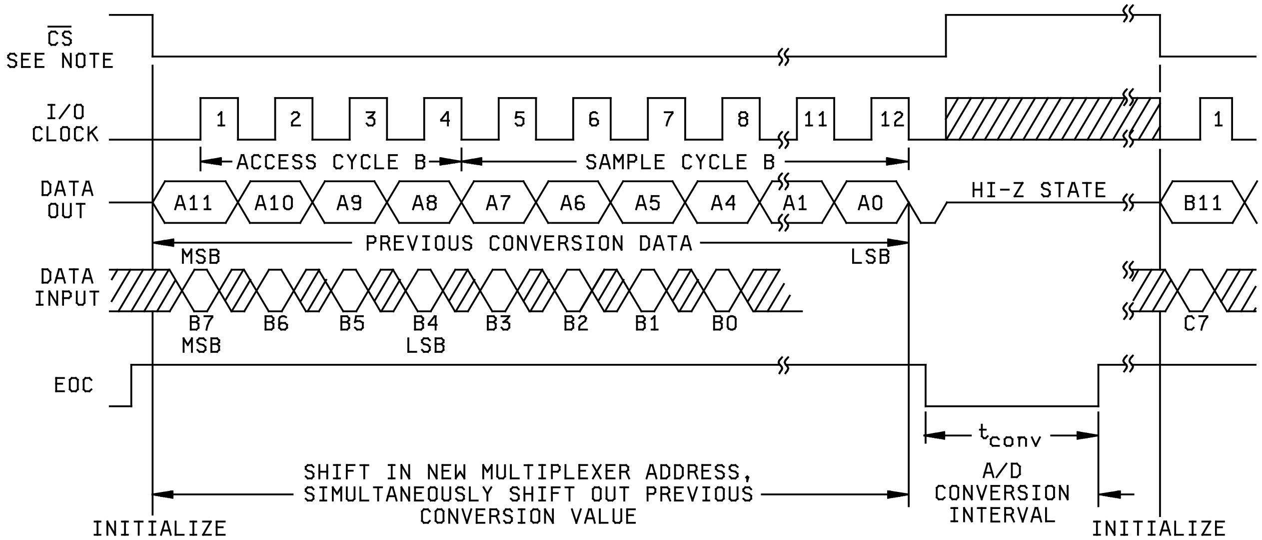
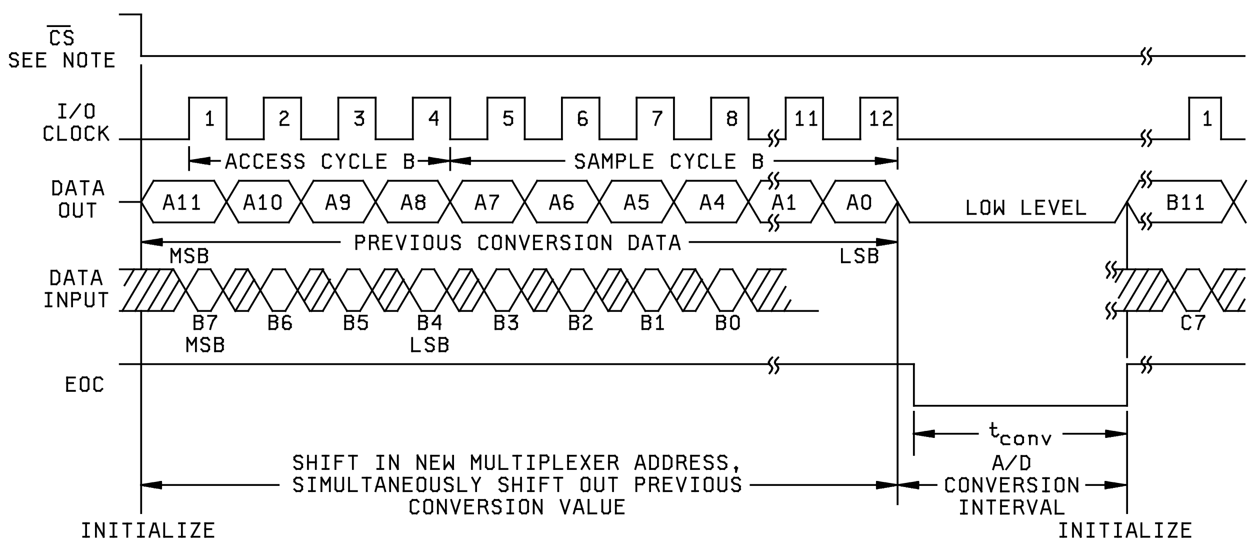


FIGURE 6. Timing waveforms – continued.



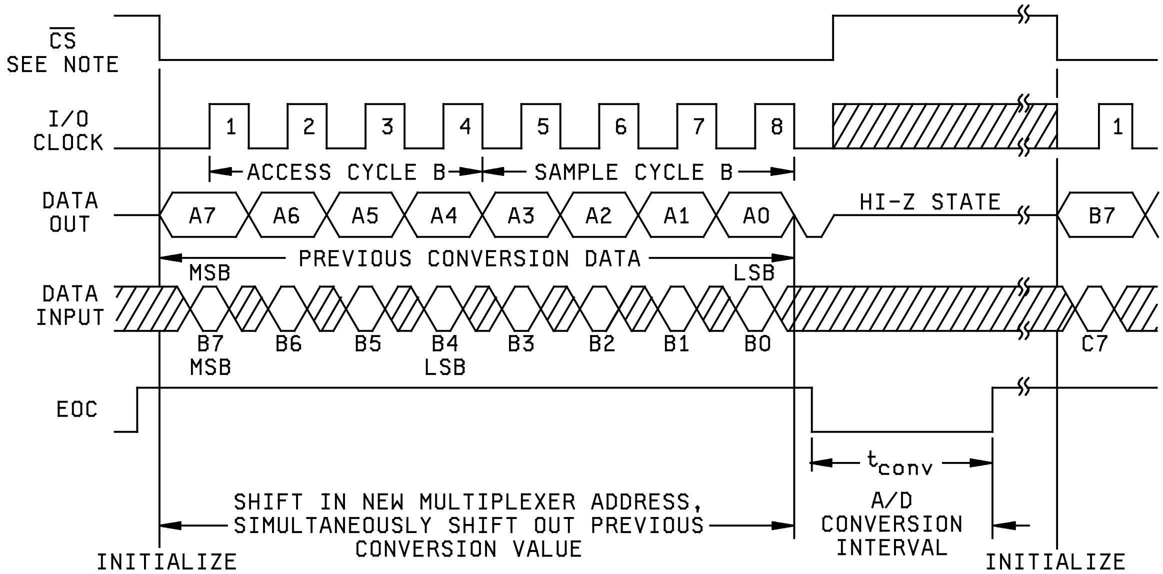
TIMING FOR 12-CLOCK TRANSFER USING $\overline{CS}$ WITH MSB FIRST



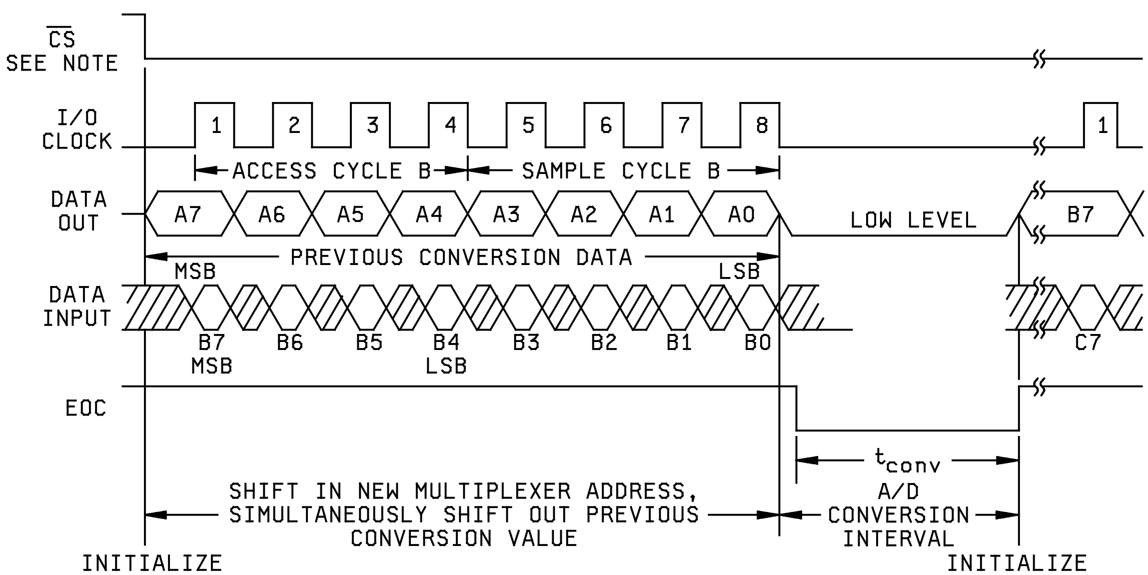
TIMING FOR 12-CLOCK TRANSFER NOT USING $\overline{CS}$ WITH MSB FIRST

NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

FIGURE 6. Timing waveforms – continued.



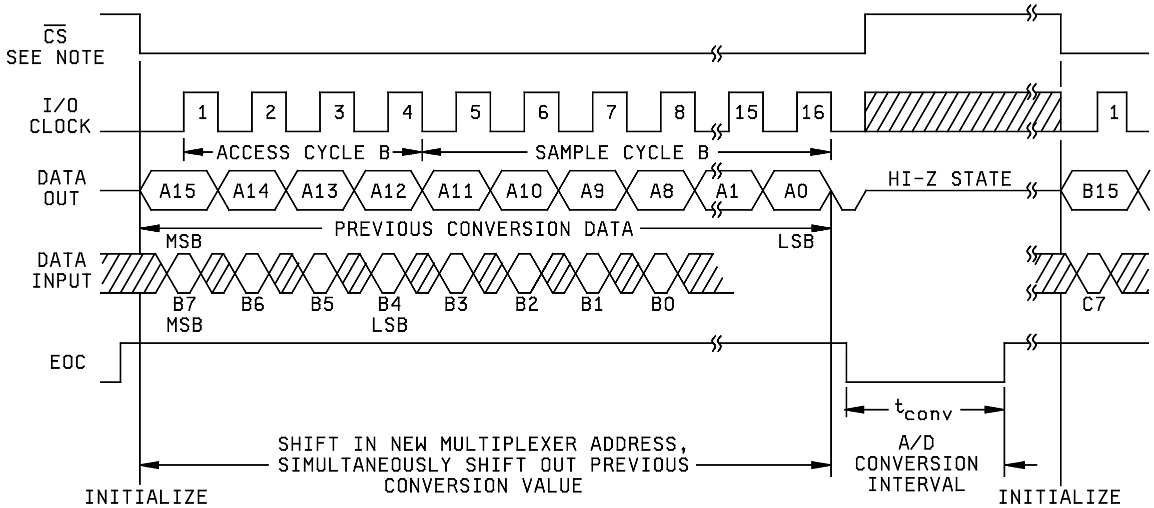
TIMING FOR 8-CLOCK TRANSFER USING $\overline{\text{CS}}$ WITH MSB FIRST



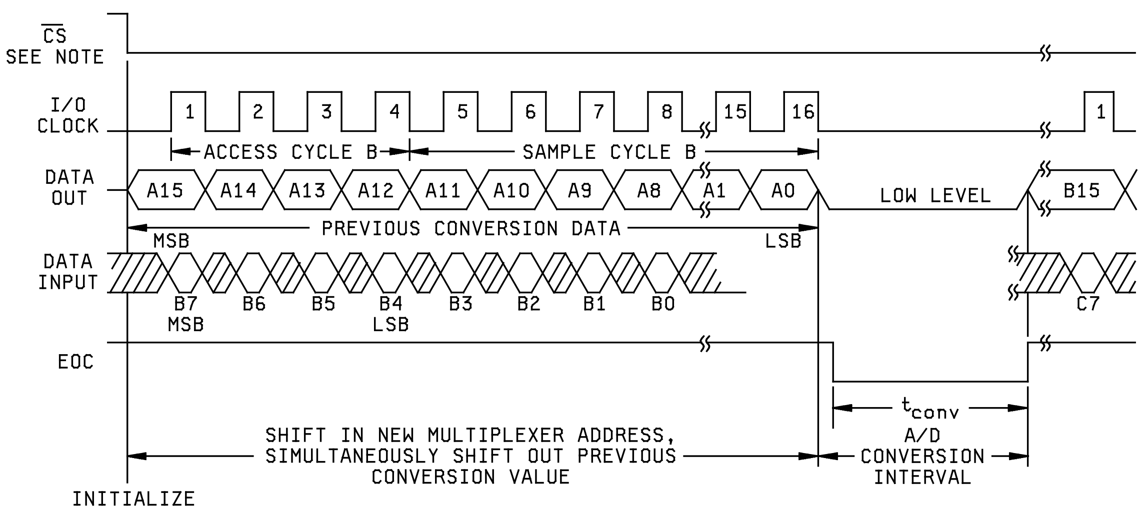
TIMING FOR 8-CLOCK TRANSFER NOT USING $\overline{\text{CS}}$ WITH MSB FIRST

NOTE: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{\text{CS}}$ setup time has elapsed.

FIGURE 6. Timing waveforms – continued.



TIMING FOR 16-CLOCK TRANSFER USING $\overline{CS}$ WITH MSB FIRST



TIMING FOR 16-CLOCK TRANSFER NOT USING $\overline{CS}$ WITH MSB FIRST

NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

FIGURE 6. Timing waveforms – continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03614-01XE	01295	TLC2543QDWREP	TLC2543QEP
V62/03614-02YE	01295	TLC2543MDBREP	TLC2543MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493