

REVISIONS			
LTR	DESCRIPTION	DATE (YY-MM-DD)	APPROVED
A	Correct lead finish on last page. Update boilerplate. - CFS	05-11-01	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	12-03-22	Thomas M. Hess
C	Correct device Lead Fished F to case outline Y. Update boilerplate paragraphs to current requirements. - PHN	18-01-16	Thomas M. Hess



CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV	C	C	C	C	C	C	C	C	C														
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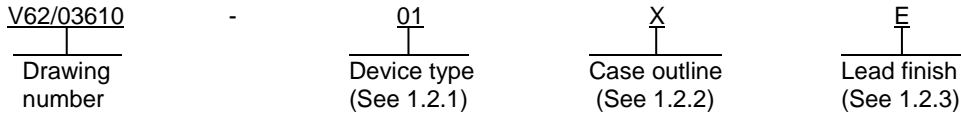
PMIC N/A	PREPARED BY Thanh V. Nguyen	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD 02-12-18	CHECKED BY Thanh V. Nguyen	TITLE MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/03610
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DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance digital signal processor microcircuit, with an operating temperature range of -40°C to +100°C for device type 01 and -55°C to +125°C for device type 02 as shown in 1.2.1 below.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	320VC33-EP	Digital signal processor
02	320VC33-EP	Digital signal processor

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	144	MS-026	Plastic quad flatpack
Y	144		Ceramic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA) <u>1/</u>
Z	Other

1/ Devices listed on this drawing are supplied to lead finish "F". The solder ball material contains compositions of: Sn = 63% and Pb = 37%.

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1.3 Absolute maximum ratings. 2/

Supply voltage range (DV _{DD})	-0.3 V to +4.0 V	3/
Supply voltage range (CV _{DD})	-0.3 V to +2.4 V	3/
Input voltage range (V _I).....	-1.0 V to +4.6 V	4/
Output voltage range (V _O).....	-0.3 V to +4.6 V	
Continuous power dissipation (worst case) (P _D)	500 mW	5/
Storage temperature range (T _{STG})	-55°C to +150°C	6/
Case operating temperature range (T _C):		
Device type 01.....	-40°C to +100°C	
Device type 02.....	-55°C to +125°C	

1.4 Recommended operating conditions. 3/ 7/ 8/ 9/

Supply voltage range for the core CPU (CV _{DD})	1.71 V to 1.89 V	10/
Supply voltage range for the I/O pins (DV _{DD})	3.0 V to 3.6 V	11/
Supply ground (V _{SS}).....	0.0 V	
High level input voltage range (V _{IH}).....	0.7 x DV _{DD} to DV _{DD} + 0.3 V	4/
Low level input voltage range (V _{IL})	-0.3 V to 0.3 x DV _{DD}	4/
Maximum high level output current (I _{OH})	4.0 mA	
Maximum low level output current (I _{OL})	4.0 mA	
Case operating temperature range (T _C):		
Device type 01.....	-40°C to +100°C	
Device type 02.....	-55°C to +125°C	
Maximum capacitive load per output pin (C _L).....	30 pF	

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- 2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 - 3/ All voltage values are with respect to V_{SS}.
 - 4/ Absolute dc input level should not exceed the DV_{DD} or V_{SS} supply rails by more than 0.3 V. An instantaneous low current pulse of < 2 ns, < 10 mA, and < 1 V amplitude is permissible.
 - 5/ Actual operating power is much lower. This value was obtained under specially produced worst-case test conditions for the device, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external data and address buses at the maximum possible rate with a capacitive load of 30 pF. See normal (I_{DD}) current specification in table I herein.
 - 6/ Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
 - 7/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
 - 8/ All inputs and I/O pins are configured as inputs.
 - 9/ All inputs and I/O pins use a Schmidt hysteresis inputs except $\overline{\text{SHZ}}$ and D0 – D31. Hysteresis is approximately 10% of DV_{DD} and is centered at 0.5 x DV_{DD}.
 - 10/ CV_{DD} should not exceed DV_{DD} by more than 0.7 V. (Use a Schottky clamp diode between these supplies.)
 - 11/ DV_{DD} should not exceed CV_{DD} by more than 2.5 V.

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2. APPLICABLE DOCUMENTS

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at <http://www.ieee.org> or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331).

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107 or online at <https://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.4 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Functional block diagram. The functional block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 4.

3.5.5 Boundary scan instruction code. The boundary scan instruction code shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _C	Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	DV _{DD} = Min, I _{OH} = Max	25°C, -40°C to 100°C	01	2.4		V
			25°C, -55°C to 125°C	02	2.4		
Low level output voltage	V _{OL}	DV _{DD} = Min, I _{OL} = Max	25°C, -40°C to 100°C	01		0.4	V
			25°C, -55°C to 125°C	02		0.4	
High impedance current	I _Z	DV _{DD} = Max	25°C	All	-5.0	+5.0	μA
Input current	I _I	V _I = V _{SS} to DV _{DD}	25°C	All	-5.0	+5.0	μA
Input current (with internal pullup)	I _{IPU}	Inputs with internal pullups <u>4/</u>	25°C, -40°C to 100°C	01	-600	10	μA
			25°C, -55°C to 125°C	02	-600	10	
Input current (with internal pulldown)	I _{IPD}	Inputs with internal pulldowns <u>4/</u>	25°C, -40°C to 100°C	01	600	-10	μA
			25°C, -55°C to 125°C	02	600	-10	
Input current (with bus keeper) pullup <u>5/</u>	I _{BKU}	Bus keeper opposes until conditions match	25°C, -40°C to 100°C	01	-600	10	μA
			25°C, -55°C to 125°C	02	-600	10	
Input current (with bus keeper) pulldown <u>5/</u>	I _{BKD}		25°C, -40°C to 100°C	01	600	-10	μA
			25°C, -55°C to 125°C	02	600	-10	
Supply current, pins <u>6/ 7/</u>	I _{DDD}	DV _{DD} = Max, f _X = 60 MHz	25°C	01		120	mA
		DV _{DD} = Max, f _X = 75 MHz	25°C	02		260	
Supply current, core CPU <u>6/ 7/</u>	I _{DDC}	CV _{DD} = Max, f _X = 60 MHz	25°C	01		80	mA
		CV _{DD} = Max, f _X = 75 MHz	25°C	02		215	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _c	Device type	Limits		Unit
					Min	Max	
IDLE2, Supply current, I _{DD} plus I _{DDC}	I _{DD}	PLL enabled, oscillator enabled	25°C, -40°C to 100°C	01	2 typical		mA
			25°C, -55°C to 125°C	02	2 typical		
		PLL disabled, oscillator enabled	25°C, -40°C to 100°C	01	500 typical		μA
			25°C, -55°C to 125°C	02	500 typical		
		PLL disabled, oscillator disabled, FLCK = 0	25°C, -40°C to 100°C	01	50 typical		
			25°C, -55°C to 125°C	02	50 typical		
Input capacitance <u>8/</u>	C _i	All inputs except XIN	25°C	All		10	pF
		XIN input				10	
Output capacitance <u>8/</u>	C _o		25°C	All		10	pF
Phase-locked loop characteristics using EXTCLK or on-chip crystal oscillator <u>9/</u>							
Frequency range, PLL input <u>8/</u>	F _{pllin}		25°C, -40°C to 100°C	01	5	15	MHz
			25°C, -55°C to 125°C	02	5	15	
Frequency range, PLL output <u>8/</u>	F _{plout}		25°C, -40°C to 100°C	01	25	75	MHz
			25°C, -55°C to 125°C	02	25	75	
PLL current, CV _{DD} supply <u>8/</u>	I _{pll}		25°C, -40°C to 100°C	01		2	mA
			25°C, -55°C to 125°C	02		2	
PLL power, CV _{DD} supply <u>8/</u>	P _{pll}		25°C, -40°C to 100°C	01		5	mW
			25°C, -55°C to 125°C	02		5	
PLL output duty cycle at H1 <u>8/</u>	PLL _{dc}		25°C, -40°C to 100°C	01	45	55	%
			25°C, -55°C to 125°C	02	45	55	
PLL output jitter, F _{plout} = 25 MHz <u>8/</u>	PLL _J		25°C, -40°C to 100°C	01		400	ps
			25°C, -55°C to 125°C	02		400	
PLL lock time in input cycles	PLL _{LOCK}		25°C, -40°C to 100°C	01		1000	cycles
			25°C, -55°C to 125°C	02		1000	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _C	Device type	Limits		Unit
					Min	Max	
Circuit parameters for on-chip crystal oscillator <u>10/</u>							
Oscillator internal supply voltage	V _O	See figure 4	25°C, -40°C to 100°C	01	CV _{DD} typical		V
			25°C, -55°C to 125°C	02	CV _{DD} typical		
Fundamental mode frequency range <u>8/</u>	F _O		25°C, -40°C to 100°C	01	1	20	MHz
			25°C, -55°C to 125°C	02	1	20	
DC bias point (input threshold) <u>8/</u>	V _{bias}		25°C, -40°C to 100°C	01	40	60	%V _O
			25°C, -55°C to 125°C	02	40	60	
Feedback resistance <u>8/</u>	R _{fbk}		25°C, -40°C to 100°C	01	100	500	kΩ
			25°C, -55°C to 125°C	02	100	500	
Small signal ac output impedance <u>8/</u>	R _{out}		25°C, -40°C to 100°C	01	250	1000	Ω
			25°C, -55°C to 125°C	02	250	1000	
The ac output voltage with test crystal <u>11/</u>	V _{xoutac}		25°C, -40°C to 100°C	01	85 typical		%V _O
			25°C, -55°C to 125°C	02	85 typical		
The ac input voltage with test crystal <u>11/</u>	V _{xinac}		25°C, -40°C to 100°C	01	85 typical		%V _O
			25°C, -55°C to 125°C	02	85 typical		
V _{xin} = V _{xinh} , I _{xout} = 0, F _O = 0 (logic input) <u>8/</u>	V _{xoutl}		25°C, -40°C to 100°C	01	V _{SS} -0.1	V _{SS} +0.3	V
			25°C, -55°C to 125°C	02	V _{SS} -0.1	V _{SS} +0.3	
V _{xin} = V _{xinl} , I _{xout} = 0, F _O = 0 (logic input) <u>8/</u>	V _{xouth}		25°C, -40°C to 100°C	01	CV _{DD} - 0.3	CV _{DD} +0.1	V
			25°C, -55°C to 125°C	02	CV _{DD} - 0.3	CV _{DD} +0.1	
When used for logic level input, oscillator enabled <u>8/</u>	V _{inl}		25°C, -40°C to 100°C	01	-0.3	0.2V _O	V
			25°C, -55°C to 125°C	02	-0.3	0.2V _O	
When used for logic level input, oscillator enabled <u>8/</u>	V _{inh}		25°C, -40°C to 100°C	01	0.8V _O	DV _{DD} +0.3	V
			25°C, -55°C to 125°C	02	0.8V _O	DV _{DD} +0.3	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _C	Device type	Limits		Unit	
					Min	Max		
Circuit parameters for on-chip crystal oscillator - Continued <u>10/</u>								
When used for logic level input, oscillator disabled <u>8/</u>	V _{xinh}	See figure 4	25°C, -40°C to 100°C	01	0.7 DV _{DD}	DV _{DD} +0.3	V	
			25°C, -55°C to 125°C	02	0.7 DV _{DD}	DV _{DD} +0.3		
XOUT internal load capacitance <u>8/</u>	C _{xout}		25°C	All	2	5	pF	
XIN internal load capacitance <u>8/</u>	C _{xin}		25°C	All	2	5	pF	
Delay time, XIN to H1, x1 and x0.5 modes	t _{d(XIN-H1)}		25°C, -40°C to 100°C	01	2	8	ns	
			25°C, -55°C to 125°C	02		8		
Input current, feedback enabled, V _{il} = 0 <u>8/</u>	I _{inl}		25°C, -40°C to 100°C	01		50	μA	
			25°C, -55°C to 125°C	02		50		
Input current, feedback enabled, V _{il} = V _{ih} <u>8/</u>	I _{inh}		25°C, -40°C to 100°C	01		-50	μA	
			25°C, -55°C to 125°C	02		-50		
Timing requirements for EXTCLK, all modes								
Rise time, EXTCLK <u>8/</u>	t _{r(EXTCLK)}	See figure 4	F = F _{max} , x0.5 and x1 modes	25°C, -40°C to 100°C	01		1	ns
				25°C, -55°C to 125°C	02		1	
			F < F _{max}	25°C, -40°C to 100°C	01		4	
				25°C, -55°C to 125°C	02		4	
Fall time, EXTCLK <u>8/</u>	t _{f(EXTCLK)}		F = F _{max} , x0.5 and x1 modes	25°C, -40°C to 100°C	01		1	ns
				25°C, -55°C to 125°C	02		1	
			F < F _{max}	25°C, -40°C to 100°C	01		4	
				25°C, -55°C to 125°C	02		4	
Pulse duration, EXTCLK low <u>8/</u>	t _{w(EXTCLKL)}		x5 mode	25°C, -40°C to 100°C	01	21		ns
				25°C, -55°C to 125°C	02	21		
			x1 mode	25°C, -40°C to 100°C	01	5.5		
				25°C, -55°C to 125°C	02	5.5		
			x0.5 mode	25°C, -40°C to 100°C	01	4		
				25°C, -55°C to 125°C	02	4		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _c	Device type	Limits		Unit					
					Min	Max						
Timing requirements for EXTCLK, all modes - Continued												
Pulse duration, EXTCLK high <u>8/</u>	t _{w(EXTCLKH)}	See figure 4	x5 mode	25°C, -40°C to 100°C	01	21	ns					
				25°C, -55°C to 125°C	02	21						
			x1 mode	25°C, -40°C to 100°C	01	5.5						
				25°C, -55°C to 125°C	02	5.5						
			x0.5 mode	25°C, -40°C to 100°C	01	4						
				25°C, -55°C to 125°C	02	4						
Duty cycle, EXTCLK [t _{w(EXTCLKH)} /t _{c(H)}]	t _{dc(EXTCLK)}		x5 PLL mode <u>8/</u>	25°C, -40°C to 100°C	01	40	60	%				
				25°C, -55°C to 125°C	02	40	60					
			x1 and x0.5 modes, F = F _{max}	25°C, -40°C to 100°C	01	45	55					
				25°C, -55°C to 125°C	02	45	55					
			x1 and x0.5 modes, F = 0 Hz <u>8/</u>	25°C, -40°C to 100°C	01	0	100					
				25°C, -55°C to 125°C	02	0	100					
			Cycle time, EXTCLK	t _{c(EXTCLK)}		x5 mode <u>8/</u>	25°C, -40°C to 100°C		01	66.7	200	ns
							25°C, -55°C to 125°C		02	66.7	200	
x1 mode	25°C, -40°C to 100°C	01				13.3						
	25°C, -55°C to 125°C	02				13.3						
x0.5 mode <u>8/</u>	25°C, -40°C to 100°C	01				10						
	25°C, -55°C to 125°C	02				10						
Frequency range, 1/t _{c(EXTCLK)}	F _{ext}		x5 mode <u>8/</u>	25°C, -40°C to 100°C	01	5	15	MHz				
				25°C, -55°C to 125°C	02	5	15					
			x1 mode	25°C, -40°C to 100°C	01	0	75					
				25°C, -55°C to 125°C	02	0	75					
			x0.5 mode <u>8/</u>	25°C, -40°C to 100°C	01	0	100					
				25°C, -55°C to 125°C	02	0	100					

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _C	Device type	Limits		Unit	
					Min	Max		
Switching characteristics for EXTCLK over recommended operating conditions, all modes								
Mid-level, used to measure duty cycle	V _{mid}	See figure 4	25°C, -40°C to 100°C	01	0.5DV _{DD} typical		V	
			25°C, -55°C to 125°C	02	0.5DV _{DD} typical			
Delay time, EXTCLK to H1 and H3 <u>8/</u>	t _{d(EXTCLK-H)}		x1 mode	25°C, -40°C to 100°C	01	2	7	ns
				25°C, -55°C to 125°C	02	2	7	
			x0.5 mode	25°C, -40°C to 100°C	01	2	7	
				25°C, -55°C to 125°C	02	2	7	
Rise time, H1 and H3 <u>8/</u>	t _{r(H)}		25°C, -40°C to 100°C	01		3	ns	
			25°C, -55°C to 125°C	02		3		
Fall time, H1 and H3 <u>8/</u>	t _{r(H)}		25°C, -40°C to 100°C	01		3	ns	
			25°C, -55°C to 125°C	02		3		
Delay time, from H1 low to H3 high or from H3 low to H1 high <u>8/</u>	t _{d(HL-HH)}		25°C, -40°C to 100°C	01	-1.5	2	ns	
			25°C, -55°C to 125°C	02	-1.5	2		
Cycle time, H1 and H3	t _{c(H)}		x5 PLL mode	25°C, -40°C to 100°C	01	1/(5fext) typical		ns
				25°C, -55°C to 125°C	02	1/(5fext) typical		
			x1 mode	25°C, -40°C to 100°C	01	1/fext typical		
				25°C, -55°C to 125°C	02	1/fext typical		
			x0.5 mode	25°C, -40°C to 100°C	01	2/fext typical		
				25°C, -55°C to 125°C	02	2/fext typical		
Timing requirements for memory read/write <u>12/</u>								
Setup time, data before H1 low (read) <u>8/</u>	t _{su(D-H1L)R}	See figure 4	25°C, -40°C to 100°C	01	5		ns	
			25°C, -55°C to 125°C	02	5			
Hold time, data after H1 low (read) <u>8/</u>	t _{h(H1L-D)R}		25°C, -40°C to 100°C	01	-1		ns	
			25°C, -55°C to 125°C	02	-1			
Setup time, $\overline{\text{RDY}}$ before H1 high	t _{su(RDY-H1H)}		25°C, -40°C to 100°C	01	5		ns	
			25°C, -55°C to 125°C	02	5			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified		Temperature, T _c	Device type	Limits		Unit
						Min	Max	
Timing requirements for memory read/write - Continued <u>12/</u>								
Hold time, $\overline{\text{RDY}}$ after H1 high <u>8/</u>	t _{h(H1H-RDY)}	See figure 4		25°C, -40°C to 100°C	01	-1		ns
				25°C, -55°C to 125°C	02	-1		
Delay time, address valid to $\overline{\text{RDY}}$ <u>8/</u>	t _{d(A-RDY)}			25°C, -40°C to 100°C	01		P-7 <u>13/</u>	ns
				25°C, -55°C to 125°C	02		P-6 <u>13/</u>	
Valid time, data valid after address $\overline{\text{PAGE}}_{\text{x}}$, or $\overline{\text{STRB}}$ valid <u>8/</u>	t _{v(A-D)}	See figure 4	0 wait state, C _L = 30 pF	25°C, -40°C to 100°C	01		9	ns
				25°C, -55°C to 125°C	02		6	
			1 wait state	25°C, -40°C to 100°C	01		t _{c(H)} +9	
				25°C, -55°C to 125°C	02		t _{c(H)} +6	
Switching characteristics over recommended operating conditions for memory read/write <u>12/</u>								
Delay time, H1 low to $\overline{\text{STRB}}$ low	t _{d(H1L-SL)}	See figure 4		25°C, -40°C to 100°C	01	-1 <u>8/</u>	4	ns
				25°C, -55°C to 125°C	02	-1 <u>8/</u>	3	
Delay time, H1 low to $\overline{\text{STRB}}$ high	t _{d(H1L-SH)}			25°C, -40°C to 100°C	01	-1 <u>8/</u>	4	ns
				25°C, -55°C to 125°C	02	-1 <u>8/</u>	3	
Delay time, H1 high to R/W low (write)	t _{d(H1H-RWL)W}			25°C, -40°C to 100°C	01	-1 <u>8/</u>	4	ns
				25°C, -55°C to 125°C	02	-1 <u>8/</u>	3	
Delay time, H1 low to address valid	t _{d(H1L-A)}			25°C, -40°C to 100°C	01	-1 <u>8/</u>	4	ns
				25°C, -55°C to 125°C	02	-1 <u>8/</u>	3	
Delay time, H1 high to R/W high (write)	t _{d(H1H-RWH)W}			25°C, -40°C to 100°C	01	-1 <u>8/</u>	4	ns
				25°C, -55°C to 125°C	02	-1 <u>8/</u>	3	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _c	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for memory read/write - Continued <u>12/</u>							
Delay time, H1 high to address valid on back-to-back write cycles (write)	t _{d(H1H-A)W}	See figure 4	25°C, -40°C to 100°C	01	-1 <u>8/</u>	4 <u>8/</u>	ns
			25°C, -55°C to 125°C	02	-1 <u>8/</u>	3 <u>8/</u>	
Valid time, data after H1 low (write)	t _{v(H1L-D)W}		25°C, -40°C to 100°C	01		6	ns
			25°C, -55°C to 125°C	02		5	
Hold time, data after H1 high (write)	t _{h(H1H-D)W}		25°C, -40°C to 100°C	01	0 <u>8/</u>	5	ns
			25°C, -55°C to 125°C	02	0 <u>8/</u>	5	
Timing requirements for XF0 and XF1 when executing LDFI or LDII							
Setup time, XF1 before H1 low <u>8/</u>	t _{su(XF1-H1L)}	See figure 4	25°C, -40°C to 100°C	01	5		ns
			25°C, -55°C to 125°C	02	4		
Hold time, XF1 after H1 low <u>8/</u>	t _{h(H1L-XF1)}		25°C, -40°C to 100°C	01	0		ns
			25°C, -55°C to 125°C	02	0		
Switching characteristics over recommended operating conditions for XF0 and XF1 when executing LDFI or LDII							
Delay time, H3 high to XF0 low	t _{d(H3H-XF0L)}	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Switching characteristics over recommended operating conditions for XF0 when executing STFI or STII							
Delay time, H3 high to XF0 high <u>14/</u>	t _{d(H3H-XF0H)}	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Timing requirements for XF0 and XF1 when executing SIGI							
Setup time, XF1 before H1 low <u>8/</u>	t _{su(XF1-H1L)}	See figure 4	25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		4	
Hold time, XF1 after H1 low <u>8/</u>	t _{h(H1L-XF1)}		25°C, -40°C to 100°C	01		0	ns
			25°C, -55°C to 125°C	02		0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _c	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for XF0 and XF1 when executing SIGI							
Delay time, H3 high to XF0 low	t _{d(H3H-XF0L)}	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Delay time, H3 high to XF0 high	t _{d(H3H-XF0H)}	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Switching characteristics over recommended operating conditions for loading the XF register when configured as an output pin							
Valid time, XF _x after H3 high	t _{v(H3H-XF)}	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Timing requirements for changing XF_x from output to input mode							
Setup time, XF _x before H1 low	t _{su(XF-H1L)}	See figure 4	25°C, -40°C to 100°C	01	5		ns
			25°C, -55°C to 125°C	02	4		
Hold time, XF _x after H1 low	t _{h(H1L-XF)}	See figure 4	25°C, -40°C to 100°C	01	0		ns
			25°C, -55°C to 125°C	02	0		
Switching characteristics over recommended operating conditions for changing XF_x from output to input mode							
Disable time, XF _x after H3 high <u>8/</u>	t _{dis(H3H-XF)}	See figure 4	25°C, -40°C to 100°C	01		6	ns
			25°C, -55°C to 125°C	02		5	
Switching characteristics over recommended operating conditions for changing XF_x from input to output mode							
Delay time, H3 high to XF _x switching from input to output	t _{d(H3H-XF)}	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Timing requirements for $\overline{\text{RESET}}$							
Setup time, $\overline{\text{RESET}}$ before EXTCLK low <u>8/</u>	t _{su(RESET-EXTCLKL)}	See figure 4	25°C, -40°C to 100°C	01	6	P-7 15/	ns
			25°C, -55°C to 125°C	02	5	P-7 15/	
Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	t _{su(RESETH-H1L)}	See figure 4	25°C, -40°C to 100°C	01	6		ns
			25°C, -55°C to 125°C	02	5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _C	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for <u>RESET</u>							
Delay time, EXTCLK high to H1 high <u>8/</u>	t _d (EXTCLKH-H1H)	See figure 4	25°C, -40°C to 100°C	01	2	7	ns
			25°C, -55°C to 125°C	02	2	7	
Delay time, EXTCLK high to H1 low <u>8/</u>	t _d (EXTCLKH-H1L)		25°C, -40°C to 100°C	01	2	7	ns
			25°C, -55°C to 125°C	02	2	7	
Delay time, EXTCLK high to H3 low <u>8/</u>	t _d (EXTCLKH-H3L)		25°C, -40°C to 100°C	01	2	7	ns
			25°C, -55°C to 125°C	02	2	7	
Delay time, EXTCLK high to H3 high <u>8/</u>	t _d (EXTCLKH-H3H)		25°C, -40°C to 100°C	01	2	7	ns
			25°C, -55°C to 125°C	02	2	7	
Disable time, data (high impedance) from H1 high <u>8/ 16/</u>	t _{dis} (H1H-DZ)		25°C, -40°C to 100°C	01		7	ns
			25°C, -55°C to 125°C	02		6	
Disable time, address (high impedance) from H3 high <u>8/</u>	t _{dis} (H3H-AZ)		25°C, -40°C to 100°C	01		7	ns
			25°C, -55°C to 125°C	02		6	
Delay time, H3 high to control signals high <u>8/</u>	t _d (H3H-CONTROLH)		25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Delay time, H1 high to R/W high <u>8/</u>	t _d (H1H-RWH)		25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Delay time, H1 high to IACK high <u>8/</u>	t _d (H1H-IACKH)		25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Disable time, asynchronous reset signals disabled (high impedance) from <u>RESET</u> low <u>8/ 17/</u>	t _{dis} (RESETL-ASYNCH)		25°C, -40°C to 100°C	01		7	ns
			25°C, -55°C to 125°C	02		6	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _c	Device type	Limits		Unit	
					Min	Max		
Timing requirements for $\overline{\text{INT3}}$ - $\overline{\text{INT0}}$ response								
Setup time, $\overline{\text{INT3}}$ - $\overline{\text{INT0}}$ before H1 low <u>8/</u>	t _{su} (INT-H1L)	See figure 4	25°C, -40°C to 100°C	01	5		ns	
			25°C, -55°C to 125°C	02	4			
Hold time, $\overline{\text{INT3}}$ - $\overline{\text{INT0}}$ after H1 low	t _h (H1L-INT)		25°C, -40°C to 100°C	01		0	ns	
			25°C, -55°C to 125°C	02		0		
Pulse duration, interrupt to ensure only one interrupt <u>8/ 18/</u>	t _w (INT)		25°C, -40°C to 100°C	01	P+5	2P-5	ns	
			25°C, -55°C to 125°C	02	P+5	2P-5		
Switching characteristics over recommended operating conditions for $\overline{\text{IACK}}$								
Delay time, H1 high to $\overline{\text{IACK}}$ low	t _d (H1H-IACKL)	See figure 4	25°C, -40°C to 100°C	01	-1 <u>8/</u>	4	ns	
			25°C, -55°C to 125°C	02	-1 <u>8/</u>	3		
Delay time, H1 high to $\overline{\text{IACK}}$ high	t _d (H1H-IACKH)		25°C, -40°C to 100°C	01	-1 <u>8/</u>	4	ns	
			25°C, -55°C to 125°C	02	-1 <u>8/</u>	3		
Timing requirements for serial port parameters								
Cycle time, CLKX/R <u>8/</u>	t _c (SCK)	See figure 4	CLKX/R ext	25°C, -40°C to 100°C	01	t _c (H)X2.6		ns
				25°C, -55°C to 125°C	02	t _c (H)X2.6		
			CLKX/R int	25°C, -40°C to 100°C	01	t _c (H)X4 <u>19/</u>	t _c (H)X2 ¹⁶	
				25°C, -55°C to 125°C	02	t _c (H)X4 <u>19/</u>	t _c (H)X2 ¹⁶	
Pulse duration, CLKX/R high/low	t _w (SCK)		CLKX/R ext	25°C, -40°C to 100°C	01	t _c (H)+5		ns
				25°C, -55°C to 125°C	02	t _c (H)+5		
			CLKX/R int <u>8/</u>	25°C, -40°C to 100°C	01	[t _c (SCK)/2]-4	[t _c (SCK)/2]+4	
				25°C, -55°C to 125°C	02	[t _c (SCK)/2]-4	[t _c (SCK)/2]+4	
Rise time, CLKX/R <u>8/</u>	t _r (SCK)	See figure 4	25°C, -40°C to 100°C	01		3	ns	
			25°C, -55°C to 125°C	02		3		
Fall time, CLKX/R <u>8/</u>	t _f (SCK)		25°C, -40°C to 100°C	01		3	ns	
			25°C, -55°C to 125°C	02		3		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _c	Device type	Limits		Unit	
					Min	Max		
Timing requirements for serial port parameters - Continued								
Setup time, DR before CLKR low <u>8/</u>	t _{su(DR-CLKRL)}	See figure 4	CLKR ext	25°C, -40°C to 100°C	01	4	ns	
				25°C, -55°C to 125°C	02	4		
			CLKR int	25°C, -40°C to 100°C	01	5		
				25°C, -55°C to 125°C	02	5		
Hold time, DR after CLKR low <u>8/</u>	t _{h(CLKRL-DR)}	See figure 4	CLKR ext	25°C, -40°C to 100°C	01	3	ns	
				25°C, -55°C to 125°C	02	3		
			CLKR int	25°C, -40°C to 100°C	01	0		
				25°C, -55°C to 125°C	02	0		
Setup time, FSR before CLKR low <u>8/</u>	t _{su(FSR-CLKRL)}	See figure 4	CLKR ext	25°C, -40°C to 100°C	01	4	ns	
				25°C, -55°C to 125°C	02	4		
			CLKR int	25°C, -40°C to 100°C	01	5		
				25°C, -55°C to 125°C	02	5		
Hold time, FSX/R input after CLKX/R low <u>8/</u>	t _{h(SCKL-FS)}	See figure 4	CLKX/R ext	25°C, -40°C to 100°C	01	3	ns	
				25°C, -55°C to 125°C	02	3		
			CLKX/R int	25°C, -40°C to 100°C	01	0		
				25°C, -55°C to 125°C	02	0		
Setup time, external FSX before CLKX <u>8/</u>	t _{su(FSX-CLKX)}	See figure 4	CLKX ext	25°C, -40°C to 100°C	01	-[t _{c(H)} -6]	[t _{c(SCK)/2}]-6	ns
				25°C, -55°C to 125°C	02	-[t _{c(H)} -6]	[t _{c(SCK)/2}]-6	
			CLKX int	25°C, -40°C to 100°C	01	-[t _{c(H)} -10]	t _{c(SCK)/2}	
				25°C, -55°C to 125°C	02	-[t _{c(H)} -10]	t _{c(SCK)/2}	
Switching characteristics over recommended operating conditions for serial port parameters								
Delay time, H1 high to internal CLKX/R <u>8/</u>	t _{d(H1H-SCK)}	See figure 4		25°C, -40°C to 100°C	01		4	ns
				25°C, -55°C to 125°C	02		4	
Delay time, CLKX to DX valid	t _{d(CLKX-DX)}	See figure 4	CLKX ext	25°C, -40°C to 100°C	01		6	ns
				25°C, -55°C to 125°C	02		6	
			CLKX int <u>8/</u>	25°C, -40°C to 100°C	01		5	
				25°C, -55°C to 125°C	02		5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _c	Device type	Limits		Unit	
					Min	Max		
Switching characteristics over recommended operating conditions for serial port parameters – Continued								
Delay time, CLKX to internal FSX high/low	t _d (CLKX-FSX)	See figure 4	CLKX ext	25°C, -40°C to 100°C	01		5	ns
				25°C, -55°C to 125°C	02		5	
			CLKX int <u>8/</u>	25°C, -40°C to 100°C	01		4	
				25°C, -55°C to 125°C	02		4	
Delay time, CLKX to first DX bit, FSX precedes CLKX high	t _d (CLKX-DX)V	See figure 4	CLKX ext	25°C, -40°C to 100°C	01		4	ns
				25°C, -55°C to 125°C	02		4	
			CLKX int <u>8/</u>	25°C, -40°C to 100°C	01		5	
				25°C, -55°C to 125°C	02		5	
Delay time, FSX to first DX bit, CLKX precedes FSX	t _d (FSX-DX)V	See figure 4	25°C, -40°C to 100°C	01		6	ns	
			25°C, -55°C to 125°C	02		6		
Disable time, DX high impedance following last data bit from CLKX high	t _{dis} (CLKX-DXZ)	See figure 4	25°C, -40°C to 100°C	01		6	ns	
			25°C, -55°C to 125°C	02		6		

Timing requirements for $\overline{\text{HOLD}}$ / $\overline{\text{HOLDA}}$

Setup time, $\overline{\text{HOLD}}$ before H1 low	t _{su} (HOLD-H1L)	See figure 4	25°C, -40°C to 100°C	01	3		ns
			25°C, -55°C to 125°C	02	4		
Pulse duration, $\overline{\text{HOLD}}$ low <u>8/</u>	t _w (HOLD)	See figure 4	25°C, -40°C to 100°C	01	3t _{c(H)}		ns
			25°C, -55°C to 125°C	02	3t _{c(H)}		

Switching characteristics over recommended operating conditions for $\overline{\text{HOLD}}$ / $\overline{\text{HOLDA}}$

Valid time, $\overline{\text{HOLDA}}$ after H1 low <u>8/</u>	t _v (H1L-HOLDA)	See figure 4	25°C, -40°C to 100°C	01	-1	4	ns
			25°C, -55°C to 125°C	02	-1	3	
Pulse duration, $\overline{\text{HOLDA}}$ low <u>8/</u>	t _w (HOLDA)	See figure 4	25°C, -40°C to 100°C	01	2t _{c(H)} -4		ns
			25°C, -55°C to 125°C	02	2t _{c(H)} -4		
Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$	t _d (H1L-SH)H	See figure 4	25°C, -40°C to 100°C	01	-1	4	ns
			25°C, -55°C to 125°C	02	-1	3	
Disable time, $\overline{\text{STRB}}$ to the high-impedance state from H1 low	t _{dis} (H1L-S)	See figure 4	25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		4	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _c	Device type	Limits		Unit		
					Min	Max			
Switching characteristics over recommended operating conditions for <u>HOLD / HOLDA</u> - Continued									
Enable time, <u>STRB</u> enabled (active) from H1 low	t _{en(H1L-S)}	See figure 4	25°C, -40°C to 100°C	01		5	ns		
			25°C, -55°C to 125°C	02		4			
Disable time, R/ <u>W</u> to the high-impedance state from H1 low <u>8/</u>	t _{dis(H1L-RW)}		25°C, -40°C to 100°C	01		5	ns		
			25°C, -55°C to 125°C	02		5			
Enable time, R/ <u>W</u> enabled (active) from H1 low	t _{en(H1L-RW)}		25°C, -40°C to 100°C	01		5	ns		
			25°C, -55°C to 125°C	02		4			
Disable time, address to the high-impedance state from H1 low <u>8/</u>	t _{dis(H1L-A)}		25°C, -40°C to 100°C	01		5	ns		
			25°C, -55°C to 125°C	02		4			
Enable time, address enabled (valid) from H1 low	t _{en(H1L-A)}		25°C, -40°C to 100°C	01		5	ns		
			25°C, -55°C to 125°C	02		5			
Disable time, data to the high-impedance state from H1 high <u>8/</u>	t _{dis(H1H-D)}		25°C, -40°C to 100°C	01		5	ns		
			25°C, -55°C to 125°C	02		4			
Timing requirements for peripheral pin general-purpose I/O <u>20/</u>									
Setup time, general- purpose input before H1 low <u>8/</u>	t _{su(GPIO-H1L)}	See figure 4	25°C, -40°C to 100°C	01	4		ns		
			25°C, -55°C to 125°C	02	3				
Hold time, general- purpose input after H1 low <u>8/</u>	t _{h(H1L-GPIO)}		25°C, -40°C to 100°C	01	0		ns		
			25°C, -55°C to 125°C	02	0				
Switching characteristics over recommended operating conditions for peripheral pin general-purpose I/O <u>20/</u>									
Delay time, H1 high to general-purpose output	t _{d(H1H-GPIO)}		See figure 4	25°C, -40°C to 100°C	01		5	ns	
				25°C, -55°C to 125°C	02		4		
Disable time, general- purpose output from H1 high	t _{dis(H1H)}			25°C, -40°C to 100°C	01		7	ns	
				25°C, -55°C to 125°C	02		5		
Timing requirements for timer pin									
Setup time, TCLK external before H1 low <u>8/ 21/</u>	t _{su(TCLK-H1L)}			See figure 4	25°C, -40°C to 100°C	01	4		ns
					25°C, -55°C to 125°C	02	3		

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 18

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u> 3.0 V ≤ DV _{DD} ≤ 3.6 V 1.71 V ≤ CV _{DD} ≤ 1.89 V unless otherwise specified	Temperature, T _c	Device type	Limits		Unit	
					Min	Max		
Timing requirements for timer pin - Continued								
Hold time, TCLK external after H1 low <u>21/</u>	t _{h(H1L-TCLK)}	See figure 4	25°C, -40°C to 100°C	01	0		ns	
			25°C, -55°C to 125°C	02	0			
Switching characteristics over recommended operating conditions for timer pin								
Delay time, H1 high to TCLK internal valid	t _{d(H1H-TCLK)}	See figure 4	25°C, -40°C to 100°C	01		4	ns	
			25°C, -55°C to 125°C	02		3		
Cycle time, TCLK <u>8/ 22/</u>	t _{c(TCLK)}		TCLK ext	25°C, -40°C to 100°C	01	t _{c(H)} X2.6	ns	
				25°C, -55°C to 125°C	02	t _{c(H)} X2.6		
			TCLK int	25°C, -40°C to 100°C	01	t _{c(H)} X2		t _{c(H)} X2 ³²
				25°C, -55°C to 125°C	02	t _{c(H)} X2		t _{c(H)} X2 ³²
Pulse duration, TCLK <u>8/ 22/</u>	t _{w(TCLK)}		TCLK ext	25°C, -40°C to 100°C	01	t _{c(H)} +6	ns	
				25°C, -55°C to 125°C	02	t _{c(H)} +5		
			TCLK int	25°C, -40°C to 100°C	01	[t _{c(TCLK)/2]-4}		[t _{c(TCLK)/2]+4}
				25°C, -55°C to 125°C	02	[t _{c(TCLK)/2]-4}		[t _{c(TCLK)/2]+4}
Switching characteristics over recommended operating conditions for SHZ								
Disable time, SHZ low to all outputs, I/O pins disabled (high impedance) <u>8/</u>	t _{dis(SHZ)}	See figure 4	25°C, -40°C to 100°C	01	0	8	ns	
			25°C, -55°C to 125°C	02	0	8		
Timing for test access port								
Setup time, TMS/TDI to TCK high <u>8/</u>	t _{su(TMh-TCKH)}	See figure 4	25°C, -40°C to 100°C	01	5		ns	
			25°C, -55°C to 125°C	02	5			
Hold time, TMS/TDI from TCK high <u>8/</u>	t _{h(TCKH-TMh)}		25°C, -40°C to 100°C	01	5		ns	
			25°C, -55°C to 125°C	02	5			
Delay time, TCK low to TDO valid <u>8/</u>	t _{d(TCKL-TDOV)}		25°C, -40°C to 100°C	01	0	10	ns	
			25°C, -55°C to 125°C	02	0	10		
Rise time, TCK <u>8/</u>	t _{r(TCK)}		25°C, -40°C to 100°C	01		3	ns	
			25°C, -55°C to 125°C	02		3		
Fall time, TCK <u>8/</u>	t _{f(TCK)}		25°C, -40°C to 100°C	01		3	ns	
			25°C, -55°C to 125°C	02		3		

See footnotes on next page.

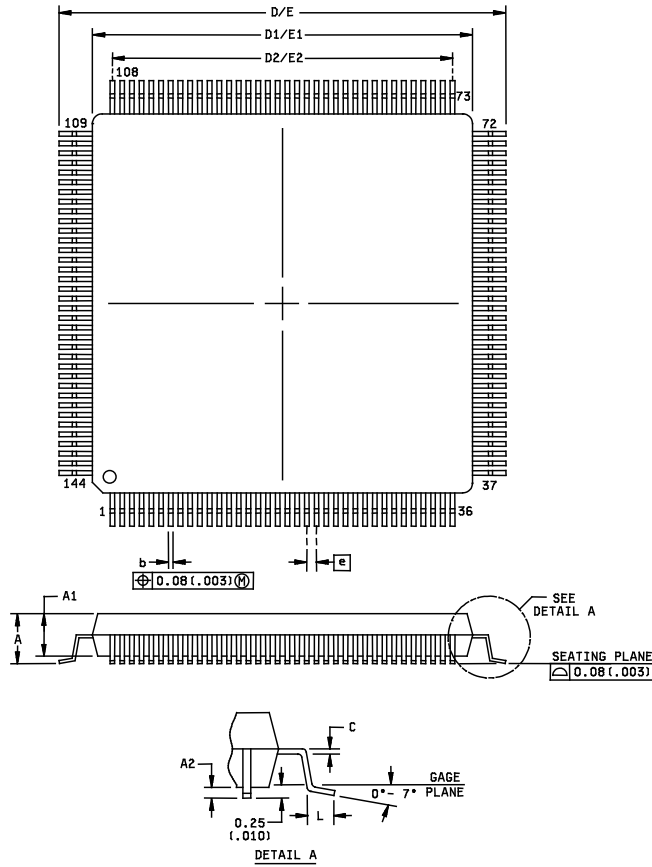
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 19

TABLE I. Electrical performance characteristics - Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ All voltage values are with respect to V_{SS} .
- 3/ For test conditions shown as Min or Max, use the appropriate value specified in section 1.4, herein.
- 4/ Pins with internal pullup devices: TDI, TCK, and TMS. Pins with internal pulldown devices: \overline{TRST} .
- 5/ Pins D0 – D31 include internal bus keepers that maintain valid logic levels when the bus is not driven.
- 6/ Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern at the maximum rate possible.
- 7/ f_x is the PLL output clock frequency.
- 8/ Not production tested.
- 9/ Duty cycle is defined as $100xt_1/(t_1+t_2)\%$.
- 10/ This circuit is intended for series resonant fundamental mode operation.
- 11/ Signal amplitude is dependent on the crystal and load used.
- 12/ These timings assume a similar loading of 30 pF on all pins.
- 13/ $P = t_{c(H)}/2$ (when duty cycle equals 50%).
- 14/ XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store is not driven until the store can execute.
- 15/ $P = t_{c(EXTCLK)}$.
- 16/ High impedance for data bus is limited to nominal bus keeper $Z_{OUT} = 15 \text{ k}\Omega$.
- 17/ Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
- 18/ $P = t_{c(H)}$.
- 19/ A cycle time of $t_{c(H)} \times 2$ is possible when the device is operated at lower CPU frequencies.
- 20/ Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.
- 21/ These requirements are applicable for a synchronous input clock.
- 22/ These requirements are applicable for an asynchronous input clock.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.60	D/E	21.80	22.20
A1	1.35	1.45	D1/E1	19.80	20.20
A2	0.05		D2/E2	17.50 TYP	
b	0.17	0.27	e	0.59 BSC	
c	0.13 NOM		L	0.45	0.75

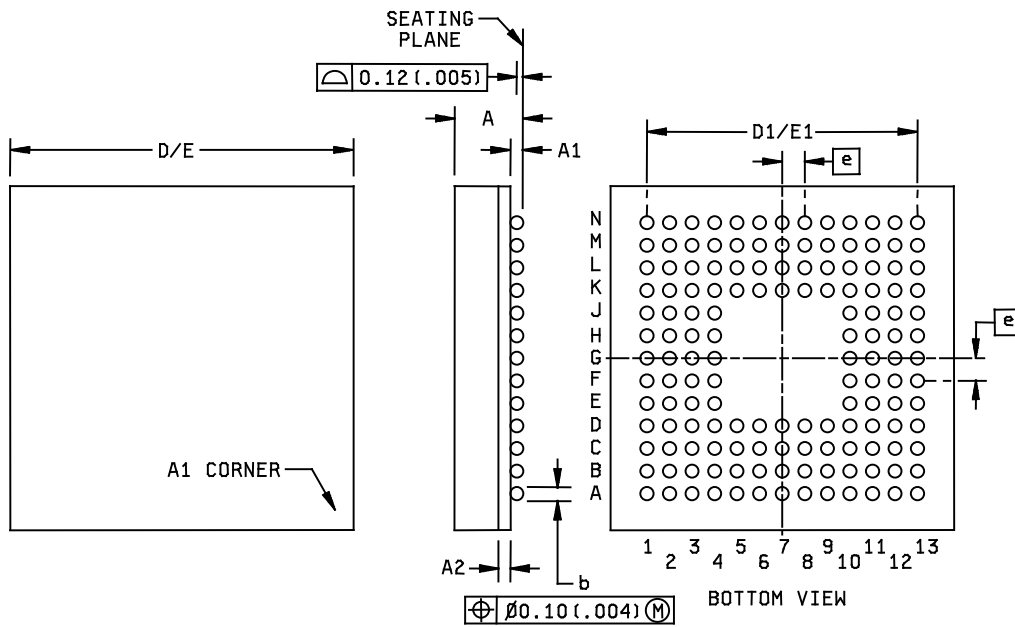
NOTES:

1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Fall within JEDEC MS-026.

FIGURE 1. Case outlines.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 21

Case Y



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		2.40	D/E	11.85	12.15
A1	0.35	0.50	D1/E1	9.60 TYP	
A2	0.34	0.56	e	0.80 BSC	
b	0.45	0.55			

NOTES:

1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.

FIGURE 1. Case outlines - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 22

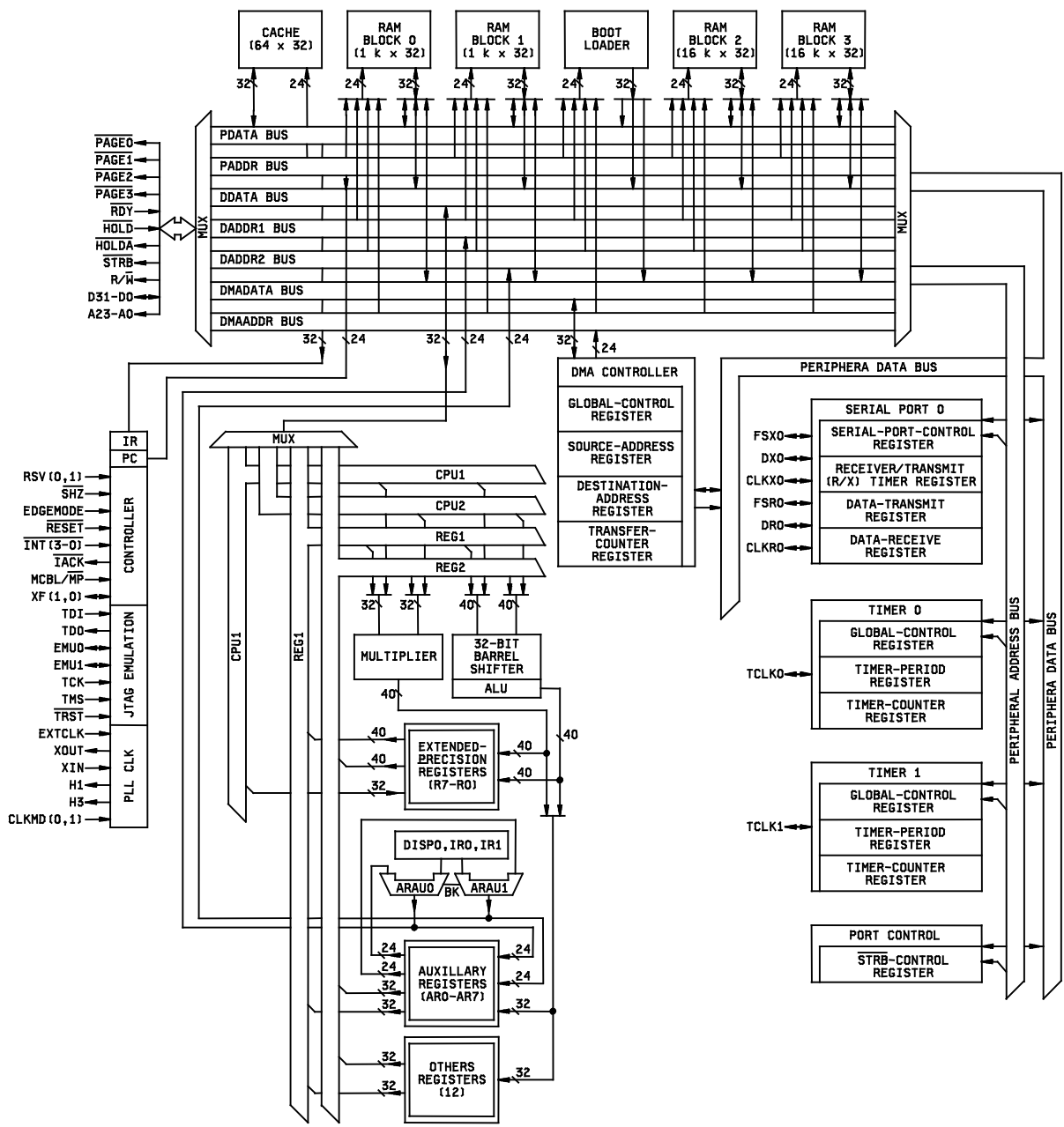


FIGURE 2. Functional block diagram.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03610</p>
		<p>REV C</p>	<p>PAGE 23</p>

Case X

Pin number	Pin name 1/	Pin number	Pin name 1/	Pin number	Pin name 1/	Pin number	Pin name 1/
1	A20	37	DV _{DD}	73	D15	109	CLKX0
2	V _{SS}	38	H1	74	D14	110	FSX0
3	A19	39	H3	75	D13	111	DX0
4	A18	40	V _{SS}	76	D12	112	V _{SS}
5	A17	41	$\overline{\text{STRB}}$	77	DV _{DD}	113	TCLK1
6	DV _{DD}	42	R/ $\overline{\text{W}}$	78	D11	114	TCLK0
7	A16	43	DV _{DD}	79	D10	115	DV _{DD}
8	A15	44	$\overline{\text{IACK}}$	80	V _{SS}	116	XF1
9	V _{SS}	45	$\overline{\text{RDY}}$	81	D9	117	XF0
10	A14	46	CV _{DD}	82	D8	118	V _{SS}
11	A13	47	$\overline{\text{HOLD}}$	83	CV _{DD}	119	$\overline{\text{INT3}}$
12	CV _{DD}	48	$\overline{\text{HOLDA}}$	84	D7	120	$\overline{\text{INT2}}$
13	A12	49	V _{SS}	85	D6	121	$\overline{\text{INT1}}$
14	A11	50	D31	86	DV _{DD}	122	$\overline{\text{INT0}}$
15	DV _{DD}	51	D30	87	D5	123	CV _{DD}
16	A10	52	D29	88	D4	124	EDGEMODE
17	A9	53	DV _{DD}	89	V _{SS}	125	MCBL/ $\overline{\text{MP}}$
18	V _{SS}	54	D28	90	D3	126	V _{SS}
19	A8	55	D27	91	D2	127	$\overline{\text{RESET}}$
20	A7	56	V _{SS}	92	D1	128	$\overline{\text{SHZ}}$
21	A6	57	D26	93	D0	129	DV _{DD}
22	A5	58	D25	94	DV _{DD}	130	EXTCLK
23	DV _{DD}	59	D24	95	EMU1	131	PLL _{VDD} 2/
24	A4	60	DV _{DD}	96	EMU0	132	XOUT
25	V _{SS}	61	D23	97	V _{SS}	133	XIN
26	A3	62	D22	98	TCK	134	PLL _{VSS} 2/
27	A2	63	V _{SS}	99	TDO	135	CLKMD1
28	CV _{DD}	64	D21	100	TDI	136	CLKMD0
29	A1	65	D20	101	CV _{DD}	137	CV _{DD}
30	A0	66	CV _{DD}	102	TMS	138	RSV1
31	DV _{DD}	67	D19	103	$\overline{\text{TRST}}$	139	RSV0
32	$\overline{\text{PAGE3}}$	68	D18	104	DR0	140	V _{SS}
33	$\overline{\text{PAGE2}}$	69	DV _{DD}	105	V _{SS}	141	A23
34	V _{SS}	70	D17	106	FSR0	142	A22
35	$\overline{\text{PAGE1}}$	71	D16	107	CLKR0	143	DV _{DD}
36	$\overline{\text{PAGE0}}$	72	V _{SS}	108	DV _{DD}	144	A21

- 1/ DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.
- 2/ PLL_{VDD} and PLL_{VSS} are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

FIGURE 3. Terminal connections – Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 24

Case Y

Pin number	Pin name 1/	Pin number	Pin name 1/	Pin number	Pin name 1/	Pin number	Pin name 1/
A1	DV _{DD}	C11	V _{SS}	G10	D1	L4	R/ \bar{W}
A2	A22	C12	FSR0	G11	D3	L5	CV _{DD}
A3	CV _{DD}	C13	\bar{TRST}	G12	D0	L6	D29
A4	PLL _{VSS} 2/	D1	V _{SS}	G13	V _{SS}	L7	V _{SS}
A5	PLL _{VDD} 2/	D2	DV _{DD}	H1	A6	L8	D25
A6	DV _{DD}	D3	A18	H2	DV _{DD}	L9	CV _{DD}
A7	EDGEMODE	D4	A21	H3	A5	L10	D17
A8	CV _{DD}	D5	RSV1	H4	A4	L11	D14
A9	$\bar{INT3}$	D6	XOUT	H10	D4	L12	D15
A10	DV _{DD}	D7	\bar{SHZ}	H11	DV _{DD}	L13	DV _{DD}
A11	TCLK1	D8	$\bar{INT2}$	H12	D6	M1	DV _{DD}
A12	DX	D9	XF1	H13	D5	M2	$\bar{PAGE0}$
A13	V _{SS}	D10	FSX	J1	V _{SS}	M3	V _{SS}
B1	V _{SS}	D11	DR0	J2	A0	M4	\bar{STRB}
B2	A20	D12	CV _{DD}	J3	CV _{DD}	M5	\bar{RDY}
B3	A23	D13	TDO	J4	A3	M6	V _{SS}
B4	RSV0	E1	A13	J10	D7	M7	D27
B5	CLKMD1	E2	A14	J11	D8	M8	DV _{DD}
B6	XIN	E3	CV _{DD}	J12	D9	M9	D24
B7	\bar{RESET}	E4	A15	J13	CV _{DD}	M10	D21
B8	$\bar{MCBL/MP}$	E10	TMS	K1	A2	M11	D20
B9	$\bar{INT1}$	E11	TDI	K2	A1	M12	D16
B10	XF0	E12	EMU1	K3	$\bar{PAGE3}$	M13	D13
B11	CLKX0	E13	V _{SS}	K4	\bar{IACK}	N1	DV _{DD}
B12	DV _{DD}	F1	DV _{DD}	K5	\bar{HOLDA}	N2	H3
B13	CLKR0	F2	A12	K6	D31	N3	$\bar{PAGE1}$
C1	A16	F3	A10	K7	D28	N4	DV _{DD}
C2	A17	F4	A11	K8	D22	N5	\bar{HOLD}
C3	A19	F10	TCK	K9	D18	N6	D30
C4	V _{SS}	F11	DV _{DD}	K10	D12	N7	DV _{DD}
C5	CLKMD0	F12	EMU0	K11	V _{SS}	N8	D26
C6	EXTCLK	F13	D2	K12	D11	N9	D23
C7	V _{SS}	G1	A8	K13	D10	N10	V _{SS}
C8	$\bar{INT0}$	G2	A9	L1	$\bar{PAGE2}$	N11	D19
C9	V _{SS}	G3	V _{SS}	L2	V _{SS}	N12	DV _{DD}
C10	TCLK0	G4	A7	L3	H1	N13	V _{SS}

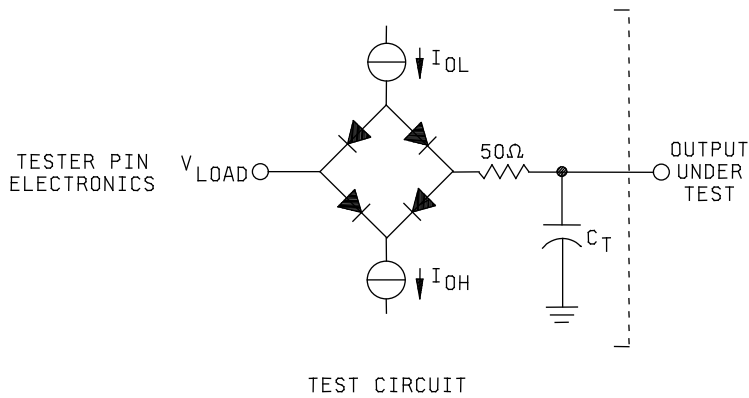
1/ DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

2/ PLL_{VDD} and PLL_{VSS} are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

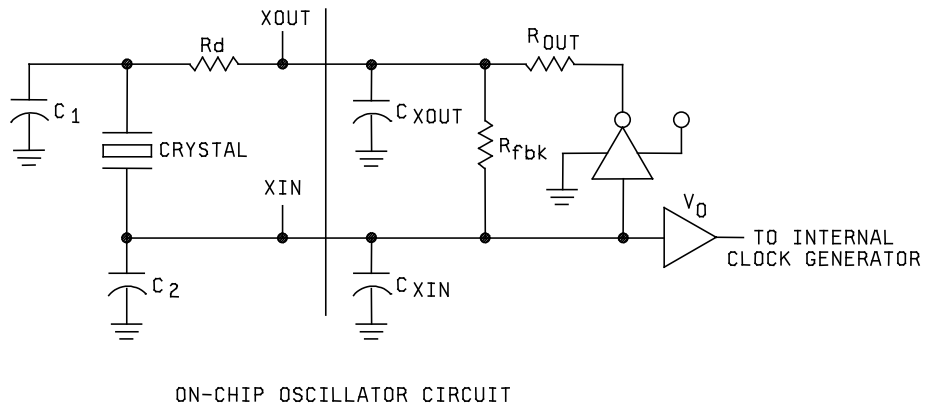
FIGURE 3. Terminal connections – Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 25

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 26



NOTES: $I_{OL} = 4.0$ mA (all outputs) for dc levels test.
 I_{OL} and I_{OH} are adjusted during ac timing analysis to achieve an ac termination of 50Ω .
 $V_{LOAD} = DV_{DD}/2$.
 $C_T = 40$ pF, typical load-circuit capacitance.



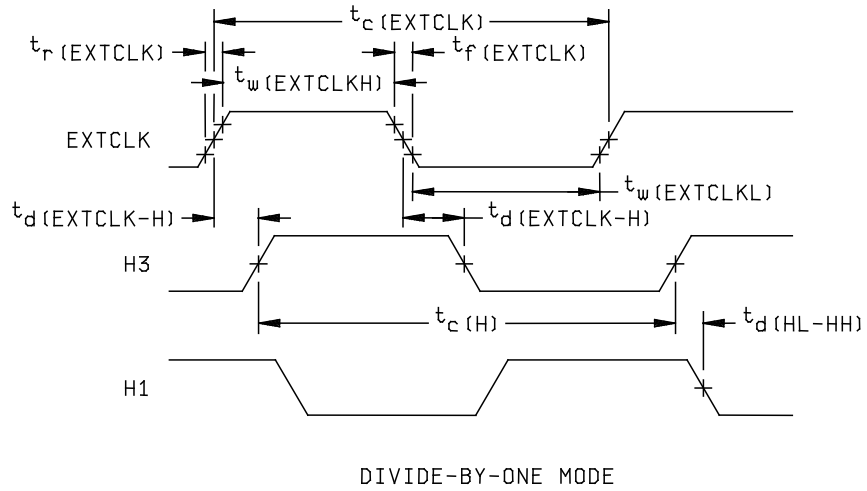
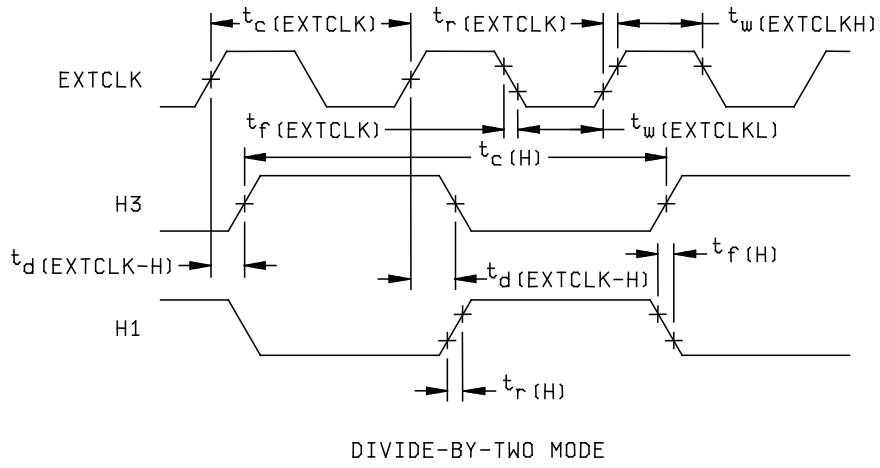
Frequency (MHz)	R_d (Ω)	C_1 (pF)	C_2 (pF)	CL (pF) ^{1/}	RL (Ω) ^{1/}
2	4700	18	18	12	200
5	2200	18	18	12	60
10	470	15	15	12	30
15	0	15	12	12	25
20	0	9	9	10	25

^{1/} CL and RL are typical internal series load capacitance and resistance of the crystal.

TYPICAL CRYSTAL CIRCUIT LOADING

FIGURE 4. Test circuit and timing waveforms.

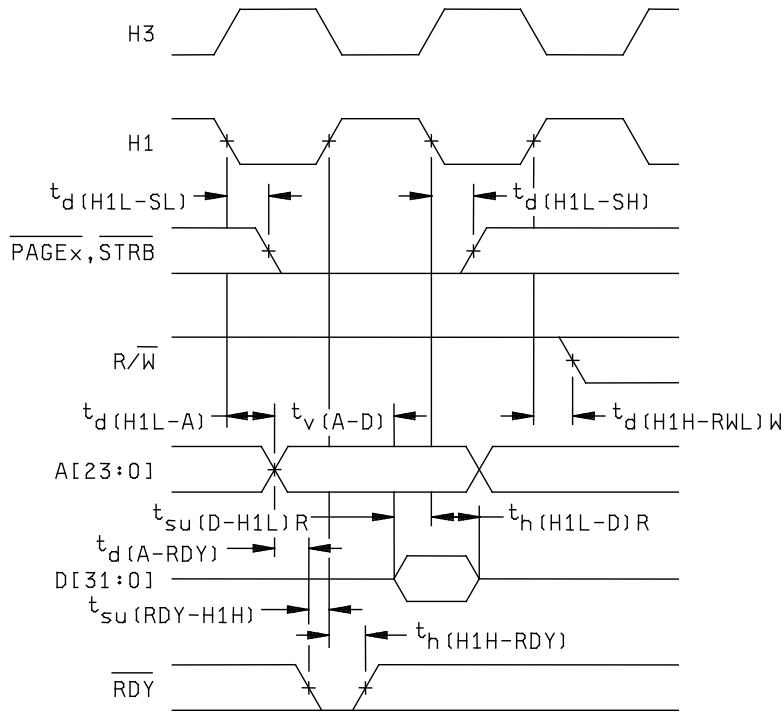
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 27



NOTE: EXTCLK is held low.

FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 28

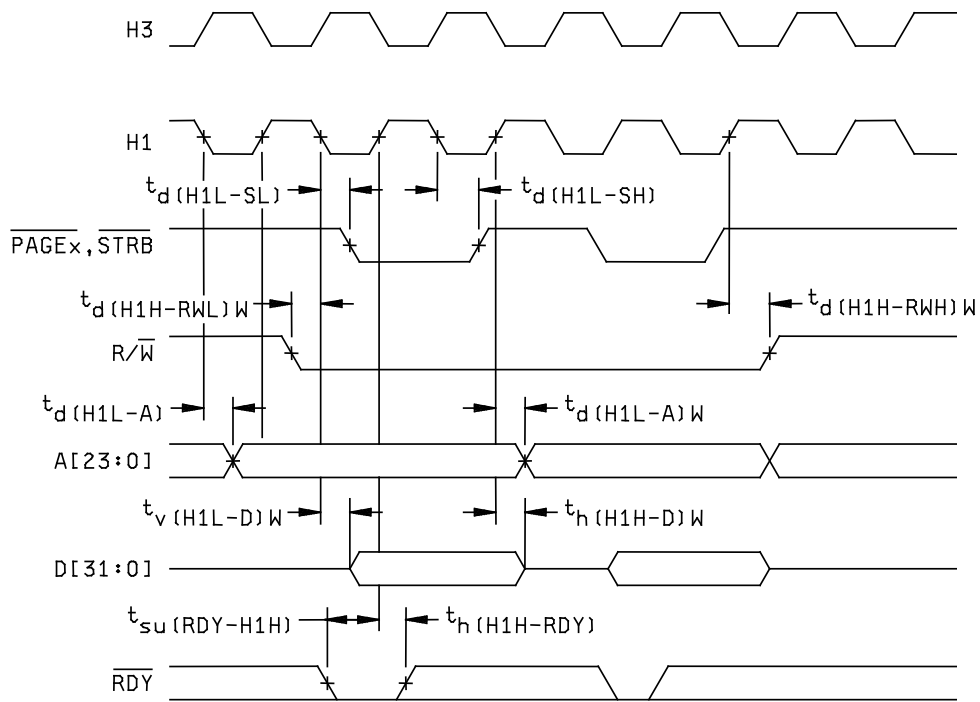


TIMING FOR MEMORY ($\overline{STRB}=0$ AND $\overline{PAGE}_x=0$) READ

NOTE: \overline{STRB} remains low during back-to-back read operation.

FIGURE 4. Test circuit and timing waveforms - Continued.

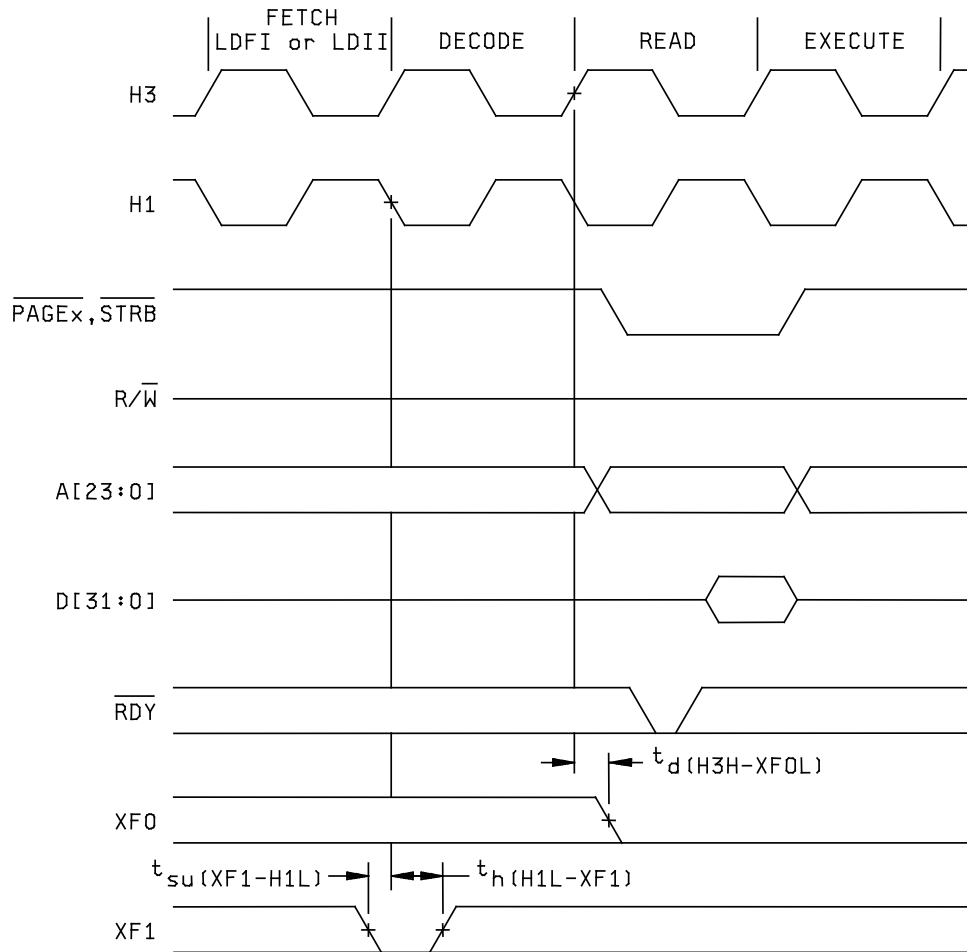
<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03610</p>
		<p>REV C</p>	<p>PAGE 29</p>



TIMING FOR MEMORY ($\overline{STRB}=0$ AND $\overline{PAGEx}=0$) WRITE

FIGURE 4. Test circuit and timing waveforms - Continued.

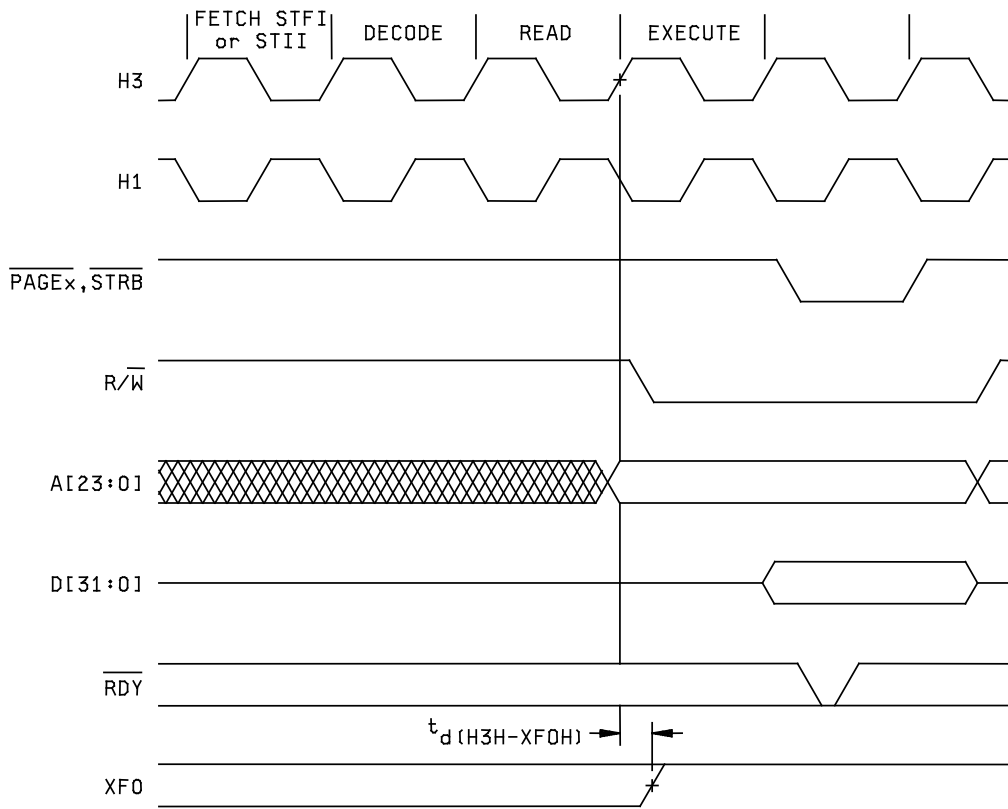
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 30



TIMING FOR XFO AND XF1 WHEN EXECUTING LDFI OR LDII

FIGURE 4. Test circuit and timing waveforms - Continued.

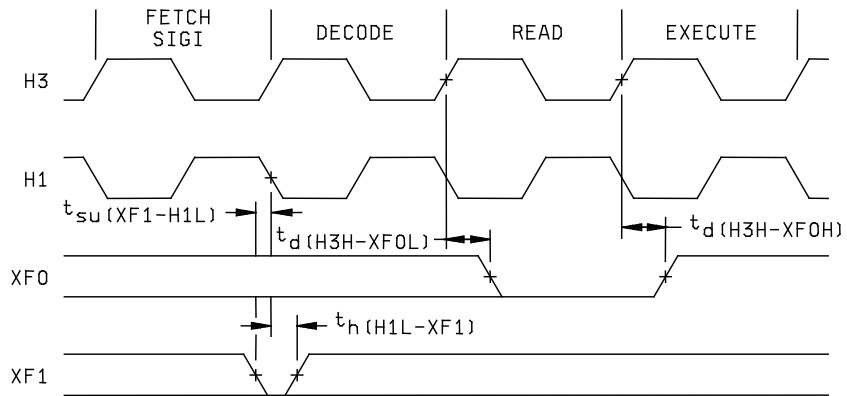
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 31



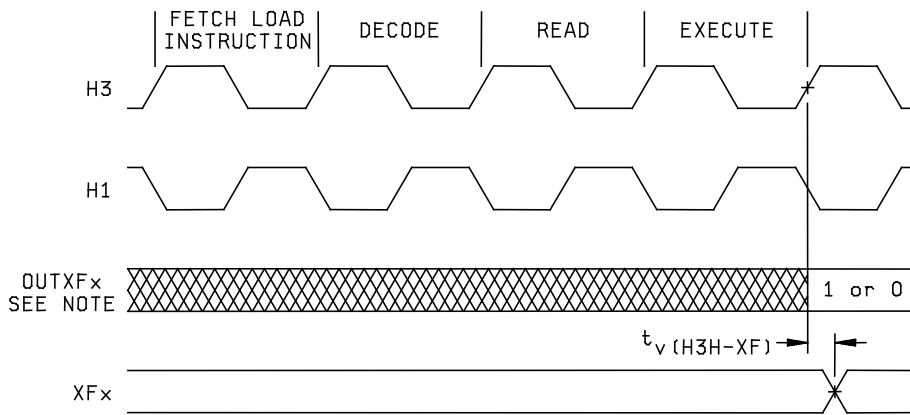
TIMING FOR XFO WHEN EXECUTING AN STFI OR STII

FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 32



TIMING FOR XFO AND XF1 WHEN EXECUTING SIGI

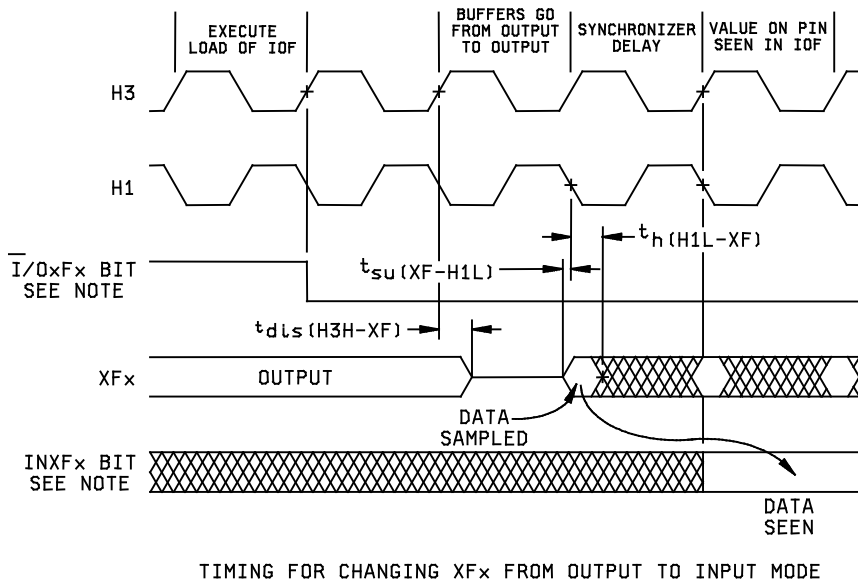


TIMING FOR LOADING XF REGISTER WHEN CONFIGURED AS AN OUTPUT PIN

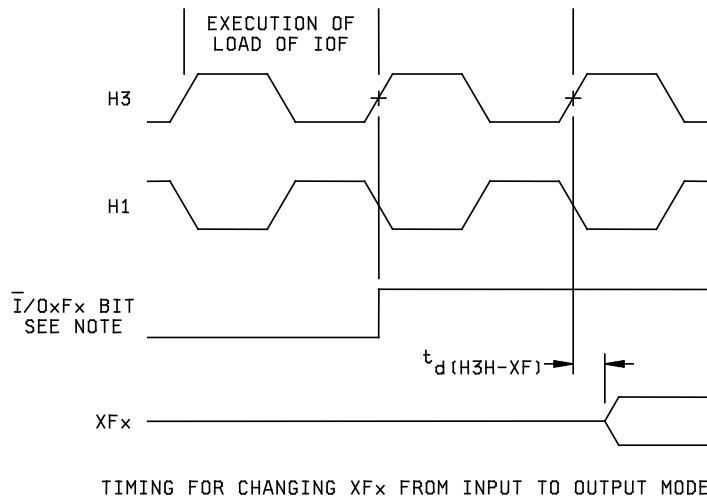
NOTE: OUTXF_x represents either bit 2 or 6 of the IOF register.

FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 33



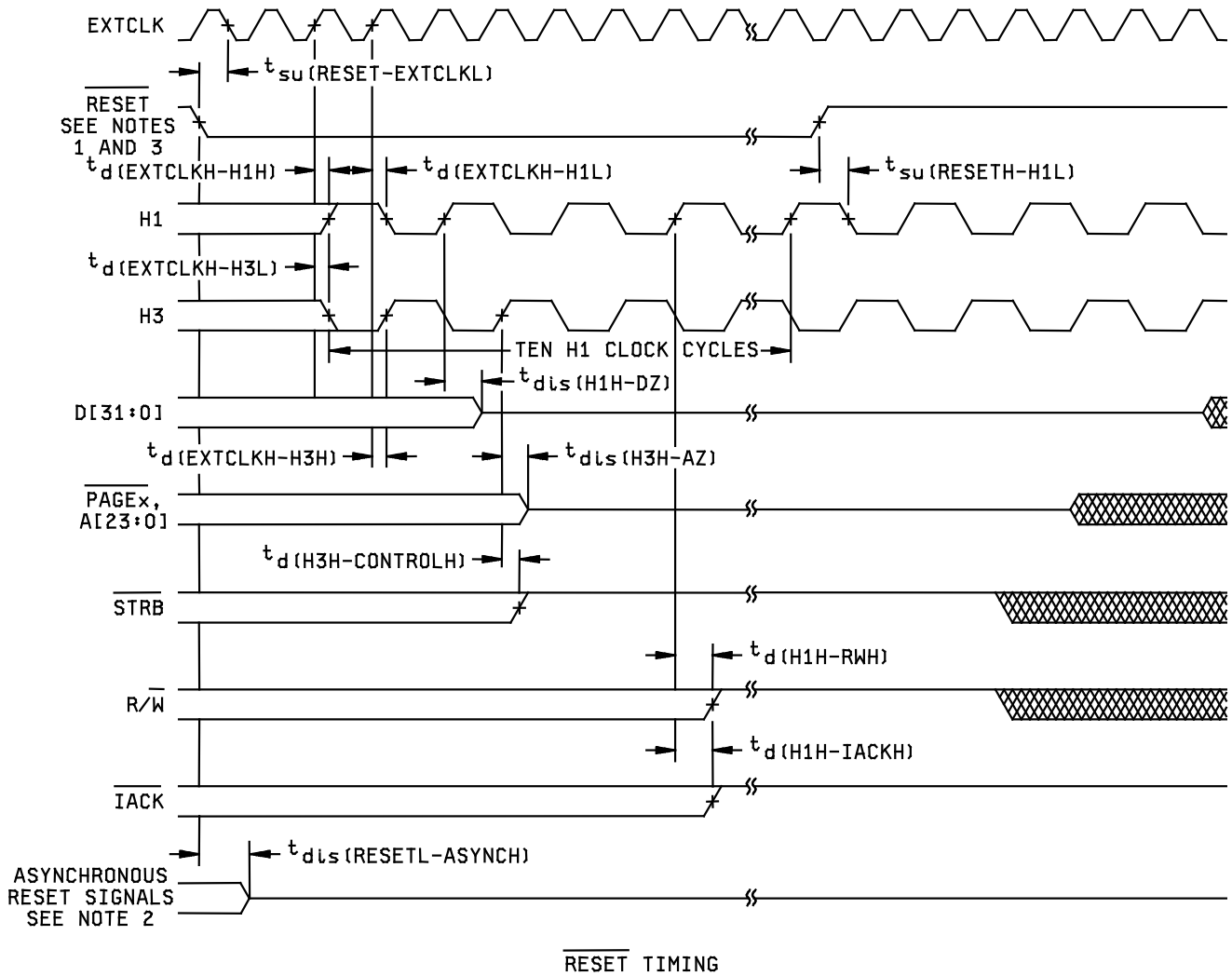
NOTE: \bar{I}/OxF_x represents either bit 1 or bit 5 of the IOF register, and $INxF_x$ represents either bit 3 or bit 7 of the IOF register.



NOTE: \bar{I}/OxF_x represents either bit 1 or bit 5 of the IOF register.

FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE	CODE IDENT NO.	DWG NO.
	A	16236	V62/03610
	REV	C	PAGE 34

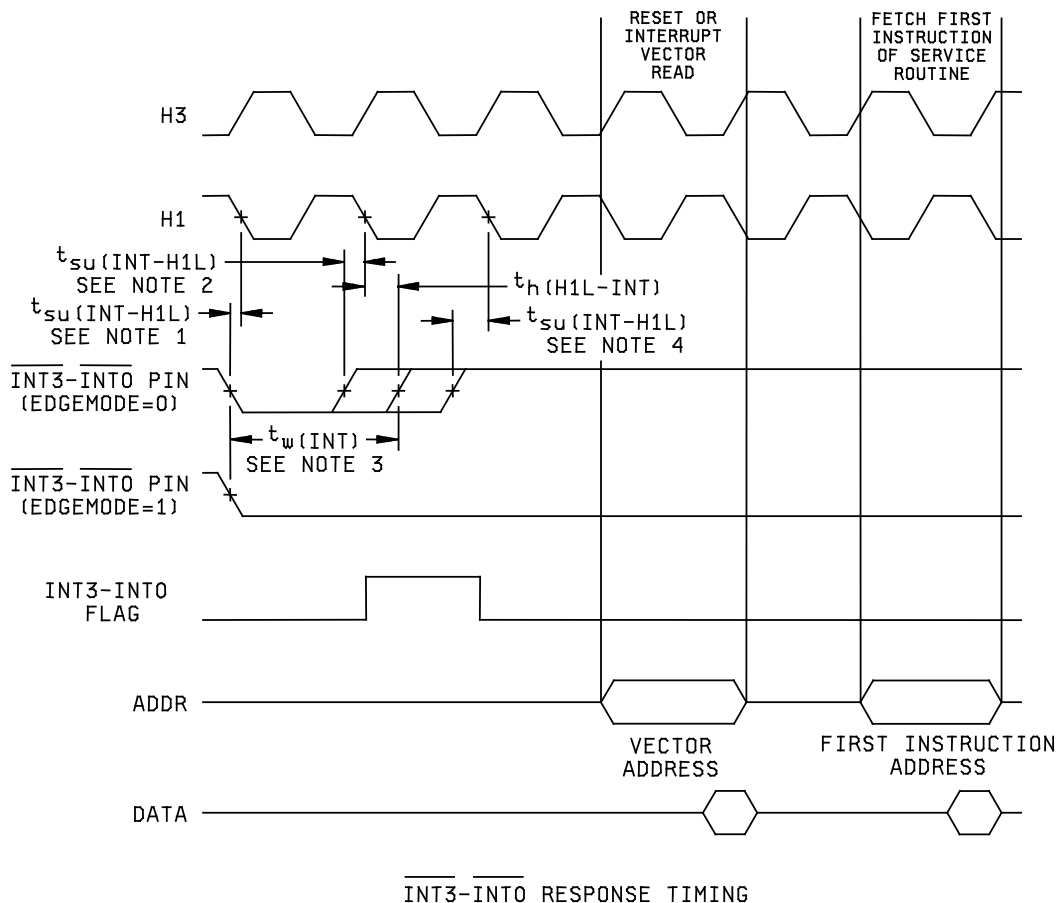


NOTES:

1. Clock circuit is configured in 'C31-compatible divide-by-2 mode. If configured for x1 mode, EXTCLK directly drives H3.
2. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
3. $\overline{\text{RESET}}$ is a synchronous input that can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
4. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
5. The address and $\text{PAGE3} - \text{PAGE0}$ outputs are placed in a high-impedance state during reset requiring a nominal 10-22 k Ω pullup. If not, undesirable spurious reads can occur when these outputs are not driven.

FIGURE 4. Test circuit and timing waveforms - Continued.

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NOTES:

1. Falling edge of H1 just detects $\overline{\text{INTx}}$ falling edge.
2. Falling edge of H1 detects second $\overline{\text{INTx}}$ low, however flag clear takes precedence.
3. Nominal width.
4. Falling edge of H1 misses previous $\overline{\text{INTx}}$ low as $\overline{\text{INTx}}$ rises.

FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
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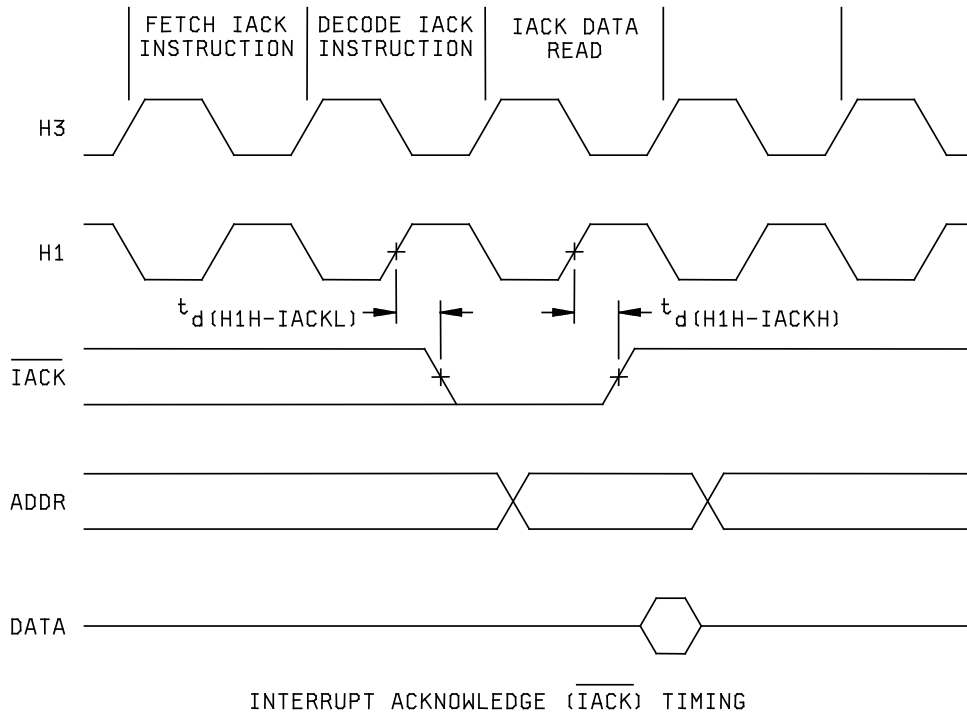
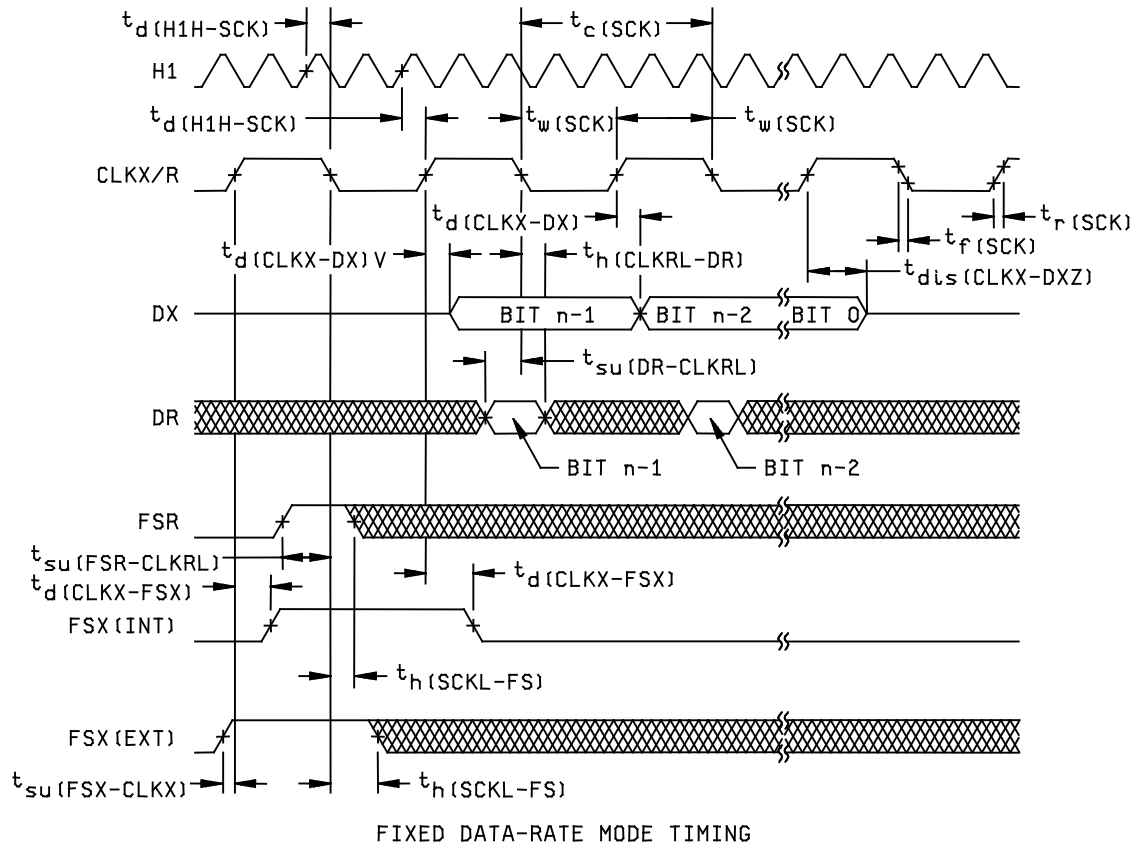


FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV C	PAGE 37

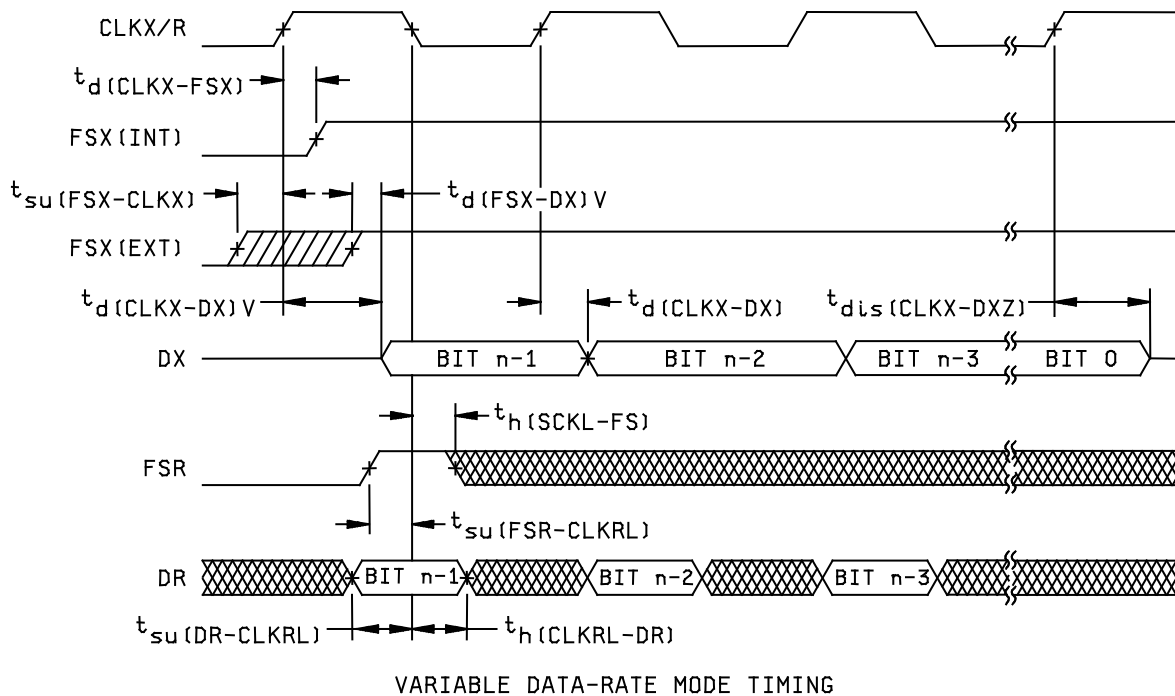


NOTES:

1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
2. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE	CODE IDENT NO.	DWG NO.
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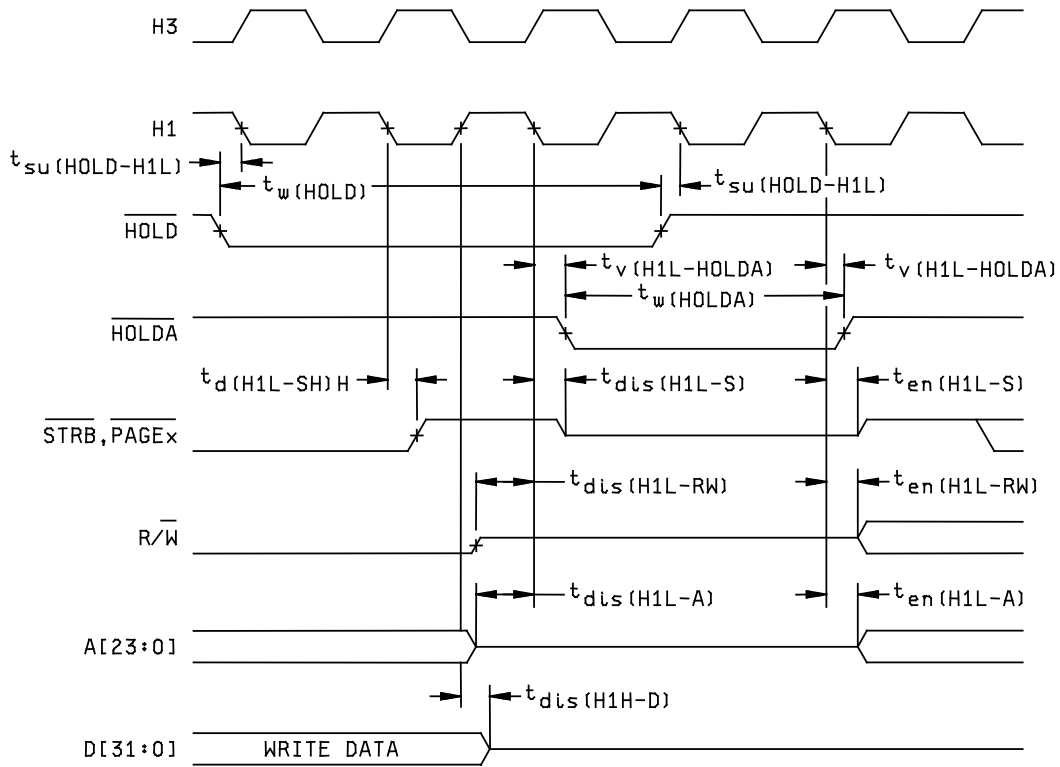


NOTES:

1. Timing diagrams show operations with $\text{CLKXP} = \text{CLKRP} = \text{FSXP} = \text{FSRP} = 0$.
2. Timing diagrams depend on the length of the serial-port word, where $n = 8, 16, 24,$ or 32 bits, respectively.
3. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
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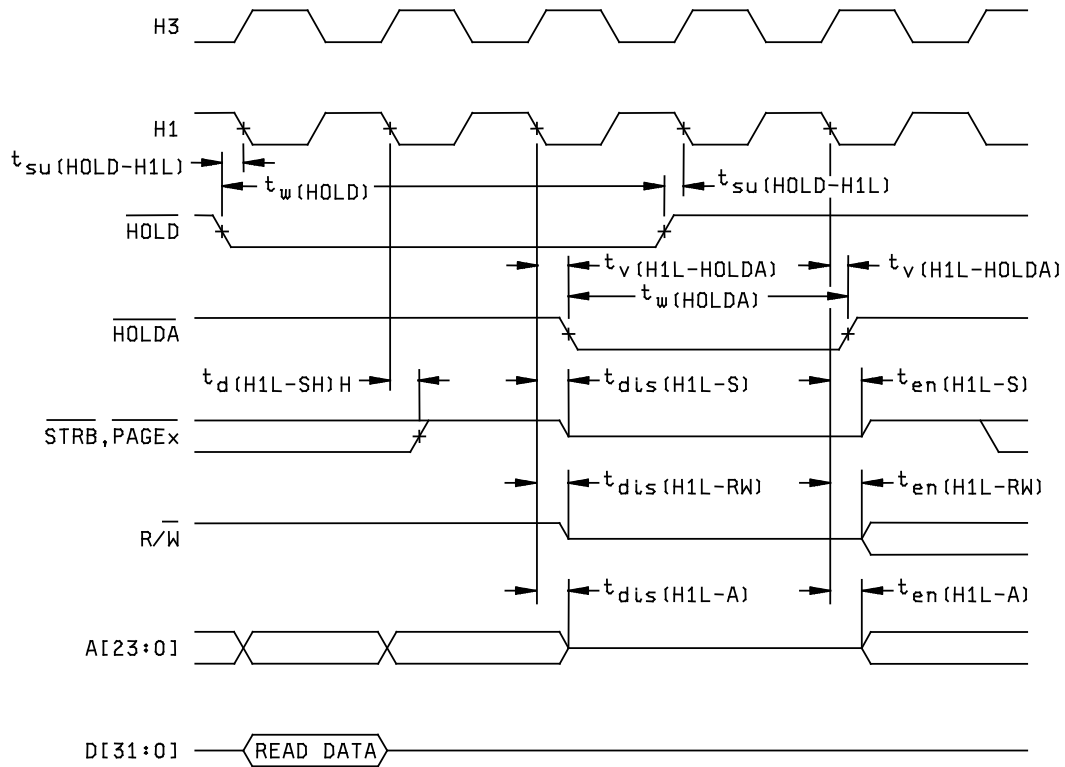


TIMING FOR $\overline{HOLD}/\overline{HOLDA}$ (AFTER WRITE)

NOTE: \overline{HOLDA} goes low in response to \overline{HOLD} going low and continues to remain low until one H1 cycle after \overline{HOLD} goes back high.

FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
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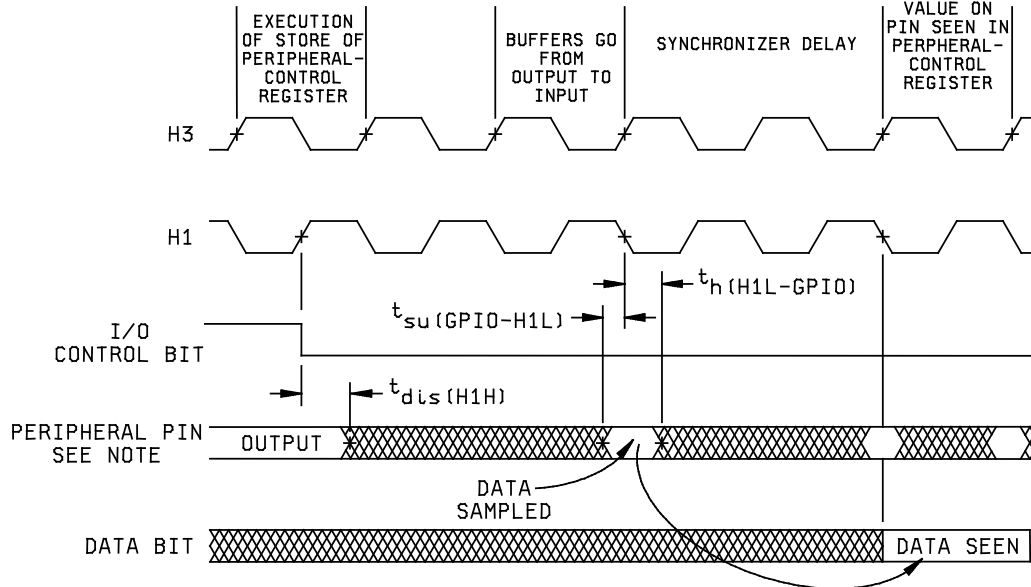


TIMING FOR $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ (AFTER READ)

NOTE: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

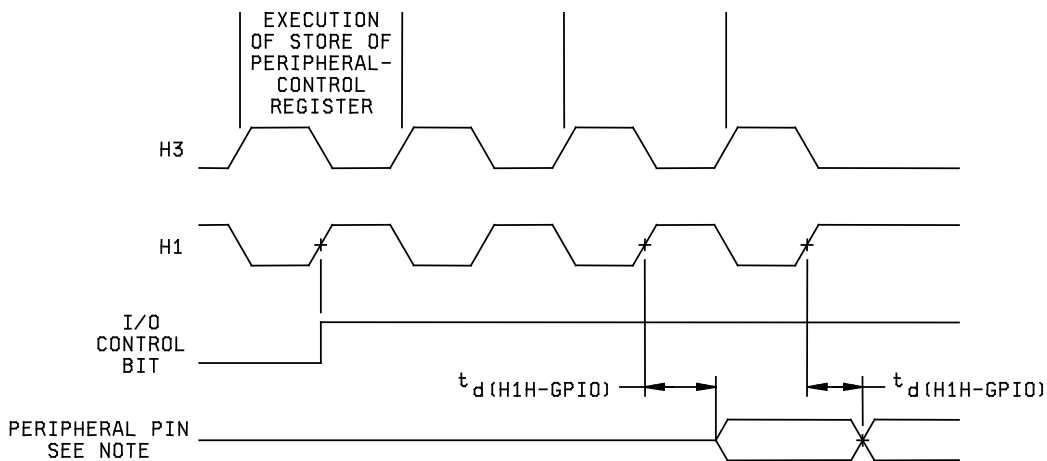
FIGURE 4. Test circuit and timing waveforms - Continued.

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CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE OUTPUT TO INPUT MODE TIMING

NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

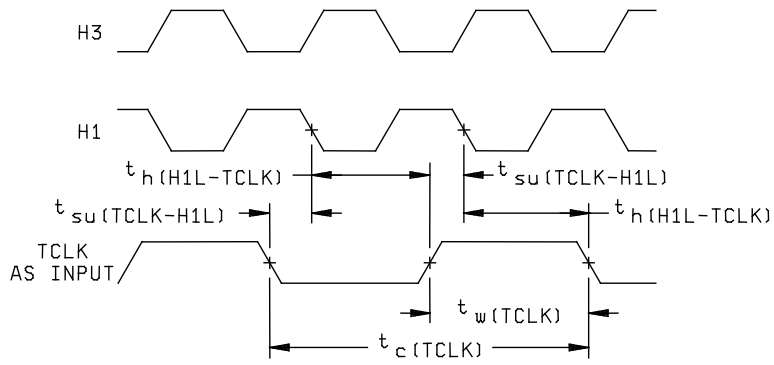


CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE INPUT TO OUTPUT MODE TIMING

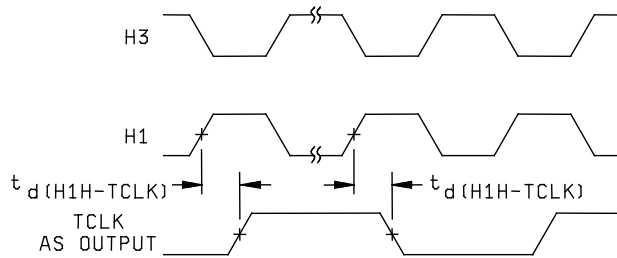
NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

FIGURE 4. Test circuit and timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE	CODE IDENT NO.	DWG NO.
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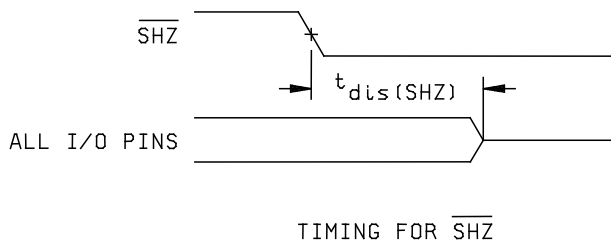
TIMER PIN TIMING, INPUT



TIMER PIN TIMING, OUTPUT

FIGURE 4. Test circuit and timing waveforms - Continued.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03610</p>
		<p>REV C</p>	<p>PAGE 43</p>



NOTE: Enabling $\overline{\text{SHZ}}$ destroys the device register and memory contents. Assert $\overline{\text{SHZ}} = 1$ and reset the device to restore it to a known condition.

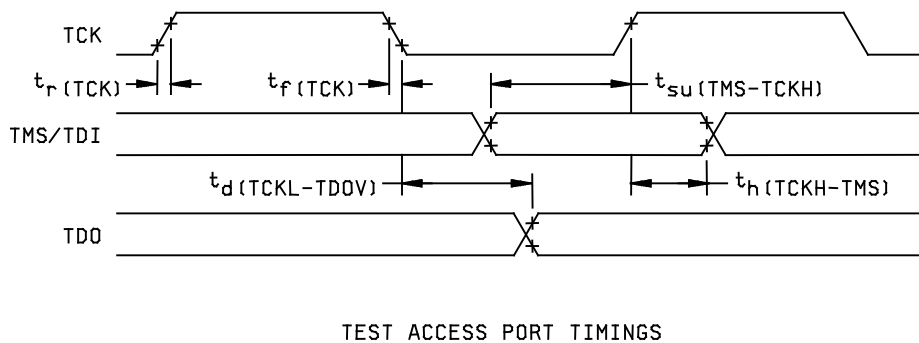


FIGURE 4. Test circuit and timing waveforms - Continued.

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Instruction name	Instruction code
EXTEST	00000000
BYPASS	11111111
SAMPLE	00000010
HIGHZ	00000110
PRIVATE1 <u>1/</u>	00000011
PRIVATE2 <u>1/</u>	00100000
PRIVATE3 <u>1/</u>	00100001
PRIVATE4 <u>1/</u>	00100010
PRIVATE5 <u>1/</u>	00100011
PRIVATE6 <u>1/</u>	00100100
PRIVATE7 <u>1/</u>	00100101
PRIVATE8 <u>1/</u>	00100110
PRIVATE9 <u>1/</u>	00100111
PRIVATE10 <u>1/</u>	00101000
PRIVATE11 <u>1/</u>	00101001

Boundary is only one dummy cell

Boundary is only one dummy cell

1/ Use of private opcodes could cause the device to operate in an unexpected manner.

FIGURE 5. Boundary scan instruction code.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Terminal functions. The terminal functions used herein are defined in the following table II.

TABLE II. Terminal functions.

Terminal name	Type <u>1/</u>	Description	Conditions when signal is Z type <u>2/</u>
Primary-bus interface			
D31 – D0	I/O/Z	32-bit data port.	S H R
		Data port bus keepers.	S
A23 – A0	O/Z	24-bit address port.	S H R
R/ \overline{W}	O/Z	Read/Write. $\overline{R/\overline{W}}$ is high when a read is performed and low when a write is performed over the parallel interface.	S H R
\overline{STRB}	O/Z	Strobe. For all external-accesses.	S H
$\overline{PAGE0}$ - $\overline{PAGE3}$	O/Z	Page strobes. Four decoded page strobes for external access.	S H R
\overline{RDY}	I	Ready. \overline{RDY} indicates that the external device is prepared for a transaction completion.	
\overline{HOLD}	I	Hold. When \overline{HOLD} is a logic low, any ongoing transaction is completed. A23 – A0, D31 – D0, \overline{STRB} , and R/ \overline{W} are placed in the high-impedance state and all transactions over the primary-bus interface are held until \overline{HOLD} becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.	

See footnotes at end table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
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TABLE II. Terminal functions - Continued.

Terminal name	Type <u>1/</u>	Description	Conditions when signal is Z type <u>2/</u>	
Primary-bus interface – Continued				
$\overline{\text{HOLDA}}$	O/Z	Hold acknowledge. $\overline{\text{HOLDA}}$ is generated in response to a logic-low on $\overline{\text{HOLD}}$. $\overline{\text{HOLDA}}$ indicates that A23 – A0, D31 – D0, $\overline{\text{STRB}}$, and R/ $\overline{\text{W}}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{\text{HOLDA}}$ is high in response to a logic-high of $\overline{\text{HOLD}}$ or the NOHOLD bit of the primary-bus-control register is set.	S	
Control signals				
$\overline{\text{RESET}}$	I	Reset. When $\overline{\text{RESET}}$ is a logic low, the device is in the reset condition. When $\overline{\text{RESET}}$ becomes a logic high, execution begins from the location specified by the reset vector.		
EDGEMODE	I	Edge mode. Enables interrupt edge mode detection.		
$\overline{\text{INT3}}$ - $\overline{\text{INT0}}$	I	External interrupts.		
$\overline{\text{IACK}}$	O/Z	Internal acknowledge. $\overline{\text{IACK}}$ is generated by the IACK instruction. $\overline{\text{IACK}}$ can be used to indicate when a section of code is being executed.	S	
MCBL/ $\overline{\text{MP}}$	I	Microcomputer bootloader/microprocessor mode-select.		
$\overline{\text{SHZ}}$	I	Shutdown high impedance. When active, $\overline{\text{SHZ}}$ places all pins in the high-impedance state. $\overline{\text{SHZ}}$ can be used for board-level testing or to ensure that no dual-drive conditions occur. Caution: A low on $\overline{\text{SHZ}}$ corrupts the device memory and register contents. Reset the device with $\overline{\text{SHZ}}$ high to restore it to a known operating condition.		
XF1, XF0	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S	R
Serial port 0 signals				
CLKR0	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S	R
CLKX0	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S	R
DR0	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S	R
DX0	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S	R
FSR0	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S	R
FSX0	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S	R

See footnotes at end table.

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TABLE II. Terminal functions - Continued.

Terminal name	Type ^{1/}	Description	Conditions when signal is Z type ^{2/}
Timer signals			
TCLK0	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S R
TCLK1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S R
Supply and oscillator signals			
H1	O/Z	External H1 clock.	S
H3	O/Z	External H3 clock.	S
CV _{DD}	I	+V _{DD} . Dedicated 1.8-V power supply for the core CPU. All must be connected to a common supply plane. ^{3/}	
DV _{DD}	I	+V _{DD} . Dedicated 3.3-V power supply for the I/O pins. All must be connected to a common supply plane. ^{3/}	
V _{SS}	I	Ground. All grounds must be connected to a common ground plane.	
PLL _{VDD}	I	Internally isolated PLL supply. Connect to CV _{DD} (1.8 V).	
PLL _{VSS}	I	Internally isolated PLL ground. Connect to V _{SS} .	
EXTCLK	I	External clock. Logic level compatible clock input. If the XIN/XOUT oscillator is used, tie this pin to ground.	
XOUT	O	Clock out. Output from the internal-crystal oscillator. If a crystal is not used, XOUT should be left unconnected.	
XIN	I	Clock in. Internal-oscillator input from a crystal. If EXTCLK is used, tie this pin to ground.	
CLKMD0, CLKMD1	I	Clock mode select pins.	
RSV0, RSV1	I	Reserved. Use individual pullups to DV _{DD} .	
JTAG emulation			
EMU1, EMU0	I/O	Emulation pins 0 and 1. Use individual pullups to DV _{DD} .	
TDI	I	Test data input.	
TDO	O	Test data output.	
TCK	I	Test clock.	
TMS	I	Test mode select.	
$\overline{\text{TRST}}$	I	Test reset.	

^{1/} I = input, O = output, Z = high-impedance state.

^{2/} S = SHZ active, H = HOLD active, R = RESET active.

^{3/} Recommended decoupling. Four 0.1 μ F for CV_{DD} and eight 0.1 μ F for DV_{DD}.

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6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03610-01XE	01295	SM320VC33PGEA120EP	SM320VC33PGEA120EP
V62/03610-02YF	01295	SM320VC33GNMM150EP	SM320VC33GNMM150EP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ Devices listed on this drawing are supplied to lead finish "F". The solder ball material contains compositions of Sn = 63% and Pb = 37%.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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