REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct lead finish on last page. Update boilerplate. - CFS	05-11-01	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	12-06-04	Thomas M. Hess
C	Update boilerplate paragraphs to current requirements. - PHN	18-01-16	Thomas M. Hess
D	Update boilerplate paragraphs to current VID description requirements. - PHN	23-05-22	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	D	D	D	D	D	D																
SHEET	23	24	25	26	27	28																
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 02-12-12	**CHECKED BY** TOM HESS **APPROVED BY** RAYMOND MONNIN	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, CMOS, 12-BIT, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON
	SIZE A / **CAGE CODE** 16236	**DWG NO.** V62/03609
	REV D	**PAGE** 1 OF 28

AMSC N/A

5962-V088--23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance linear-digital microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03609	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	THS1206-EP	CMOS, 12-bit, 6 MSPS, analog-to-digital converter

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	32	MO-153	Plastic thin shrink small outline package with gull wing leads

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range:
- DGND to DV_{DD} ..... -0.3 V to 6.5 V
- BGND to BV_{DD} ..... -0.3 V to 6.5 V
- AGND to AV_{DD} ..... -0.3 V to 6.5 V

Analog input voltage range ..... AGND – 0.3 V to AV_{DD} + 1.5 V
Reference input voltage ..... -0.3 V + AGND to AV_{DD} + 0.3 V
Digital input voltage range ..... -0.3 V to BV_{DD} / DV_{DD} + 0.3 V
Power dissipation (P_D) ($T_A \leq 25°C$) ..... 1453 mW 2/
Operating virtual junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature range ..... -65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C

1.4 Recommended operating conditions. 3/

Power supply section
Supply voltage:
- AV_{DD} ..... 4.75 V to 5.25 V
- DV_{DD} ..... 3 V to 5.25 V
- BV_{DD} ..... 3 V to 5.25 V

Analog and reference inputs section
Analog input voltage in single-ended configuration ..... V_{REFM} to V_{REFP}
Common-mode input voltage V_{CM} in differential configuration ..... 1 V to 4 V
External reference voltage, V_{REFP} ..... AV_{DD} – 1.2 V maximum
External reference voltage, V_{REFM} ..... 1.4 V minimum
Digital inputs section
High-level input voltage (V_{IH}):
- With BV_{DD} = 3.3 V ..... 2 V minimum
- With BV_{DD} = 5.25 V ..... 2.6 V minimum

Low-level input voltage (V_{IL})
- With BV_{DD} = 3.3 V ..... 0.6 V maximum
- With BV_{DD} = 5.25 V ..... 0.6 V maximum

Input CONV_CLK frequency, (with DV_{DD} = 3 V to 5.25 V) ..... 0.1 MHz to 6 MHz
CONV_CLK pulse duration, clock high, t_W (CONV_CLKH):
- With DV_{DD} = 3 V to 5.25 V ..... 80 ns to 5000 ns

CONV_CLK pulse duration, clock low, t_W (CONV_CLKL):
- With DV_{DD} = 3 V to 5.25 V ..... 80 ns to 5000 ns

Ambient operating temperature (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “ recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The derating factor above T_A = +25°C is 11.62 mW/°C.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https:/www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$	Limits		Unit
			Min	Max	
Digital input section					
High-level input current	I_{IH}	DV_{DD} = digital inputs	-50	50	µA
Low-level input current	I_{IL}	Digital input = 0 V	-50	50	µA
Input capacitance	C_{IN}		5 TYP		pF
High-level output voltage	V_{OH}	I_{OH} = -50 µA, BV_{DD} = 3.3 V	BV_{DD} – 0.5		V
		I_{OH} = -50 µA, BV_{DD} = 5 V	BV_{DD} – 0.5		
Low-level output voltage	V_{OL}	I_{OL} = 50 µA, BV_{DD} = 3.3 V		0.4	V
		I_{OL} = 50 µA, BV_{DD} = 5 V		0.4	
High-impedance-state output current	I_{OZ}	CS1 = DGND, CS0 = DV_{DD}	-10	10	µA
Output capacitance	C_{OUT}		5 TYP		pF
Load capacitance at databus D0 – D11	C_L			30	pF
Resolution	RES		12		Bits
Integral nonlinearity	INL			±1.8	LSB
Differential nonlinearity	DNL			±1	LSB
Offset error 2/	OE	After calibration in differential mode	-20	20	LSB
		After calibration in single-ended mode	20 TYP		
Gain error 2/	GE		-20	20	LSB
Analog input section					
Input capacitance	C_{IN}		15 TYP		
Input leakage current	I_{INL}	V_{AIN} = V_{REFM} to V_{REFP}		±10	µA
Internal voltage reference section					
Accuracy	V_{REFP}		3.3	3.7	V
	V_{REFM}		1.3	1.7	V
	REFOUT		2.3	2.7	V
Temperature coefficient	TC		50 TYP		PPM/°C
Reference noise	RN		10 TYP		µV
Power supply section					
Analog supply current	I_{DDA}	AV_{DD} = 5 V, BV_{DD} = DV_{DD} = 3.3 V		40	mA
Digital supply current	I_{DDD}			1	mA
Buffer supply current	I_{DDB}			4	mA
Supply current in power-down mode	$I_{DD\,P}$			10	mA
Power dissipation	P_D			216	mW
Power dissipation In power down	P_D		30 TYP		mW

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$	Limits		Unit
			Min	Max	
AC section					
Signal-to-noise ratio + distortion 3/	SINAD	Differential mode	63		dB
		Single-ended mode 4/	64	TYP	
Signal-to-noise ratio 3/	SNR	Differential mode	64		
		Single-ended mode 4/	68	TYP	
Total harmonic distortion 3/	THD	Differential mode		-67	
		Single-ended mode	-68	TYP	
Effective number of bits	ENOB	Differential mode	10.17		Bits
	(SNR)	Single-ended mode 4/	10.4	TYP	
Spurious free dynamic range 3/	SFDR	Differential mode	67		dB
Analog input section					
Full power bandwidth with a source impedance of 150 Ω in differential configuration		FS sinewave, -3 dB	96 TYP		MHz
Full power bandwidth with a source impedance of 150 Ω in single ended configuration		FS sinewave, -3 dB	54 TYP		
Small signal bandwidth with a source impedance of 150 Ω in differential configuration		100 mVpp sinewave, -3 dB	96 TYP		
Small signal bandwidth with a source impedance of 150 Ω in single ended configuration		100 mVpp sinewave, -3 dB	54 TYP		
Timing specification section					
Delay time	$t_{d(DATA\_AV)}$				ns
Delay time	$t_{d(o)}$				
Latency	t_{pipe}				CONV CLK
Timing section					
Clock cycle of the internal clock oscillator 5/	t_C		159	175	ns
Pulse width, $\overline{\text{CONVST}}$ 5/	t_1	1 analog input	1.5 x t_C		
		2 analog input	2.5 x t_C		
		3 analog input	3.5 x t_C		
		4 analog input	4.5 x t_C		
Aperture time	t_{dA}		1	TYP	
Time between consecutive start of single conversion 5/	t_2	1 analog input	2 x t_C		
		2 analog input	3 x t_C		
		3 analog input	4 x t_C		
		4 analog input	5 x t_C		

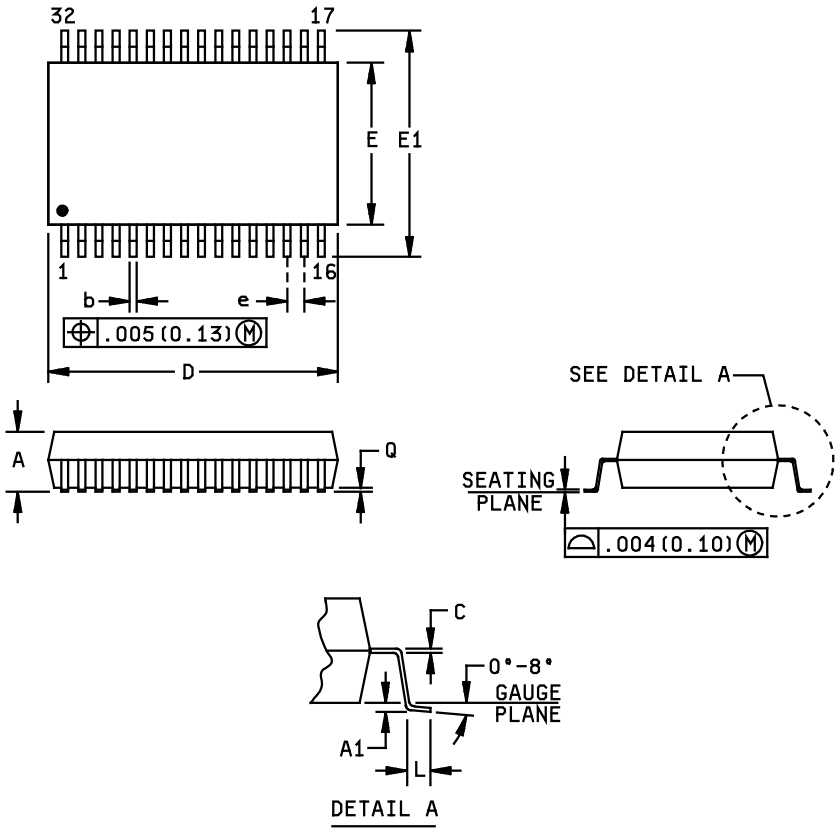
See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$	Limits		Unit
			Min	Max	
Timing section - continued					
Delay time, DATA-AV becomes active for the trigger level condition: TRIG0 = 0, TRG1 = 0 5/	$t_{d(DATA\_AV)}$	1 analog input, TL = 1		$6 \times t_C$	ns
		2 analog inputs, TL = 2		$7 \times t_C$	
		3 analog inputs, TL = 3		$8 \times t_C$	
		4 analog inputs, TL = 4		$9 \times t_C$	
Delay time, DATA-AV becomes active for the trigger level condition: TRIG0 = 1, TRG1 = 0 5/	$t_{d(DATA-AV)}$	1 analog input, TL = 4		$3 \times t_2 + 6 \times t_C$	
		2 analog inputs, TL = 4		$t_2 + 7 \times t_C$	
		3 analog inputs, TL = 6		$t_2 + 8 \times t_C$	
		4 analog inputs, TL = 8		$t_2 + 9 \times t_C$	
Delay time, DATA-AV becomes active for the trigger level condition:TRIG0 = 0, TRG1 = 1 5/	$t_{d(DATA-AV)}$	1 analog input, TL = 8		$7 \times t_2 + 6 \times t_C$	
		2 analog inputs, TL = 8		$3 \times t_2 + 7 \times t_C$	
		3 analog inputs, TL = 9		$2 \times t_2 + 8 \times t_C$	
		4 analog inputs, TL = 12		$2 \times t_2 + 9 \times t_C$	
Delay time, DATA-AV becomes active for the trigger level condition: TRIG0 = 1, TRG1 = 1 5/	$t_{d(DATA-AV)}$	1 analog input, TL = 14		$13 \times t_2 + 6 \times t_C$	
		2 analog inputs, TL = 12		$5 \times t_2 + 7 \times t_C$	
		3 analog inputs, TL = 12		$3 \times t_2 + 8 \times t_C$	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ This test is not production tested.
3/ f_S = 6 MHz, f_1 = 2 MHz at –1 dBFS, AV_{DD} = 5 V, BV_{DD} = DV_{DD} = 3.3 V, $C_L < 30$ pF.
4/ The SNR (ENOB) and SINAD is degraded typically be 2 dB in single-ended mode when the reading of data is asynchronous to the sampling clock.
5/ This timing parameter is ensured by design but is not tested.

Case outline X



Dimensions

Symbol	Millimeter		Symbol	Millimeter	
	Min	Max		Min	Max
A	---	1.20	E	6.20	---
A1	---	0.25	E1	7.80	8.40
b	0.19	0.30	L	0.26	0.46
C	0.15	---	Q	0.05	0.15
D	10.90	11.10	N	32	
e	---	0.65			

NOTE: All dimensions are in millimeters.

FIGURE 1. Case outlines.

Device Type 01
Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D0	17	DGND
2	D1	18	DV_{DD}
3	D2	19	$\overline{RD}$
4	D3	20	$\overline{WR}$ (R / $\overline{W}$)
5	D4	21	CS1
6	D5	22	$\overline{CS0}$
7	BV_{DD}	23	AV_{DD}
8	BGND	24	AGND
9	D6	25	REFM
10	D7	26	REFP
11	D8	27	REFOUT
12	D9	28	REFIN
13	D10 / RA0	29	BINM
14	D11 / RA1	30	BINP
15	CONV_CLK ($\overline{CONVST}$)	31	AINM
16	DATA_AV	32	AINP

FIGURE 2. Terminal connection.

Terminal symbol	I / O	Description
AINP	I	Analog input, single-ended or positive input of differential channel A
AINM	I	Analog input, single-ended or negative input of differential channel A
BINP	I	Analog input, single-ended or positive input of differential channel B
BINM	I	Analog input, single-ended or negative input of differential channel B
AV_{DD}	I	Analog supply voltage
AGND	I	Analog ground
BV_{DD}	I	Digital supply voltage for buffer
BGND	I	Digital ground for buffer
CONV_CLK ($\overline{\text{CONVST}}$)	I	Digital input. This input is used to apply an external conversion clock in continuous conversion mode. In single conversion mode, this input functions as the conversion start ($\overline{\text{CONVST}}$) input. A high to low transition on this input holds simultaneously the selected analog input channels and initiates a single conversion of all selected analog inputs.
$\overline{\text{CS0}}$	I	Chip select input (active low)
CS1	I	Chip select input (active high)
DATA_AV	O	Data available signal, which can be used to generate an interrupt for processors and as level information of the internal FIFO. This signal can be configured to be active low or high and can be configured as a static level or pulse output.
DGND	I	Digital ground. Ground reference for digital circuitry.
DV_{DD}	I	Digital supply voltage.
D0-D9	I / O / Z	Digital input, output; D0 = LSB
D10/RA0	I / O / Z	Digital input, output. The data line D10 is also used as an address line (RA0) for the control register. This is required for writing to the control register 0 and control register 1.
D11/RA1	I / O / Z	Digital input, output (D11 = MSB). The data line D11 is also used as an address line (RA1) for the control register. This is required for writing to control register 0 and control register 1.
REFIN	I	Common-mode reference input for the analog input channels. It is recommended that this pin be connected to the reference output REFOUT.
REFP	I	Reference input, requires a bypass capacitor of 10 μF to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0.
REFM	I	Reference input, requires a bypass capacitor of 10 μF to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0.
REFOUT	O	Analog fixed reference output voltage of 2.5 V. Sink and source capability of 250 μA. The reference output requires a capacitor of 10 μF to AGND for filtering and stability.
$\overline{\text{RD}}$ (See note)	I	The $\overline{\text{RD}}$ input is used only if the $\overline{\text{WR}}$ input is configured as a write only input. In this case, it is a digital input, active low as a data read select from the processor.
$\overline{\text{WR}}$ (R / $\overline{\text{W}}$) (See note)	I	This input is programmable. It functions as a read-write input R / $\overline{\text{W}}$ and can also be configured as write-only input $\overline{\text{WR}}$, which is active low and used as data write selection from the processor. In this case, the $\overline{\text{RD}}$ input is used as a read input from the processor.

NOTE: The start-conditions of $\overline{\text{RD}}$ and $\overline{\text{WR}}$ (R / $\overline{\text{W}}$) are unknown. The first access to the ADC has to be a write access to initialize the ADC.

FIGURE 2. Terminal connections – continued.

Reference voltage

This device has a built in reference, which provides the reference voltages for the ADC. V_{REFP} is set to 3.5 V and V_{REFM} is set to 1.5 V. An external reference can also be used through two reference input pins. REFP and REFM, if the reference source is programmed as external. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full scale and zero scale reading respectively.

Analog inputs

This device consists of 4 analog input, which are sampled simultaneously. These inputs can be selected individually and configured as single ended or differential inputs. The desired analog input channel can be programmed.

Converter

This device uses a 12-bit pipelined multi-staged architecture with 4 1-bit stages followed by 4 2-bit stages, which achieves a high sample rate with low power consumption. This device distributes the conversion over several smaller ADC sub-blocks, refining the conversion with progressively higher accuracy as the device passes the results from stage to stage. This distributed conversion requires a small fraction of the number of comparators used in a traditional flash ADC. A sample and hold amplifier (SHA) within each of the stages permits the first stage to operate on a new input sample while the second through the eighth stages operate on the seven preceding samples.

Conversion modes

The conversion can be performed in two different conversion modes. In the single conversion mode, the conversion is initiated by an external signal ($\overline{\text{CONVST}}$). An internal oscillator controls the conversion time. In the continuous conversion mode, an external clock signal is applied to the clock input (CONV_CLK). A new conversion is started with every falling edge of the applied clock signal.

Sampling rate

The maximum possible conversion rate per channel is dependent on the selected analog input channels. The table below shows the maximum conversion rate in the continuous conversion mode for different combinations.

Maximum conversion ratio in continuous conversion mode

Channel configuration	Number of channels	Maximum conversion rate per channel
1 single ended channel	1	6 MSPS
2 single ended channels	2	3 MSPS
3 single ended channels	3	2 MSPS
4 single ended channels	4	1.5 MSPS
1 differential channel	1	6 MSPS
2 differential channels	2	3 MSPS
1 single ended and 1 differential channel	2	3 MSPS
2 single ended and 1 differential channels	3	2 MSPS

The maximum conversion rate in the continuous conversion mode per channel, fC is given by:

f_C = 6 MSPS / (number of channels)

FIGURE 2. Terminal connections – continued.

Sampling rate – continued.

Maximum conversion rate in single conversion mode

Channel configuration	Number of channels	Maximum conversion rate per channel
1 single ended channel	1	3 MSPS
2 single ended channels	2	2 MSPS
3 single ended channels	3	1.5 MSPS
4 single ended channels	4	1.2 MSPS
1 differential channel	1	3 MSPS
2 differential channels	2	2 MSPS
1 single ended and 1 differential channel	2	1.5 MSPS
2 single ended and 1 differential channels	3	1.2 MSPS

Digital output data format

The digital output data format of this device can either be in binary format or in two's complement format. The following tables list the digital outputs for the analog input voltages.

Binary output format for single ended configuration

Analog input voltage	Digital output code
AIN = V_{REFP}	FFFh
AIN = (V_{REFP} + V_{REFM}) / 2	800h
AIN = V_{REFM}	000h

Two's complement output format for single ended configuration

Analog input voltage	Digital output code
AIN = V_{REFP}	7FFh
AIN = (V_{REFP} + V_{REFM}) / 2	000h
AIN = V_{REFM}	800h

Binary output format for differential configuration

Analog input voltage	Digital output code
Vin = AINP – AINM V_{REF} = V_{REFP} - V_{REFM}	
V_{in} = V_{REF}	FFFh
V_{in} = 0	800h
V_{in} = -V_{REF}	000h

FIGURE 2. Terminal connections – continued.

Digital output data format – continued.

Two's complement output format for differential configuration

Analog input voltage	Digital output code
Vin = AINP – AINM $V_{REF} = V_{REFP} - V_{REFM}$	
$V_{in} = V_{REF}$	7FFh
$V_{in} = 0$	000h
$V_{in} = -V_{REF}$	800h

ADC control register

This device contains two 10-bit wide control registers (CR0, CR1) in order to program the device into the desired mode. The bit definitions of both control registers are shown in the table below.

Bit definitions of control register CR0 and CR1

BIT	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CR0	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	MODE	V_{REF}
CR1	RBACK	OFFSET	BIN/2's	R/W	DATA_P	DATA_T	TRIG1	TRIG0	OVFL/FRST	RESET

Writing to control register 0 and control register 1

The 10-bit wide control register 0 and control register 1 can be programmed by addressing the desired control register and writing the register value to the ADC. The addressing is performed with the upper data bits D10 and D11, which function in this case as address lines RA0 and RA1. During this write process, the data bits D0 to D9 contain the desired control register value. The table below shows the addressing of each control register.

Control register addressing

D0-D9	D10/RA0	D11/RA1	Addressed control register
Desired register value	0	0	Control register 0
Desired register value	1	0	Control register 1
Desired register value	0	1	Reserved for future
Desires register value	1	1	Reserved for future

FIGURE 2. Terminal connections – continued.

ADC control registers

Control register 0

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	MODE	V_{REF}

Control register 0 bit functions

Bits	Reset value	Name	Function
0	0	V_{REF}	V_{REF} select: Bit 0 = 0 → The internal reference is selected Bit 0 = 1 →The external reference voltage to selected.
1	0	MODE	Continuous conversion mode/single conversion mode Bit 1 = 0 → Continuous conversion mode is selected. An external clock signal is applied to the CONV_CLK input in this mode. With every falling edge of the CONV_CLK signal a new converted value is written into the FIFO. Bit 1 = 1 → Single conversion mode is selected. In this mode, the CONV_CLK input function as a $\overline{\text{CONVST}}$ input. A single conversion is initiated on the device by pulsing the $\overline{\text{CONVST}}$ input. On the falling edge of $\overline{\text{CONVST}}$, the sample and hold stages of the selected analog inputs are placed into hold simultaneously and the conversion sequence for the selected channels is started. The signal DATA_AV (data available) becomes active when the trigger condition is satisfied.
2	0	PD	Power down Bit 2 = 0 → The ADC is active Bit 2 = 1 → Power down The reading and writing to and from the digital outputs is possible during power down. It is also possible to read out the FIFO.
3,4	0,0	CHSEL0, CHSEL1	Channel select. Bit 3 and bit 4 select the analog input channel of the ADC. Refer to the analog input channel configuration table.
5,6	1,0	DIFF0, DIFF1	Number of differential channels. Bit 5 and bit 6 contain information about the number of selected differential channels. Refer to the analog input channel configuration table.
7	0	SCAN	Autoscan enable. Bit 7 enables or disables the autoscan function of the ADC. Refer to the analog input channel configuration table.
8,9	0,0	TEST0, TEST1	Test input enable. Bit 8 and bit 9 control the test function of the ADC. Three different test voltages can be measured. This feedback allows the check of all hardware connections and the ADC operation. Refer to the test mode table for selection of the three different test voltages.

FIGURE 2. Terminal connections – continued.

Analog input channel selection

The analog input channels of the device can be selected via bits 3 to 7 of control register 0. One single channel (single ended or differential) is selected via bit 3 and bit 4 of control register 0. Bit 5 controls the selection between single ended and differential configuration. Bit 6 and bit 7 select the autoscan mode, if more than one input channel is selected. The table below shows the possible selections.

Analog input channel configuration

Bit 7 SCAN	Bit 6 DIFF1	Bit 5 DIFF0	Bit 4 CHSEL1	Bit 3 CHSEL0	Description of the selected inputs
0	0	0	0	0	Analog input AINP (single ended)
0	0	0	0	1	Analog input AINM (single ended)
0	0	0	1	0	Analog input BINP (single ended)
0	0	0	1	1	Analog input BINM (single ended)
0	0	1	0	0	Differential channel (AINP - AINM)
0	0	1	0	1	Differential channel (BINP - BINM)
1	0	0	0	1	Autoscan two single ended channels: AINP, AINM, AINP,…
1	0	0	1	0	Autoscan three single ended channels: AINP, AINM, BINP, AINP,…
1	0	0	1	1	Autoscan four single ended channels: AINP, AINM, BINP, BINM, AINP,...
1	0	1	0	1	Autoscan one differential channel and one single ended channel AINP, (BINP - BINM), AINP, (BINP - BINM),…
1	0	1	1	0	Autoscan one differential channel and two single ended channel AINP, AINM, (BINP - BINM), AINP,…
1	1	0	0	1	Autoscan two differential channels (AINP - AINM), (BINP - BINM), (AINP - AINM),…
0	0	1	1	0	Reserved
0	0	1	1	1	Reserved
1	0	0	0	0	Reserved
1	0	1	0	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

FIGURE 2. Terminal connections – continued.

Analog input channel selection – continued.

Test mode

The test mode of the ADC is selected via bit 8 and bit 9 of control register 0. The differential sections are shown in the table below. Three different options can be selected. This feature allows support testing of hardware connections between the ADC and the processor.

Bit 9 Test1	Bit 8 Test0	Output result
0	0	Normal mode
0	1	V_{REFP}
1	0	$((V_{REFM}) + (V_{REFP})) / 2$
1	1	V_{REFM}

Control register 1

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RBACK	OFFSET	BIN/2's	R/ $\overline{W}$	DATA_P	DATA_T	TRIG1	TRIG0	OVFL/FRST	RESET

Control register 1 bit functions

Bits	Reset value	Name	Function
0	0	RESET	Reset Writing a 1 into this bit resets the device and sets the control register 0 and control register 1 to the reset values. In addition, the FIFO pointer and offset register is reset. After reset, it takes 5 clock cycles until the first value is converted and written into the FIFO.
1	0	OVFL (read only)	Overflow flag (read only) Bit 1 of control register 1 indicates an overflow in the FIFO. Bit 1 = 0 $\rightarrow$ no overflow occurred. Bit 1 = 1 $\rightarrow$ an overflow occurred. This bit is reset to 0, after this control register is read from the processor.
		FRST (write only)	FRST: FIFO reset (write only) By writing a 1 into this bit, the FIFO is reset.
2,3	0,0	TRIG 0, TRIG 1	FIFO trigger level Bit 2 and bit 3 of control register 1 are used to set the trigger level for the FIFO. If the trigger level is reached, the signal DATA_AV (data available) becomes active according to the settings of DATA_T and DATA_P. This indicates to the processor that the ADC values can be read. Refer to the FIFO trigger level table.
4	1	DATA_T	DATA_AV type. Bit 4 of control register 1 controls whether the DATA_AV signal is a pulse or static (for edge or level sensitive interrupt inputs). If it is set to 0, the DATA_AV signal is static. If it is set to 1, the DATA_AV signal is a pulse. Refer to DATA_AV type table.

FIGURE 2. Terminal connections – continued.

Control register 1 bit functions - continued

Bits	Reset value	Name	Function
5	1	DATA_P	DATA_AV polarity. Bit 5 of control register 1 control the polarity of DATA_AV. If it is set to 1, DATA_AV is active high. If it is set to 0, DATA_AV is active low. Refer to the DATA_AV type table.
6	0	R/ $\overline{W}$	R/ $\overline{W}$, RD/ $\overline{WR}$ selection. Bit 6 of control register 1 controls the function of the inputs $\overline{RD}$ and $\overline{WR}$. When bit 6 in control register 1 is set to 1, $\overline{WR}$ becomes a R/ $\overline{W}$ input and $\overline{RD}$ is disabled. From now on, a read is signalled with R/W high and write with R/W as low signal. If bit 6 in control register 1 is set to 0, the input $\overline{RD}$ becomes a read input and the input $\overline{WR}$ becomes a write input.
7	0	BIN/2's	Complement select. If bit 7 of control register 1 is set to 0, the output value of the ADC is in twos complement. If bit 7 of control register 1 is set to 1, the output value of the ADC is in binary format. Refer to digital output data format tables..
8	0	OFFSET	Offset cancellation mode. Bit 8 = 0 $\rightarrow$ normal conversion mode Bit 8 = 1 $\rightarrow$ offset calibration mode If a 1 is written into bit 8 of control register 1, the device internally sets the inputs to zero and does a conversion. The conversion results is stored in an offset register and subtracted from all conversions in order to reduce the offset error.
9	0	RBACK	Debug mode. Bit 9 = 0 $\rightarrow$ normal conversion mode Bit 9 = 1 $\rightarrow$ enable debug mode. When bit 9 of control register 1 is set to 1, debug mode is enabled. In this mode, the contents of control register 0 and control register 1 can be read back. The first read after bit 9 is set to 1 contains the value of control register 0. The second read after bit 9 is set to 1 contains the value of control register 1.

FIGURE 2. Terminal connections – continued.

FIFO trigger level

Bit 2 and bit 3 (TRIG1, TRIG0) of control register 1 are used to set the trigger level of the FIFO. If the trigger level is reached, the DATA_AV (data available) signal becomes active according to the setting of the signal DATA_AV to indicate to the processor that the ADC values can be read.

The table below shows four different programmable trigger levels for each configuration. The FIFO trigger level, which can be selected, is dependent on the number of input channels. Both, a differential or single ended input is considered as one channel. The processor therefore always reads the data from the FIFO in the same order and is able to distinguish between the channels.

Bit 3 TRIG1	Bit 2 TRIG0	Trigger level for 1 channel (ADC values)	Trigger level for 2 channels (ADC values)	Trigger level for 3 channel (ADC values)	Trigger level for 4 channels (ADC values)
0	0	01	02	03	04
0	1	04	04	06	08
1	0	08	08	09	12
1	1	14	12	12	Reversed

DATA_AV type

Bit 4 and bit 5 (DATA_T, DATA_P) of control register 1 are used to program the signal DATA_AV. Bit 4 of control register 1 determines whether the DATA_AV signal is static or a pulse. Bit 5 of the control register determines the polarity of DATA_AV. This is shown in the table below.

Bit 5 DATA_P	Bit 4 DATA_T	DATA_AV type
0	0	Active low level
0	1	Active low pulse
1	0	Active high level
1	1	Active high pulse

FIGURE 2. Terminal connections – continued.

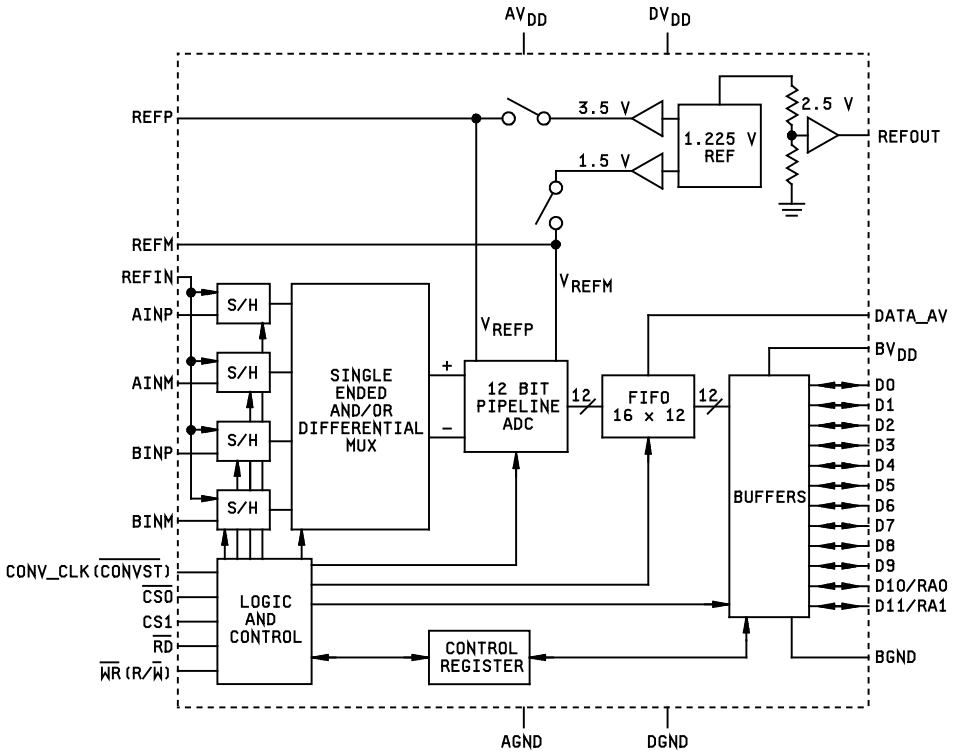
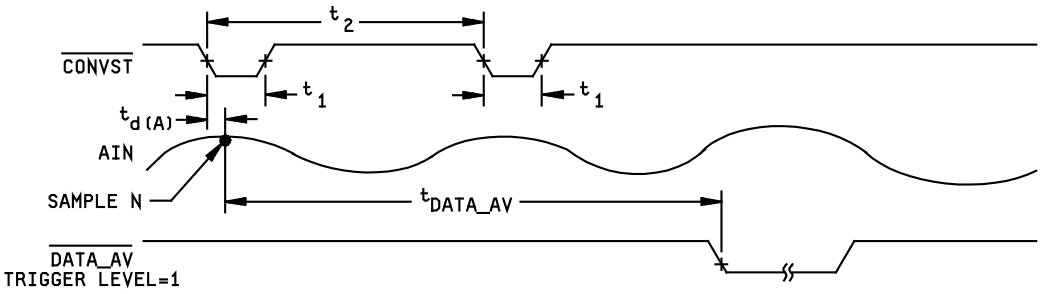


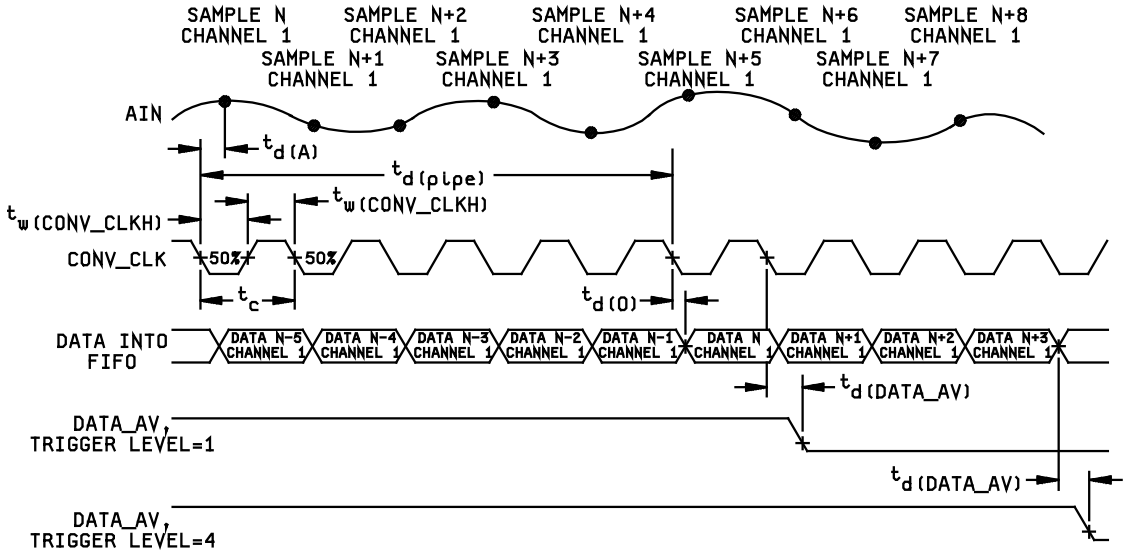
FIGURE 3. Block diagram.

SINGLE CONVERSION MODE



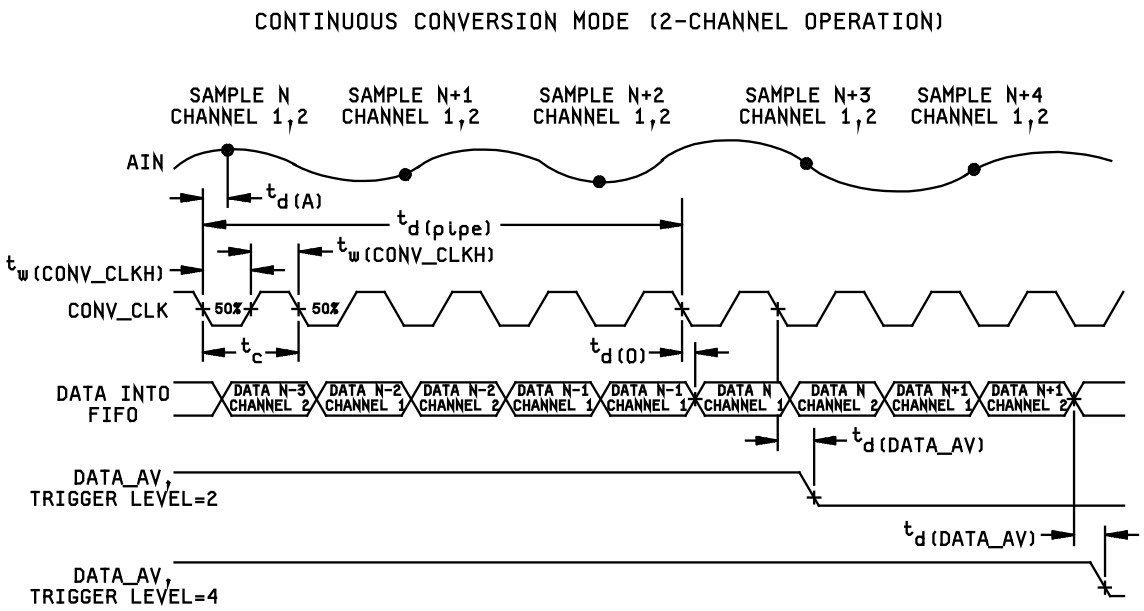
In this mode, up to four analog input channels can be selected to be sampled simultaneously.

CONTINUOUS CONVERSION MODE (1-CHANNEL OPERATION)

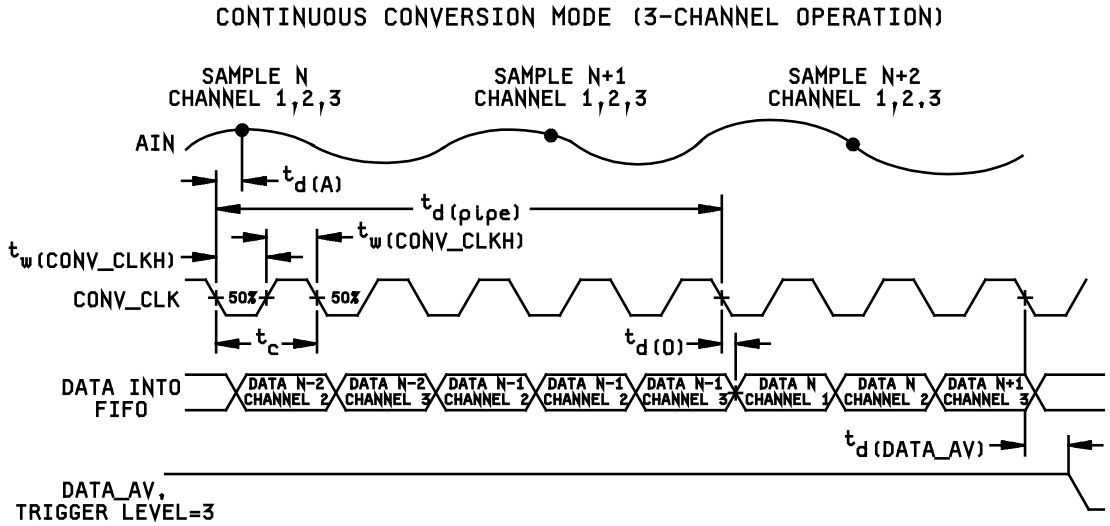


The maximum throughput rate is 6 MSPS in this mode. The timing of the DATA_AV signal is shown here in the case of a trigger level set to 1 or 4.

FIGURE 4. Timing waveforms.



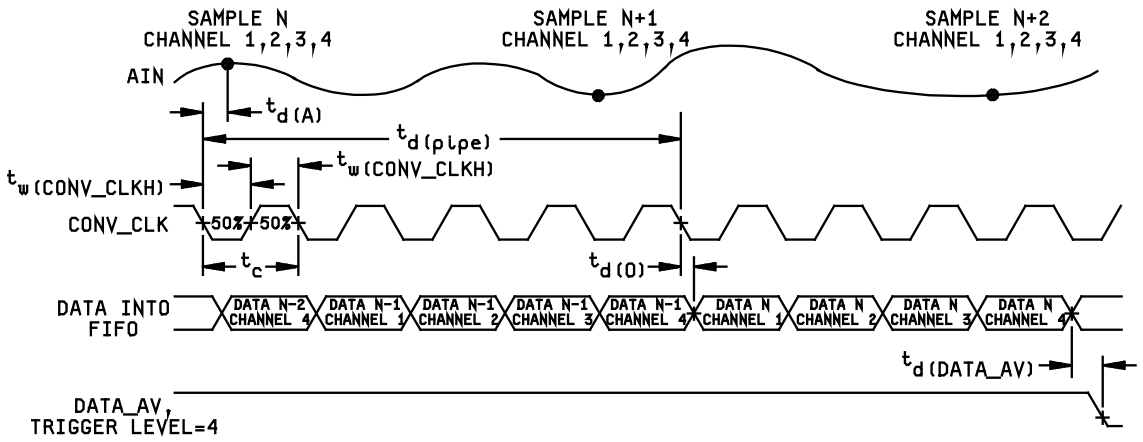
The maximum throughput rate per channel is 3 MSPS in this mode. The data flow in the bottom of the figure shows the order the converted data is written into the FIFO. The timing of the DATA_AV signal shown here is for a trigger level set to 2 or 4.



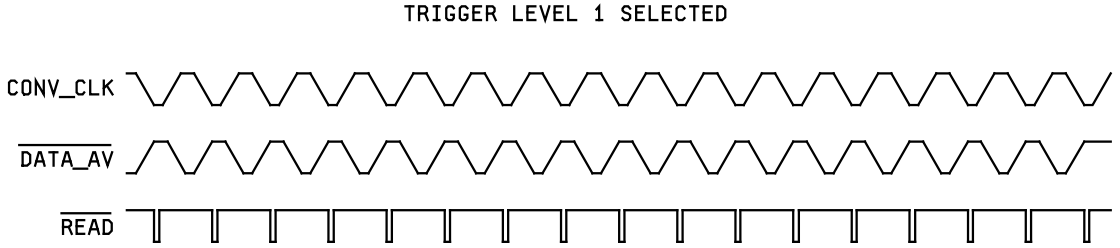
The maximum throughput rate per channel is 2 MSPS in this mode. The data flow in the bottom of the figure shows in which order the converted data is written into the FIFO. The timing of the DATA_AV signal shown here is for a trigger level set to 3.

FIGURE 4. Timing waveforms – continued.

CONTINUOUS CONVERSION MODE (4-CHANNEL OPERATION)

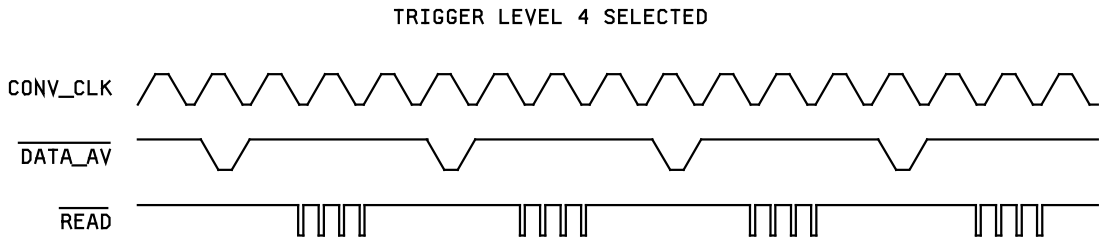


The maximum throughput rate per channel is 1.5 MSPS in this mode. The data flow in the bottom of the figure shows in which order the converted data is written into the FIFO. The timing of the DATA_AV signal here is for a trigger level of 4.

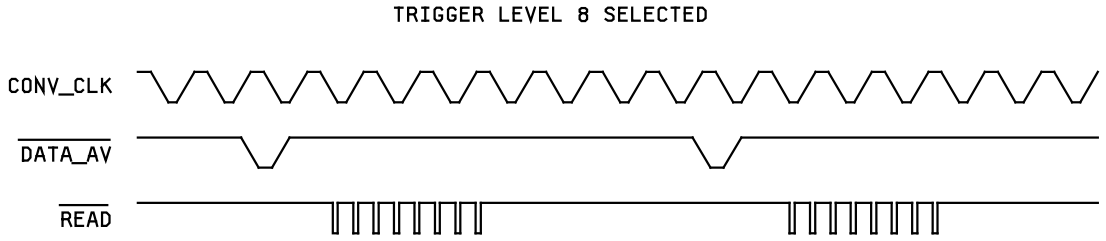


The control signal DATA_AV is set to an active low pulse. This means that the connected processor has the task to read 1 value from the ADC after every DATA_AV low pulse.

FIGURE 4. Timing waveforms – continued.

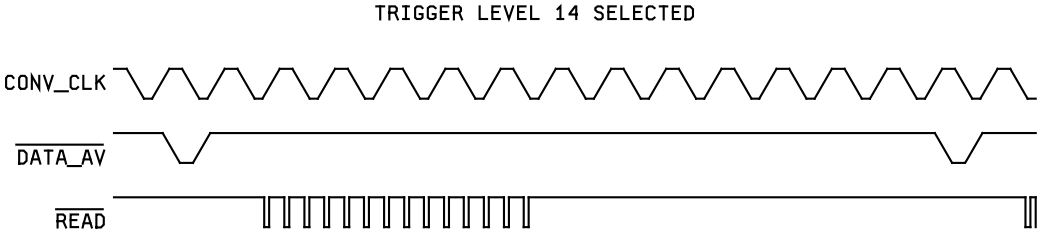


The control signal DATA_AV is set to an active low pulse. This means that the connected processor has the task to read 4 values from the ADC after every DATA_AV low pulse.



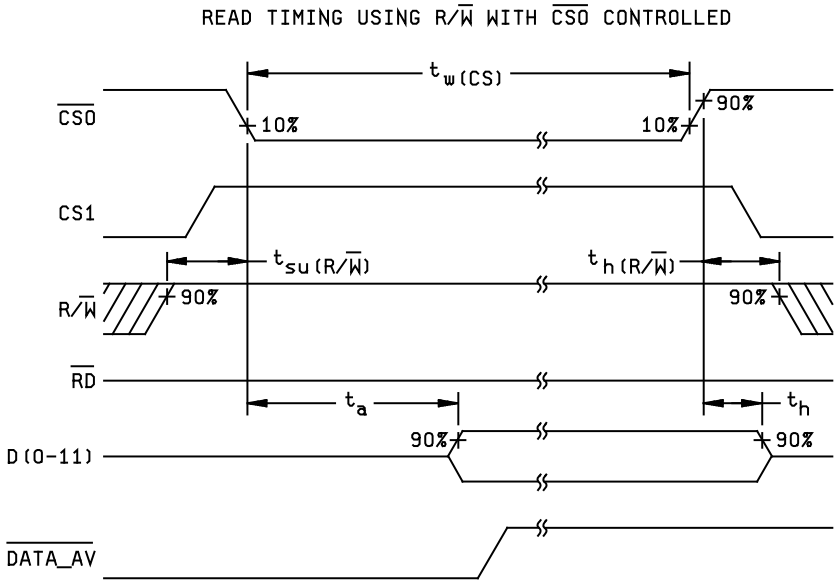
The control signal DATA_AV is set to an active low pulse. This means that the connected processor has the task to read 8 values from the ADC after every DATA_AV low pulse.

FIGURE 4. Timing waveforms. – continued.



The control signal DATA_AV is set to an active low pulse. This means that the connected processor has the task to read 14 values from the ADC after every DATA_AV low pulse.

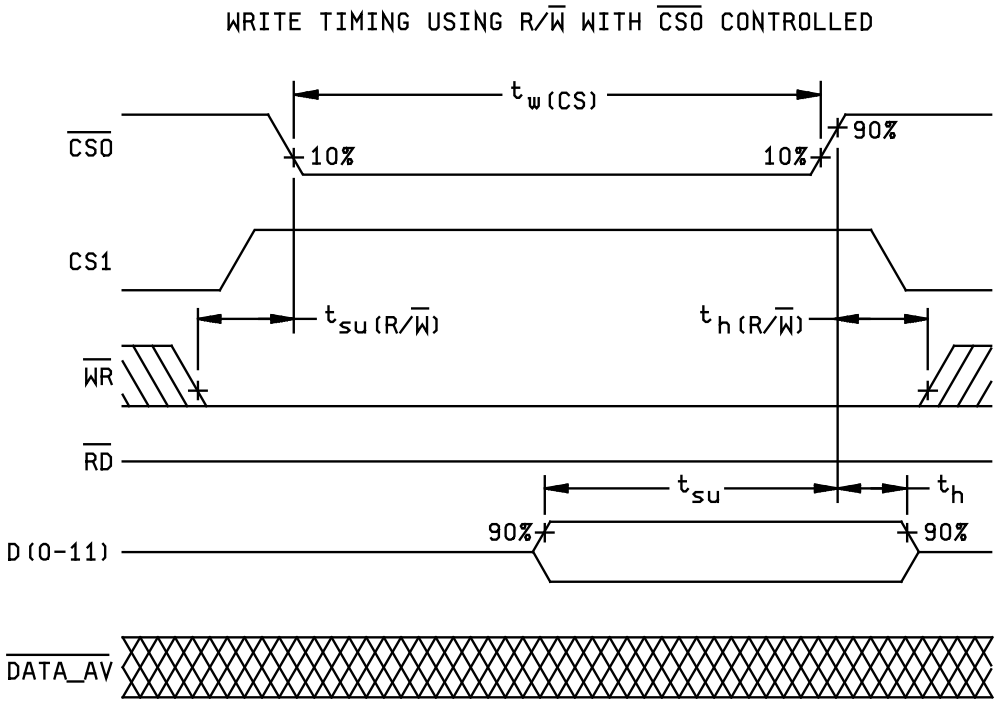
FIGURE 4. Timing waveforms. – continued.



This diagram shows the read timing behavior when the $\overline{WR}$ (R/$\overline{W}$) input is programmed as a combined read-write input R/$\overline{W}$. The $\overline{RD}$ input has to be tied to high-level in this configuration. This timing is called $\overline{CS0}$ controlled because $\overline{CS0}$ is the last external signal of $\overline{CS0}$, CS1, and R/$\overline{W}$ which becomes valid.

Design Parameters	Symbol	Min	Max	Unit
Setup time, R/$\overline{W}$ high to last CS valid	$t_{SU(R/\overline{W})}$	0		ns
Access time, last CS valid to data valid	t_a	0	10	ns
Hold time, first CS invalid to data invalid	t_h	0	5	ns
Hold time, first external CS invalid to R/$\overline{W}$ change	$t_{h(R/\overline{W})}$	5		ns
Pulse duration, CS active	$t_{W(CS)}$	10		ns

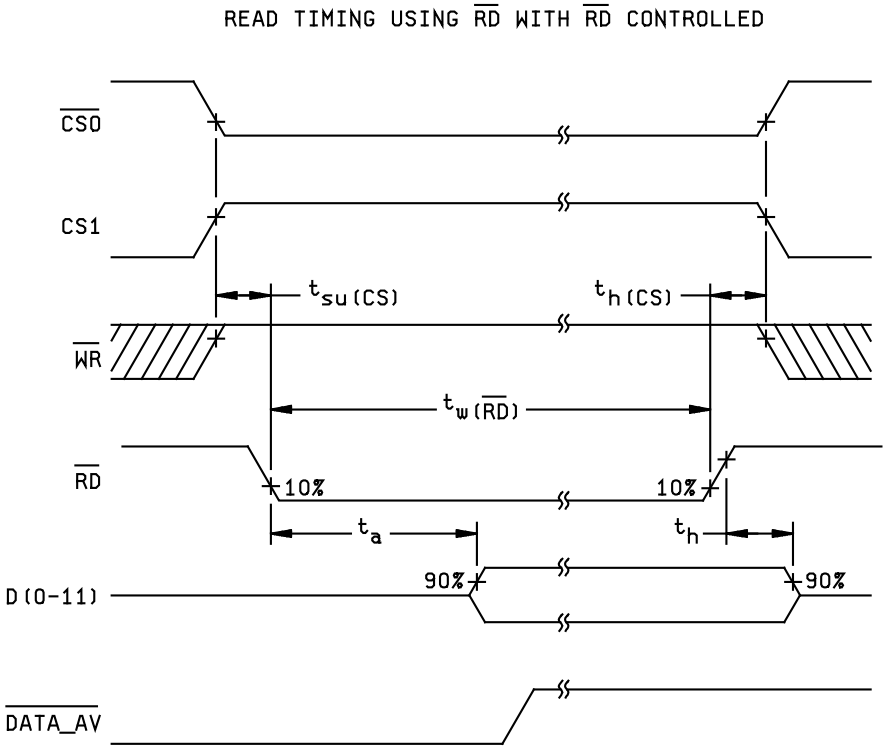
FIGURE 4. Timing waveforms. – continued.



This diagram shows the write timing behavior when the $\overline{WR}$ (R/$\overline{W}$) input is programmed as a combined read-write input R/$\overline{W}$. The $\overline{RD}$ input has to be tied to high-level in this configuration. This timing is called $\overline{CS0}$ controlled because $\overline{CS0}$ is the last external signal of $\overline{CS0}$, CS1, and R/$\overline{W}$ which becomes valid.

Design Parameters	Symbol	Min	Max	Unit
Setup time, R/$\overline{W}$ high to last CS valid	$t_{SU(R/\overline{W})}$	0		ns
Setup time, data valid to first CS invalid	t_{SU}	5		ns
Hold time, first CS invalid to data invalid	t_h	5		ns
Hold time, first CS invalid to R/$\overline{W}$ change	$t_{h(R/\overline{W})}$	5		ns
Pulse duration, CS active	$tw_{(CS)}$	10		ns

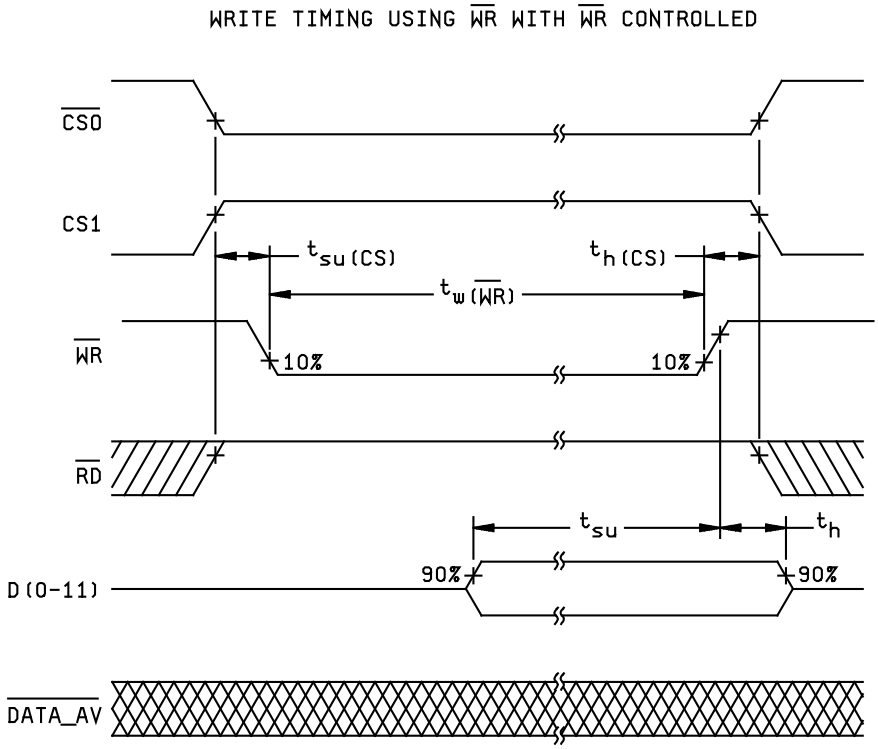
FIGURE 4. Timing waveforms. – continued.



This diagram shows the read timing behavior when the $\overline{WR}$ (R/$\overline{W}$) input is programmed as a write-input only. The $\overline{RD}$ input acts as the read-input in this configuration. This timing is called $\overline{RD}$ controlled because $\overline{RD}$ is the last external signal of $\overline{CS0}$, CS1, and $\overline{RD}$ which becomes valid.

Design Parameters	Symbol	Min	Max	Unit
Setup time, $\overline{RD}$ low to last CS valid	$t_{SU(CS)}$	0		ns
Access time, last CS valid to data valid	t_a	0	10	ns
Hold time, first CS invalid to data invalid	t_h	0	5	ns
Hold time, $\overline{RD}$ change to first CS invalid	$t_{h(CS)}$	5		ns
Pulse duration, $\overline{RD}$ active	$tw(\overline{RD})$	10		ns

FIGURE 4. Timing waveforms. – continued.



This diagram shows the write timing behavior when the $\overline{WR}$ (R/$\overline{W}$) input is programmed as a write-input $\overline{WR}$ only. The input $\overline{RD}$ acts as the read-input in this configuration. This timing is called $\overline{WR}$ controlled because $\overline{WR}$ is the last external signal of $\overline{CS0}$, CS1, and $\overline{WR}$ which becomes valid.

Design Parameters	Symbol	Min	Max	Unit
Setup time, CS stable to last $\overline{WR}$ valid	$t_{SU(CS)}$	0		ns
Setup time, data valid to first $\overline{WR}$ invalid	t_{su}	5		ns
Hold time, $\overline{WR}$ invalid to data invalid	t_h	5		ns
Hold time, $\overline{WR}$ invalid to CS change	$t_{h(CS)}$	5		ns
Pulse duration, $\overline{WR}$ active	$tw(\overline{WR})$	10		ns

FIGURE 4. Timing waveforms. – continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03609-01XE	01295	THS1206MDAREP	THS1206MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243