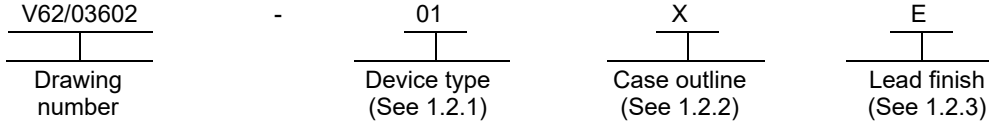


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-bit D type transparent latch with three-state outputs, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device Type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74ACT16373Q-EP	16-Bit D-type transparent latch with three-state outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline Letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	48	JEDEC MO-118	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3. Absolute maximum ratings 1/

Supply voltage range (V_{CC})	-0.5 V to 7 V
Input voltage range (V_I)	-0.5 V to $V_{CC} + 0.5$ V 2/
Output voltage range (V_O)	-0.5 V to $V_{CC} + 0.5$ V 2/
Input clamp current (I_{IK}) ($V_I < 0$ V or $V_I > V_{CC}$)	± 20 mA
Output clamp current (I_{OK}) ($V_I < 0$ V or $V_I > V_{CC}$)	± 24 mA
Continuous output current (I_O) ($V_O = 0$ V to V_{CC})	± 24 mA
Continuous current through V_{CC} or GND	± 260 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air)	1.2 W 3/
Storage temperature range, T_{stg}	-65°C to 150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output voltage ratings may be exceeded if the input and output ratings are observed.

3/ The maximum package power dissipation is calculated using a junction temperature of 150°C and a broad trace length of 750 mils.

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1.4 Recommended operating conditions 4/ 5/

Supply voltage range (V_{CC})	+4.5 V to +5.5 V	6/
Input voltage range (V_{IN})	+0.0 V to V_{CC}	
Output voltage range (V_{OUT})	+0.0 V to V_{CC}	
Minimum high-level input voltage (V_{IH})	2.0 V	
Maximum low level input voltage (V_{IL})	0.8 V	
Maximum high level output current (I_{OH})	-16 mA	
Maximum low level output current (I_{OL})	16 mA	
Input transition rise or fall rate ($\Delta t/\Delta V$)	0 to 10 ns/V	
Ambient operating temperature (T_A)	-40°C to 125°C	

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, cage code or logo
- B. Pin 1 identifier
- C. ESDS identification (Optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) diagram shall be as shown in 1.2.2 and in figure 1.

3.5.2 Block diagram. The block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

4/ Unused inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater to keep them from floating. Refer to the device manufacturer’s application report.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

6/ All V_{CC} and GND pins must be connected to the proper-voltage power supply.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{CC}	T _A at	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	I _{OH} = -50 μA	4.5 V	25°C	4.40		V
				-40°C to +125°C	4.40		
			5.5 V	25°C	5.40		
				-40°C to +125°C	5.40		
		I _{OH} = -16 mA	4.5 V	25°C	3.94		
				-40°C to +125°C	3.70		
			5.5 V	25°C	4.94		
				-40°C to +125°C	4.70		
I _{OH} = -24 mA <u>2/</u>	5.5 V	-40°C to +125°C	3.85				
Low level output voltage		I _{OL} = 50 μA	4.5 V	25°C		0.10	V
				-40°C to +125°C		0.10	
			5.5 V	25°C		0.10	
				-40°C to +125°C		0.10	
		I _{OL} = 16 mA	4.5 V	25°C		0.36	
				-40°C to +125°C		0.50	
			5.5 V	25°C		0.36	
				-40°C to +125°C		0.50	
I _{OL} = 24 mA <u>2/</u>	5.5 V	-40°C to +125°C		0.50			
Input current	I _I	V _I = V _{CC} or GND	5.5 V	25°C		± 0.10	μA
				-40°C to +125°C		± 1	
Three-state output leakage current	I _{OZ}	V _O = V _{CC} or GND	5.5 V	25°C		± 0.50	μA
				-40°C to +125°C		± 10	
Quiescent supply current	I _{CC}	V _I = V _{CC} or GND , I _O = 0	5.5 V	25°C		8	μA
				-40°C to +125°C		160	
Quiescent supply current delta <u>3/</u>	ΔI _{CC}	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V	25°C		0.9	mA
				-40°C to +125°C		1	
Input capacitance	C _I	V _I = V _{CC} or GND	5.0 V	25°C	4.5 TYP		pF
Output capacitance	C _{IO}	V _O = V _{CC} or GND	5.0 V	25°C	12 TYP		pF
Power dissipation capacitance per latch	C _{PD}	Output enabled C _L = 50 pF, f = 1 MHz	5.0 V	25°C	43 TYP		pF
		Output disabled C _L = 50 pF, f = 1 MHz			4.5 TYP		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

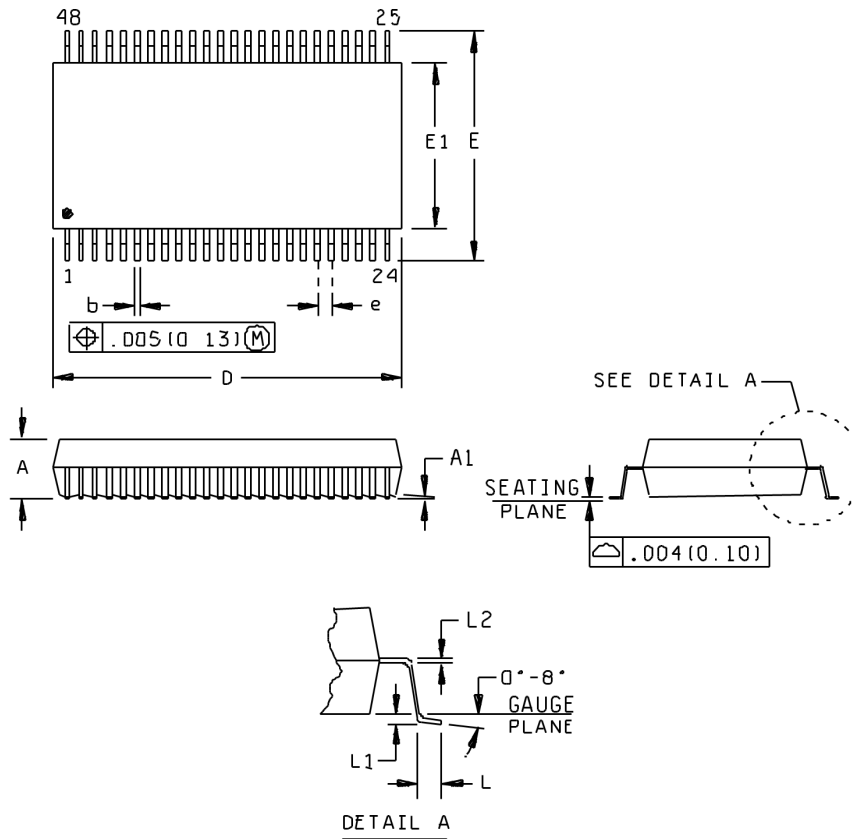
Test	Symbol	Test conditions unless otherwise specified		V _{CC}	T _A at	Limits		Unit
						Min	Max	
Pulse duration, LE high	t _w			4/	25°C	4		ns
					-40°C to +125°C	4		
Setup time, data before LE↓	t _{su}			4/	25°C	1		ns
					-40°C to +125°C	1		
Hold time, data after LE↓	t _h			4/	25°C	5		ns
					-40°C to +125°C	5		
Propagation delay time		From (Input)	To (Output)					
	t _{PLH}	D	Q	4/	25°C	3.8	9.4	ns
					-40°C to +125°C	3.8	11.8	
	t _{PHL}	D	Q	4/	25°C	3.1	9.7	ns
					-40°C to +125°C	3.1	13	
	t _{PLH}	LE	Q	4/	25°C	4.6	10.8	ns
					-40°C to +125°C	4.6	13.7	
	t _{PHL}	LE	Q	4/	25°C	4.5	10.5	ns
					-40°C to +125°C	4.5	13	
	t _{PZH}	$\overline{\text{OE}}$	Q	4/	25°C	3.1	9.5	ns
					-40°C to +125°C	3.1	13	
	t _{PZL}	$\overline{\text{OE}}$	Q	4/	25°C	3.8	11.1	ns
					-40°C to +125°C	3.8	15.1	
	t _{PHZ}	$\overline{\text{OE}}$	Q	4/	25°C	5.3	9.9	ns
-40°C to +125°C					5.3	11		
t _{PLZ}	$\overline{\text{OE}}$	Q	4/	25°C	4.3	8.7	ns	
				-40°C to +125°C	4.3	9.8		

Notes:

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
- 3/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
- 4/ V_{CC} = 4.5 V to 5.5 V

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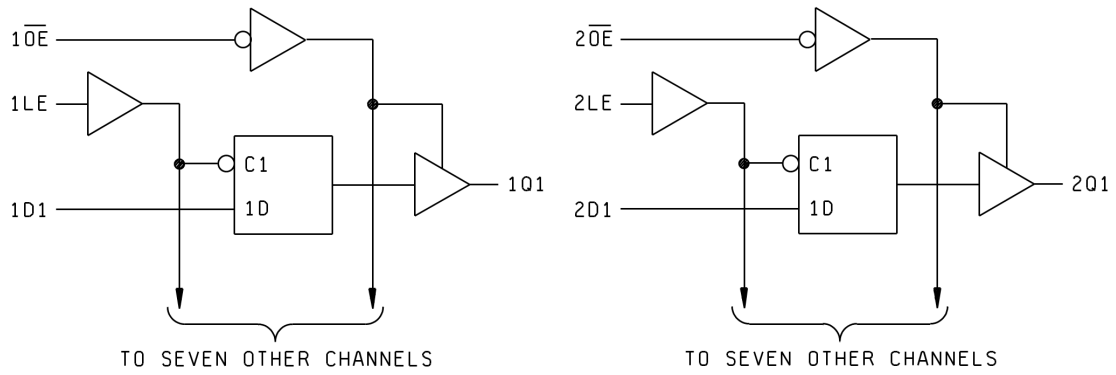
Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		0.110		2.79	E1	0.291	0.299	7.39	7.59
A1	0.008		0.20		e	0.025 Typ		0.635 Typ	
b	0.008	0.013	0.20	0.34	L	0.020	0.040	0.51	1.02
D	0.620	0.630	15.75	16.00	L1	0.010		0.25	
E	0.395	0.420	10.03	10.67	L2	0.005	0.010	0.13	0.25

FIGURE 1. Case outline.

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Function Table			
Inputs			Outputs
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low
H = High
X = Don't care

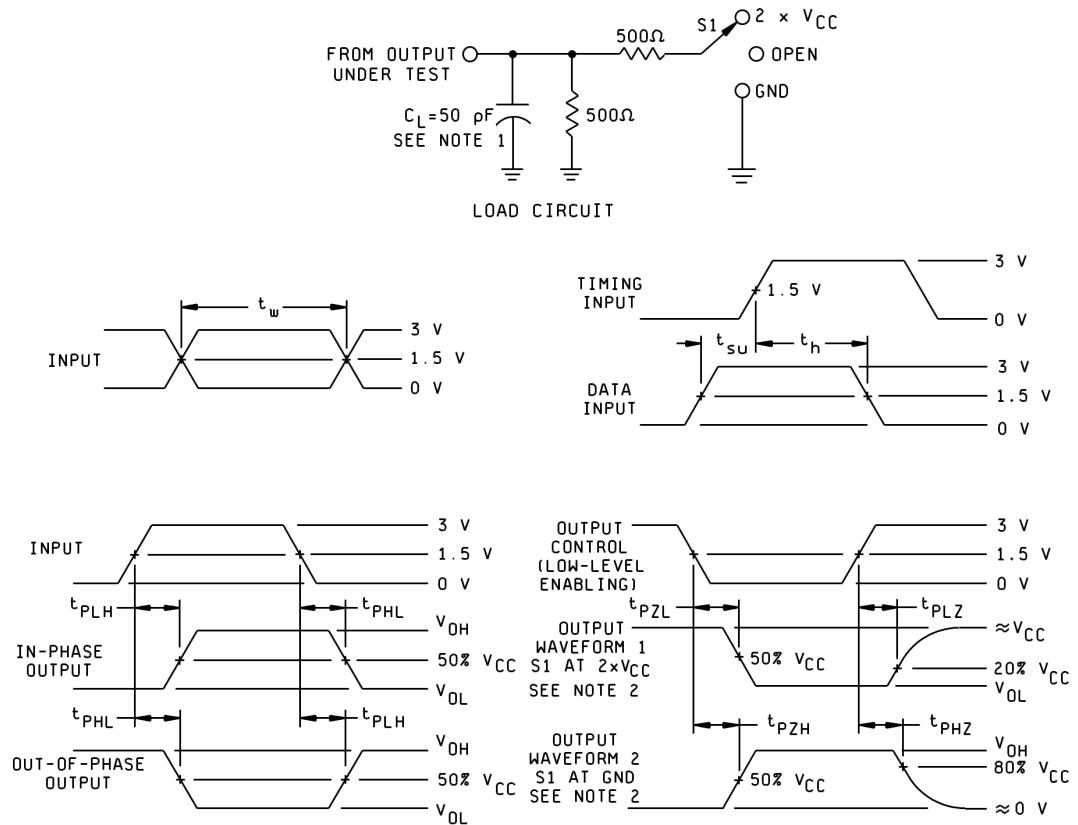
FIGURE 2. Block diagram.

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Terminal number	Terminal Symbol	Terminal number	Terminal Symbol
1	\overline{OE}	25	2LE
2	1Q1	26	2D8
3	1Q2	27	2D7
4	GND	28	GND
5	1Q3	29	2D6
6	1Q4	30	2D5
7	V _{CC}	31	V _{CC}
8	1Q5	32	2D4
9	1Q6	33	2D3
10	GND	34	GND
11	1Q7	35	2D2
12	1Q8	36	2D1
13	2Q1	37	1D8
14	2Q2	38	1D7
15	GND	39	GND
16	2Q3	40	1D6
17	2Q4	41	1D5
18	V _{CC}	42	V _{CC}
19	2Q5	43	1D4
20	2Q6	44	1D3
21	GND	45	GND
22	2Q7	46	1D2
23	2Q8	47	1D1
24	$2\overline{OE}$	48	1LE

FIGURE 3. Terminal connections.

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|| This value was obtained with continuous external writes, CLKOFF = 0 and load = 15 pF.

Test	S1
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	$2 \times V_{CC}$
t_{PHZ} / t_{PZH}	GND

Notes:

- 1/ CL includes probe and jig capacitance.
- 2/ Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control
- 3/ All impulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
- 4/ The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03602-01XE	01295	SN74ACT16373QDLREP	ACT16373QEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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