REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets																						
REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12										

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TITLE
MICROCIRCUIT, LINEAR, 40 V, RAIL TO RAIL INPUT/OUTPUT, LOW OFFSET VOLTAGE, LOW NOISE, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/21615
REV		PAGE 1 OF 12

AMSC N/A

5962-V113-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 40 V, rail to rail input/output, low offset voltage, low noise operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/21615	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	OPA4991-EP	40 V, rail to rail input/output, low offset voltage, low noise operational amplifier
02	OPA4H199-SEP	Radiation hardened, 40 V, rail to rail input/output, low offset voltage, low noise operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	See figure 1	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage, (V_S = V+ - V-) ..... 0 V to 42 V
Signal input pins:
Common mode voltage ..... (V-) - 0.5 V to (V+) + 0.5 V 2/
Differential voltage ..... V_S + 0.2 V maximum 2/
Current ..... -10 mA to + 10 mA 2/
Output short circuit ..... Continuous 3/
Junction temperature range (T_J) ..... +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Operating ambient temperature range (T_A) ..... -55°C to +125°C
Electrostatic discharge (ESD) rating:
Human body model (HDM), per AEC Q100-002 ..... ±2000 V 4/
Charge device model (CDM), per AEC Q1000-011 ..... ±1000 V

1.4 Recommended operating conditions. 5/

Supply voltage range (V_S = V+ - V-) ..... 2.7 V to 40 V
Input voltage range (V_I) ..... (V-) - 0.1 V to (V+) + 0.1 V
Specified ambient temperature range (T_A) ..... -55°C to +125°C

Thermal characteristics single channel.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	121.6	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	53.6	°C/W
Thermal resistance, junction-to-board	θ_{JB}	47.8	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	2.1	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	47.6	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	N/A	°C/W

Thermal characteristics quad channel.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	121.6	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	53.6	°C/W
Thermal resistance, junction-to-board	θ_{JB}	47.8	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	2.1	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	47.6	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	N/A	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must becurrent limited to 10 mA or less.
3/ Short-circuit to ground, one amplifier per package. This device has been designed to limit electrical damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual thermal destruction.
4/ AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.5 Radiation features.

Device type 02 only.
Maximum total dose available (dose rate = 50 - 300 rad(Si)/s) ..... 30 krads(Si) 6/

2. APPLICABLE DOCUMENTS

AUTOMOTIVE ELECTRONICS COUNCIL

AEC-Q11-002 – Human Body Model Electrostatic Discharge Test
AEC Q100-011 – Charged Device Model Electrostatic Discharge Test

(Copies of these documents are available from www.aecouncil.com.)

JEDEC Solid State Technology Association

JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

6/ For device type 02, total ionizing dose (TID) characterized in accordance with MIL-STD-883 method 1019 at dose rate condition A to TID level of 30 krads(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 30 krads(Si). For details of the TID test report, please contact the device manufacturer.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	V_{OS}	V_{CM} = V-	25°C	01, 02		±895	µV
					±125 typical		
			-55°C to +125°C			±925	
Input offset voltage drift	$\Delta V_{OS}/\Delta T$		-55°C to +125°C	01, 02	±0.3 typical		µV/°C
Input offset voltage versus power supply	PSRR	V_{CM} = V-, V_S = 4 V to 40 V	-55°C to +125°C	01, 02		±1	µV / V
					±0.3 typical		
		V_{CM} = V-, V_S = 2.7 V to 40 V 4/				±5	
					±1 typical		
Channel separation		f = 0 Hz	25°C	01, 02	5 typical		µV / V
Input bias current							
Input bias current	I_B		25°C	01, 02	±10 typical		pA
Input offset current	I_{OS}		25°C	01, 02	±10 typical		pA
Noise							
Input voltage noise	E_N	f = 0.1 Hz to 10 Hz	25°C	01, 02	1.8 typical		µVPP
					0.3 typical		µVRMS
Input voltage noise density	e_N	f = 1 kHz	25°C	01, 02	10.8 typical		$nV/\sqrt{Hz}$
		f = 10 kHz			9.4 typical		
Input current noise	i_N	f = 1 kHz	25°C	01, 02	82 typical		$fA/\sqrt{Hz}$

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input voltage range							
Common mode voltage range	V_{CM}		25°C	01, 02	(V-) – 0.1	(V+) + 0.1	V
Common mode rejection ratio	CMRR	V_S = 40 V, (V-) – 0.1 V < V_{CM} < (V+) – 2 V (main input pair)	-55°C to +125°C	01, 02	107		dB
					130 typical		
		V_S = 4 V, (V-) – 0.1 V < V_{CM} < (V+) – 2 V (main input pair)			82		
					100 typical		
		V_S = 2.7 V, 4/ (V-) – 0.1 V < V_{CM} < (V+) – 2 V (main input pair)			75		
					95 typical		
		V_S = 2.7 V to 40 V, (V+) – 1 V < V_{CM} < (V+) – 0.1 V (Aux input pair)			85 typical		
Input capacitance							
Differential	Z_{ID}	5/	25°C	01, 02	100||9 typical		MΩ||pF
Common mode	Z_{ICM}	5/	25°C	01, 02	6||1 typical		TΩ||pF
Open loop gain							
Open loop voltage gain	A_{OL}	V_S = 40 V, V_{CM} = (V-) + 0.1 V < V_O < (V+) – 0.1 V	+25°C	01, 02	120		dB
					145 typical		
			-55°C to +125°C		142 typical		
		V_S = 4 V, V_{CM} = (V-) + 0.1 V < V_O < (V+) – 0.1 V	+25°C		104		
					130 typical		
			-55°C to +125°C		125 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Open loop gain – continued.							
Open loop voltage gain – continued	A_{OL}	V_S = 2.7 V, 4/ V_{CM} = (V-) + 0.1 V < V_O < (V+) – 0.1 V	+25°C	01, 02	101		dB
					120 typical		
			-55°C to +125°C		118 typical		
Frequency response							
Gain bandwidth product	GBW		+25°C	01, 02	4.5 typical		MHz
Slew rate	SR	V_S = 40 V, G = +1, C_L = 20 pF	+25°C	01, 02	21 typical		V/µs
Settling time	t_S	To 0.01%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF	+25°C	01, 02	2.5 typical		µs
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			1.5 typical		
		To 0.1%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF			2 typical		
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			1 typical		
Phase margin		G = +1, R_L = 10 kΩ, C_L = 20 pF	+25°C	01, 02	60 typical		°
Overload recovery time		V_{IN} x gain > V_S	+25°C	01, 02	400 typical		ns
Total harmonic distortion + noise 6/	THD+N	V_S = 40 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz	+25°C	01, 02	0.00021 % typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output							
Voltage output swing from rail		V_S = 40 V, R_L = no load, 4/	+25°C	01, 02		10	mV
		Positive and negative rail headroom			5 typical		
		V_S = 40 V, R_L = 10 kΩ,				70	
		Positive and negative rail headroom			50 typical		
		V_S = 40 V, R_L = 2 kΩ,				350	
		Positive and negative rail headroom			300 typical		
		V_S = 2.7 V, R_L = no load, 4/				6	
		Positive and negative rail headroom			1 typical		
		V_S = 2.7 V, R_L = 10 kΩ,				12	
		Positive and negative rail headroom			5 typical		
		V_S = 2.7 V, R_L = 2 kΩ,				40	
		Positive and negative rail headroom			25 typical		
Short circuit current	I_{SC}		+25°C	01, 02	±75 typical		mA
Capacitive load drive	C_{LOAD}		+25°C	01, 02	1000 typical		pF
Open loop output impedance	Z_O	f = 1 MHz, I_O = 0 A	+25°C	01, 02	525 typical		Ω
Power supply							
Quiescent current per amplifier	I_Q	V_{CM} = V-, I_O = 0 A	+25°C	01, 02		685	μA
					560 typical		
			-55°C to +125°C			750	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, for V_S = (V+) – (V-) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = +25°C, R_L = 10 kΩ connected to $V_S/2$, and V_{OUT} = $V_S/2$.

3/ For device type 02, total ionizing dose (TID) characterized in accordance with MIL-STD-883 method 1019 at dose rate condition A to TID level of 30 krads(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 30 krads(Si). For details of the TID test report, please contact the device manufacturer.

4/ Specified by characterization only.

5/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

6/ Third-order filter; bandwidth = 80 kHz at –3 dB.

Case X

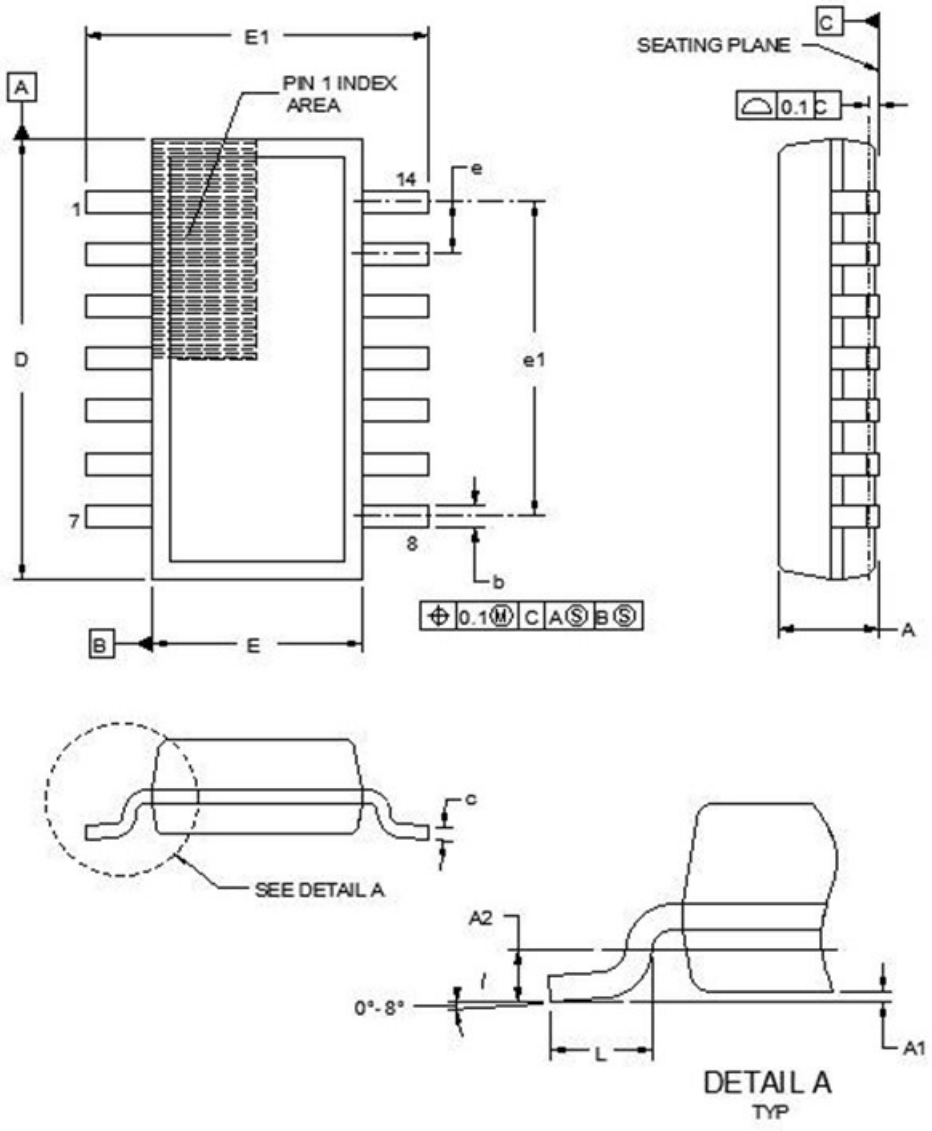

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/21615
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Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.043	---	1.10
A1	.000	.004	0.00	0.10
A2	.010	---	0.25	---
b	.004	.012	0.11	0.31
c	.003	.008	0.08	0.20
D	.161	.170	4.10	4.30
E	.074	.083	1.90	2.10
E1	.124	.132	3.16	3.36
e	.020 BSC		0.50 BSC	
e1	.118 BSC		3.00 BSC	
L	.013	.025	0.33	0.63

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimension D body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (.006 inch) per side.
3. Dimension E body width does not include interlead flash. Interlead flash shall not exceed 0.50 mm (.020 inch) per side.

FIGURE 1. Case outline - Continued.

Device types	01, 02		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	OUT 1	O	Output, channel 1.
2	IN1-	I	Inverting input, channel 1.
3	IN1+	I	Noninverting input, channel 1.
4	V+	---	Positive (highest) power supply.
5	IN2+	I	Noninverting input, channel 2.
6	IN2-	I	Inverting input, channel 2.
7	OUT2	O	Output, channel 2.
8	OUT3	O	Output, channel 3.
9	IN3-	I	Inverting input, channel 3.
10	IN3+	I	Noninverting input, channel 3.
11	V-	---	Negative (lowest) power supply.
12	IN4+	I	Noninverting input, channel 4.
13	IN4-	I	Inverting input, channel 4.
14	OUT4	O	Output, channel 4.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 02 and as specified in 1.5 herein.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/21615-01XE	01295	Reel, 3000 units	OPA4991EP	OPA4991MDYYREP
V62/21615-02XE	01295	Reel, 250 units	4H199SEP	OPA4H199MDYYTSEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243