REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13									

PMIC N/A

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TITLE
MICROCIRCUIT,LINEAR, HIGH PRECISION, LOW NOISE, RAIL-TO-RAIL OUTPUT, 11 MHz, JFET OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/21607

REV

AMSC N/A

5962-V051-22

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high precision, low noise, rail-to-rail output, 11 MHz joint field effect transistor (JFET) operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/21607	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	OPA4H014-SEP	High precision, low noise, rail-to-rail output, 11 MHz JFET operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_S = +V - -V) :
- Dual supply ..... ±10 V
- Single supply ..... 20 V

Signal input pins:
- Voltage ..... $-V_S$ – 0.5 V to $+V_S$ + 0.5 V 2/
- Current ..... ±10 mA 2/

Output short circuit ..... Continuous 3/

Temperature:
- Operating ..... -55°C to +150°C
- Junction ..... +150°C
- Storage (T_{stg}) ..... -65°C to +150°C

Electrostatic discharge (ESD) rating:
- Human body model (HBM) per JEDEC JS-001 ..... ±2000 V 4/
- Charge device model (CDM) per JEDEC JS-002 ..... ±500 V 5/

1.4 Recommended operating conditions. 6/

Supply voltage range (V_S = +V - -V) :
- Dual supply ..... ±2.25 V to ±9 V
- Single supply ..... 4.5 V to 18 V

Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	135	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	45	°C/W
Thermal resistance, junction-to-board	θ_{JB}	66	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	19	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	60	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	N/A	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Input terminal are diode clamped to the power supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.

3/ Short circuit to $V_S/2$ (ground in symmetrical dual supply setups), one amplifier per package.

4/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

5/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.6 Radiation features.

Maximum total dose available (dose rate = 50 - 300 rad(Si)/s) ..... 30 krads(Si) 7/

Single event phenomenon (SEP):
No Single event latchup (SEL) occurs at effective LET (see 4.3) ..... ≤ 43 MeV/(mg/cm^2) 8/

2. APPLICABLE DOCUMENTS

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 – Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

JEDEC Solid State Technology Association

JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JEDEC JS-002 – Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)
JESD 57 – Test Procedures for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 – Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

7/ All device types supplied to this drawing have been characterized at 30 krad(Si) of irradiation. However, these device's radiation end point limits for the noted parameters are guaranteed to TID level 30 krad(Si) as specified in MIL-STD-883, method 1019, condition A. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.6 herein).

8/ For more information on SEP test results, customers are requested to contact the manufacturer (see SEP table IB).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table IA herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	V_{OS}		+25°C	01		±120	µV
					±30 typical		
		V_S = ±9 V	-55°C to +125°C			±220	
						±4	µV/V
Input offset voltage drift	ΔV_{OS} / ΔT	V_S = ±9 V	-55°C to +125°C	01		±1	µV/°C
					±0.35 typical		
Power supply rejection ratio	PSRR		-55°C to +125°C	01		±0.5	µV/V
					±0.1 typical		
Channel separation		f = dc	+25°C	01	0.02 typical		µV/V
		f = 100 kHz			10 typical		
Input bias current							
Input bias current	I_B		+25°C	01		±10	pA
					±0.5 typical		
			-55°C to +125°C			±3	nA
Input offset current	I_{OS}		+25°C	01		±10	pA
					±0.5 typical		
			-55°C to +125°C			±1	nA
Noise							
Input voltage noise	En	f = 0.1 Hz to 10 Hz	+25°C	01	250 typical		nV_{PP}
		f = 0.1 Hz to 10 Hz			42 typical		nV_{RMS}
Input voltage noise density	e_n	f = 10 Hz	+25°C	01	8 typical		$nV/\sqrt{Hz}$
		f = 100 Hz			5.8 typical		
		f = 1 kHz			5.1 typical		
Input current noise density	i_n	f = 1 kHz	+25°C	01	0.8 typical		$fA/\sqrt{Hz}$

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input voltage range							
Common mode voltage	V_{CM}		-55°C to +125°C	01	$-V_S$ – 0.1	$+V_S$ – 3.5	V
Common mode rejection ratio	CMRR	V_S = ±9 V, V_{CM} = $-V_S$ – 0.1 V to $+V_S$ – 3.5 V	+25°C	01	126		dB
					140 typical		
			-55°C to +125°C		120		
Input impedance							
Differential	Z_{ID}		+25°C	01	10^{13}||10 typical		Ω||pF 4/
Common mode	Z_{IC}	V_{CM} = $-V_S$ – 0.1 V to $+V_S$ – 3.5 V	+25°C	01	10^{13}||7 typical		Ω||pF 4/
Open loop gain							
Open loop voltage gain	A_{OL}	V_O = $-V_S$ + 0.35 V to $+V_S$ – 0.35 V, R_L = 10 kΩ	+25°C	01	120		dB
					126 typical		
		V_O = $-V_S$ + 0.35 V to $+V_S$ – 0.35 V, R_L = 2 kΩ			114		
					126 typical		
			-55°C to +125°C		108		
Frequency response							
Gain bandwidth product	BW		+25°C	01	11 typical		MHz
Slew rate	SR		+25°C	01	20 typical		V/μs
Settling time	t_S	12 bits, 10 V step, gain = +1	+25°C	01	0.88 typical		μs
		16 bits, 10 V step, gain = +1			1.6 typical		
Overload recovery time	t_{OR}		+25°C	01	600 typical		ns
Total harmonic distortion + noise	THD+N	f = 1 kHz, G = 1, V_O = 3.5 V_{RMS}	+25°C	01	0.00005 typical		%

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output							
Voltage output swing from rail	V_O	R_L = 10 kΩ, A_{OL} ≥ 108 dB	+25°C	01	$-V_S$ + 0.2	$+V_S$ – 0.2	V
		R_L = 2 kΩ, A_{OL} ≥ 108 dB			$-V_S$ + 0.35	$+V_S$ – 0.35	
Short circuit current	I_{SC}	Source	+25°C	01	36 typical		mA
		Sink			-30 typical		
Open loop output impedance	Z_O	f = 1 MHz, I_O = 0 A	+25°C	01	16 typical		Ω
Power supply							
Quiescent current (per amplifier)	I_Q	I_O = 0 mA	+25°C	01		2	mA
					1.8 typical		
			-55°C to +125°C			2.7	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All device types supplied to this drawing have been characterized at 30 krad(Si) of irradiation. However, these device's radiation end point limits for the noted parameters are guaranteed to TID level 30 krad(Si) as specified in MIL-STD-883, method 1019, condition A. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.6 herein).

3/ Unless otherwise specified, V_S = ±2.25 V to ±9 V at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply.

4/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (T_C)	V_{IN}	Effective linear energy transfer (LET)
01	No SEL	+125°C	±9 V	≤ 43 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board.

3/ SEE test shall be performed in accordance with ASTM F1192 or JESD57. For more information on SEP test results, customers are requested to contact the manufacturer

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

4.2 Total dose irradiation testing. Total ionizing dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for all device types and as specified in 1.6 herein.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in TABLE IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ±10% for SEL.

f. For SEP test limits, see table IB herein.

Case X

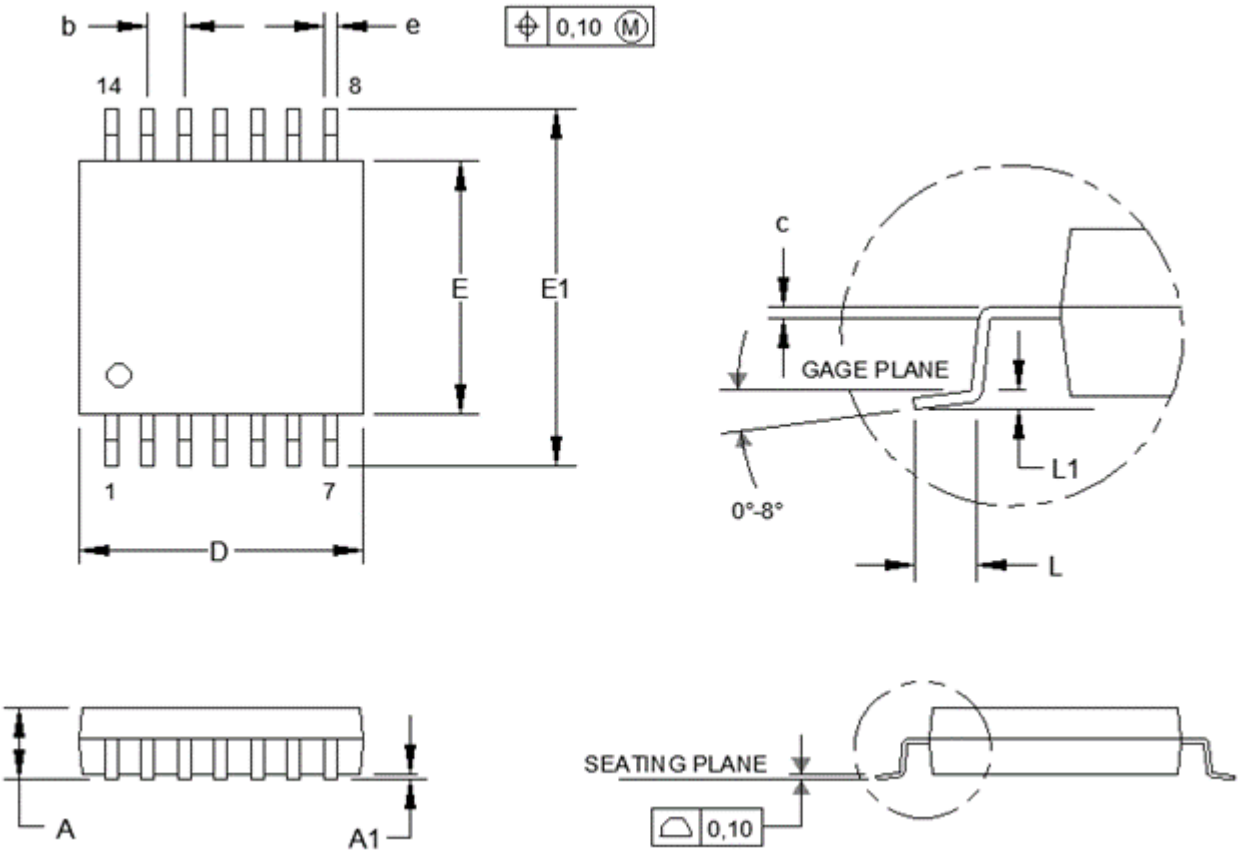

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/21607
		REV	PAGE 10

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.047	---	1.20
A1	.002	.006	0.05	0.15
b	.007	.012	0.19	0.30
c	.006 NOM		0.15 NOM	
D	.193	.201	4.90	5.10
E	.169	.177	4.30	4.50
E1	.244	.260	6.20	6.60
e	.025 BSC		0.65 BSC	
L	.020	.029	0.50	0.75
L1	.010 NOM		0.25 NOM	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (.006 inch) per side.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.25 mm (0.010 inch) each side.
4. Falls within reference to JEDEC MO-153.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	OUT A	O	Output, channel A.
2	-IN A	I	Inverting input, channel A.
3	+IN A	I	Noninverting input, channel A.
4	$+V_S$	Power	Positive (highest) power supply.
5	+IN B	I	Noninverting input, channel B
6	-IN B	I	Inverting input, channel B.
7	OUT B	O	Output channel B.
8	OUT C	O	Output, channel C.
9	-IN C	I	Inverting input, channel C.
10	+IN C	I	Noninverting input, channel C.
11	$-V_S$	Power	Negative (lowest) power supply.
12	+IN D	I	Noninverting input, channel D.
13	-IN D	I	Inverting input, channel D.
14	OUT D	O	Output, channel D.

FIGURE 2. Terminal connections.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of latchup (SEL).

6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/21607-01XE	01295	Tube, 90 units	O4H01A	OPA4H014PWSEP
		Reel, 2000 units	O4H01A	OPA4H014PWTSEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243