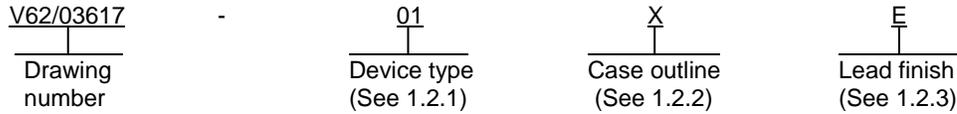


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 32-bit Floating Point Digital Signal Processor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SM320LC31-EP	32-bit Floating-Point Digital Signal Processor

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	132	JEDEC MO-069	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V to +5.0 V 2/
Input voltage range (V_I)	-0.3 V to +5.0 V
Output voltage range (V_O)	-0.3 V to +5.0 V
Continuous power dissipation (worst case) (P_D)	850 mW 3/
Operating case temperature range (T_C)	-55°C to +125°C
Storage temperature range (T_{STG})	-65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values are with respect to V_{SS} .

3/ Actual operating power is less. This value was obtained under specially produced worst-case test conditions for the TMS320C31-33 and the TMS320LC31-40, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and extension buses at the maximum rate possible. See normal (I_{CC}) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

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1.4 Recommended operating conditions. 1/ 2/

Supply voltage range (DV _{DD} , etc.) (V _{DD}).....	+3.13 V to +3.47 V	
Supply voltage (CV _{SS} , etc.) (V _{SS})	0 V NOM	
High level input voltage range (V _{IH}):		
(except RESET).....	+1.8 V to V _{DD} +0.3 V	3/
(RESET)	+2.2 V to V _{DD} +0.3 V	3/
Low level input voltage range (V _{IL}).....	-0.3 V to +0.6 V	4/
Maximum high level output current (I _{OH})	-300 μA	
Maximum low level output current (I _{OL})	+2 mA	
Operating case temperature range (T _C)	-55°C to +125°C	
High level input voltage for CLKIN (V _{TH})	+2.5 V to V _{DD} +0.3 V	3/

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Block diagram. The block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figures 4a – 4y.

-
- 1/ All voltage values are with respect to V_{SS}. All input and output voltage levels are TTL-compatible. CLKIN can be driven by a CMOS clock.
 - 2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
 - 3/ The maximum limit of this parameter is not production tested.
 - 4/ The minimum limit of this parameter is not production tested.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _c	Device type	Limits		Unit	
						Min	Max		
Electrical Characteristics 2/ 3/									
High level output voltage	V _{OH}	I _{OH} = MAX See figure 4a.	3.13 V	-55°C to +125°C	01	2.0		V	
Low level output voltage	V _{OL}	I _{OL} = MAX See figure 4a.					0.4		V
High-impedance current	I _Z		3.47 V				-20	+20	μA
Input current	I _I	V _{IN} = V _{SS} to V _{DD}	3.13 V and 3.47 V				-10	+10	μA
Input current (with internal pullup)	I _{IP}	Inputs with internal pullup. 4/	3.13 V and 3.47 V				-600	+10	μA
Supply current	I _{CC} 5/ 6/	f _x = 40 MHz	3.47 V	25°C		300	mA		
Supply current	I _{DD}	Standby, IDLE2, Clocks shut off	3.13 V and 3.47 V	-55°C to +125°C		20 TYP 7/	μA		
Input capacitance	C _i	All inputs except CLKIN	3.13 V and 3.47 V			15 8/	pF		
		CLKIN				25			
Output capacitance	C _o					20 8/	pF		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
X2/CLKIN, H1, H3 Timing Parameters								
Fall time, CLKIN	t _{r(CI)}	See ref. 1, figure 4b.	3.13 V and 3.47 V	-55°C to +125°C	01		5 <u>8/</u>	ns
Pulse duration, CLKIN low	t _{w(CIL)}	t _{c(CI)} = 25 ns See ref. 2, figure 4b.				9		ns
Pulse duration, CLKIN high	t _{w(CIH)}	t _{c(CI)} = 25 ns See ref. 3, figure 4b.				9		ns
Rise time, CLKIN	t _{r(CI)}	See ref. 4, figure 4b.					5 <u>8/</u>	ns
Cycle time, CLKIN	t _{c(CI)}	See ref. 5, figure 4b.				25	303	ns
Fall time, H1 and H3	t _{r(H)}	See ref. 6, figure 4b.					3	ns
Pulse duration, H1 and H3 low	t _{w(HL)}	See ref. 7, figure 4b.				P – 5 <u>9/</u>		ns
Pulse duration, H1 and H3 high	t _{w(HH)}	See ref. 8, figure 4b.				P – 6 <u>9/</u>		ns
Rise time, H1 and H3	t _{r(H)}	See ref. 9, figure 4b.					3	ns
Delay time, H1 low to H3 high, or H3 low to H1 high	t _{d(HL-HH)}	See ref. 10, figure 4b.				0	4	ns
Cycle time, H1 and H3	t _{c(H)}	See ref. 11, figure 4b.				50	606	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit	
						Min	Max		
Memory ($\overline{\text{STRB}} = 0$) read/write Timing Parameters 10/									
Delay time, H1 low to STRB low	t _{d(H1L-SL)}	See ref. 12, figure 4c.	3.13 V and 3.47 V	-55°C to +125°C	01	0	6	ns	
						<u>8/</u>			
Delay time, H1 low to STRB high	t _{d(H1L-SH)}	See ref. 13, figure 4c.				0	6	ns	
						<u>8/</u>			
Delay time, H1 high to R/W low (read)	t _{d(H1H-RLW)R}	See ref. 14, figure 4c.				0	9	ns	
						<u>8/</u>			
Delay time, H1 low to A valid	t _{d(H1L-A)}	See ref. 15, figure 4c.				0	10	ns	
						<u>8/</u>			
Setup time, D before H1 low (read)	t _{su(D-H1L)R}	See ref. 16, figure 4c.				14		ns	
Hold time, D after H1 low (read)	t _{h(H1L-D)R}	See ref. 17, figure 4c.				0		ns	
Setup time, $\overline{\text{RDY}}$ before H1 high	t _{su(RDY-H1H)}	See ref. 18, figure 4c.				8		ns	
Hold time, $\overline{\text{RDY}}$ after H1 high	t _{h(H1H-RDY)}	See ref. 19, figure 4c.				0		ns	
Delay time, H1 high to R/W high (write)	t _{d(H1H-RWH)W}	See ref. 20, figure 4c.					9	ns	
Valid time, D after H1 low (write)	t _{v(H1L-D)W}	See ref. 21, figure 4c.		17	ns				
Hold time, D after H1 high (write)	t _{h(H1H-D)W}	See ref. 22, figure 4c.	0		ns				
Delay time, H1 high to A valid on back-to-back write cycles (write)	t _{d(H1H-A)W}	See ref. 23, figure 4c.		15	ns				
Delay time, $\overline{\text{RDY}}$ from A valid	t _{d(A-RDY)}	See ref. 24, figure 4c.		7	ns				
				<u>8/</u>					

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Timing for XF0 and XF1 when executing LDFI or LDFIL								
Delay time, H3 high to XF0 low	t _{d(H3H-XF0L)}	See ref. 25, figure 4e.	3.13 V and 3.47 V	-55°C to +125°C	01		13	ns
Setup time, XF1 before H1 low	t _{su(XF1-H1L)}	See ref. 26, figure 4e.				10		ns
Hold time, XF1 after H1 low	t _{h(H1L-XF1)}	See ref. 27, figure 4e.				0		ns
Timing for XF0 when executing STFI or STII 11/								
Delay time, H3 high to XF0 high	t _{d(H3H-XF0H)}	See ref. 28, figure 4f.	3.13 V and 3.47 V	-55°C to +125°C	01		13	ns
Timing for XF0 and XF1 when executing SIGI								
Delay time, H3 high to XF0 low	t _{d(H3H-XF0L)}	See ref. 29, figure 4g.	3.13 V and 3.47 V	-55°C to +125°C	01		13	ns
Delay time, H3 high to XF0 high	t _{d(H3H-XF0H)}	See ref. 30, figure 4g.					13	ns
Setup time, XF1 before H1 low	t _{su(XF1-H1L)}	See ref. 31, figure 4g.				10		ns
Hold time, XF1 after H1 low	t _{h(H1L-XF1)}	See ref. 32, figure 4g.				0		ns
Timing for loading the XF register when configured as an output pin								
Valid time, H3 high to XF _x	t _{v(H3H-XF)}	See ref. 33, figure 4h.	3.13 V and 3.47 V	-55°C to +125°C	01		13	ns
Timing of XF _x changing from output to input mode								
Hold time, XF _x after H3 high	t _{h(H3H-XF)}	See ref. 34, figure 4j.	3.13 V and 3.47 V	-55°C to +125°C	01		13	ns
Setup time, XF _x before H1 low	t _{su(XF-H1L)}	See ref. 35, figure 4j.				10		ns
Hold time, XF _x after H1 low	t _{h(H1L-XF)}	See ref. 36, figure 4j.				0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Timing for XfX changing from input to output mode								
Delay time, H3 high to XfX switching from input to output	t _{d(H3H-XFIO)}	See ref. 37, figure 4k.	3.13 V and 3.47 V	-55°C to +125°C	01		17	ns
<u>RESET</u> timing								
Setup time, <u>RESET</u> before CLKIN low	t _{su(RESET-CL)}	See ref. 38, figure 4m.	3.13 V and 3.47 V	-55°C to +125°C	01	10	P 8/ 9/	ns
Delay time, CLKIN high to H1 high 12/	t _{d(CLKINH-H1H)}	See ref. 39, figure 4m.				2	14	ns
Delay time, CLKIN high to H1 low 12/	t _{d(CLKINH-H1L)}	See ref. 40, figure 4m.				2	14	ns
Setup time, <u>RESET</u> high before H1 low and after ten H1 clock cycles	t _{su(RESETH-H1L)}	See ref. 41, figure 4m.				9		ns
Delay time, CLKIN high to H3 low 12/	t _{d(CLKINH-H3L)}	See ref. 42, figure 4m.				2	14	ns
Delay time, CLKIN high to H3 high 12/	t _{d(CLKINH-H3H)}	See ref. 43, figure 4m.				2	14	ns
Disable time, H1 high to D (high impedance)	t _{dis(H1H-DZ)}	See ref. 44, figure 4m.					13 8/	ns
Disable time, H3 high to A (high impedance)	t _{dis(H3H-AZ)}	See ref. 45, figure 4m.					9 8/	ns
Delay time, H3 high to control signals high	t _{d(H3H-CONTROLH)}	See ref. 46, figure 4m.					9 8/	ns
Delay time, H1 high to R/W high	t _{d(H1H-RWH)}	See ref. 47, figure 4m.					9 8/	ns
Delay time, H1 high to IACK high	t _{d(H1H-IACKH)}	See ref. 48, figure 4m.					9 8/	ns
Disable time, <u>RESET</u> low to asynchronous reset signals disabled (high impedance)	t _{dis(RESETL-ASYNCH)}	See ref. 49, figure 4m.					21 8/	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _c	Device type	Limits		Unit
						Min	Max	
Timing for $\overline{\text{INT3}}\text{-}\overline{\text{INT0}}$								
Setup time, INT3-INT0 before H1 low	t _{su(INT-H1L)}	See ref. 50, figure 4n.	3.13 V and 3.47 V	-55°C to +125°C	01	15		ns
Pulse duration, interrupt to ensure only one interrupt	t _{w(INT)}	See ref. 51, figure 4n.				P	2P	ns
Timing for $\overline{\text{IACK}}$ 14/								
Delay time, H1 high to IACK low	t _{d(H1H-IACKL)}	See ref. 52, figure 4p.	3.13 V and 3.47 V	-55°C to +125°C	01		9	ns
Delay time, H1 high to IACK high	t _{d(H1H-IACKH)}	See ref. 53, figure 4p.					9	ns
Serial-port timing								
Delay time, H1 high to internal CLKX/R	t _{d(H1H-SCK)}	See ref. 54, figure 4q.	3.13 V and 3.47 V	-55°C to +125°C	01		13	ns
Cycle time, CLKX/R	t _{c(SCK)}	See ref. 55, figure 4q.				CLKX/R ext	t _{c(H)} x2.6	ns
			CLKX/R int	t _{c(H)} x2	t _{c(H)} x2 ³²			
Pulse duration, CLKX/R high/low	t _{w(SCK)}	See ref. 56, figure 4q.	CLKX/R ext	t _{c(H)} +10	ns			
			CLKX/R int	$\frac{[t_{c(SCK)}/2]-}{5}$	$\frac{[t_{c(SCK)}/2]+}{5}$			
Rise time, CLKX/R	t _{r(SCK)}	See ref. 57, figure 4q.		7	ns			
Fall time, CLKX/R	t _{f(SCK)}	See ref. 58, figure 4q.		7	ns			
Delay time, CLKX to DX valid	t _{d(C-DX)}	See ref. 59, figures 4q and 4r.	CLKX ext	30	ns			
			CLKX int	17				
Setup time, DR before CLKR low	t _{su(DR-CLKRL)}	See ref. 60, figures 4q and 4r.	CLKR ext	9	ns			
			CLKR int	21				
Hold time, DR from CLKR low	t _{h(CLKRL-DR)}	See ref. 61, figures 4q and 4r.	CLKR ext	9	ns			
			CLKR int	0				
Delay time, CLKX to internal FSX high/low	t _{d(C-FSX)}	See ref. 62, figures 4q and 4r.	CLKX ext	27	ns			
			CLKX int	15				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _c	Device type	Limits		Unit	
						Min	Max		
Serial-port timing - continued.									
Setup time, FSR before CLKR low	t _{su(FSR-CLKRL)}	See ref. 63, figures 4q and 4r.	CLKR ext	3.13 V and 3.47 V	-55°C to +125°C	01	9		ns
			CLKR int				9		
Hold time, FSX/R input from CLKX/R low	t _{h(SCKL-FS)}	See ref. 64, figures 4q and 4r.	CLKX/R ext				9		ns
			CLKX/R int				0		
Setup time, external FSX before CLKX	t _{su(FSX-C)}	See ref. 65, figures 4q and 4r.	CLKX ext				-[t _{c(H)} -8] 8/	[t _{c(SCK)} /2] -10 8/	ns
			CLKX int				[t _{c(H)} -21] 8/	t _{c(SCK)/2} 8/	
Delay time, CLKX to first DX bit, FSX precedes CLKX high	t _{d(CH-DX)V}	See ref. 66, figures 4q and 4r.	CLKX ext					30 8/	ns
			CLKX int					18 8/	
Delay time, FSX to first DX bit, CLKX precedes FSX	t _{d(FSX-DX)V}	See ref. 67, figure 4r.					30 8/	ns	
Delay time, CLKX high to DX high impedance following last data bit	t _{d(CH-DXZ)}	See ref. 68, figures 4q and 4r.					17 8/	ns	

Timing for HOLD/HOLDA

Setup time, $\overline{\text{HOLD}}$ before H1 low	t _{su(HOLD-H1L)}	See ref. 69, figure 4t.	3.13 V and 3.47 V	-55°C to +125°C	01	13		ns
Valid time, $\overline{\text{HOLDA}}$ after H1 low	t _{v(H1L-HOLDA)}	See ref. 70, figure 4t.				0 8/	9	ns
Pulse duration, $\overline{\text{HOLD}}$ low	t _{w(HOLD)} 15/	See ref. 71, figure 4t.				2t _{c(H)}		ns
Pulse duration, $\overline{\text{HOLDA}}$ low	t _{w(HOLDA)}	See ref. 72, figure 4t.				t _{c(H)} -5		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	

Timing for HOLD/HOLDA - continued.

Delay time, H1 low to STRB high for a HOLD	t _{d(H1L-SH)H}	See ref. 73, figure 4t.	3.13 V and 3.47 V	-55°C to +125°C	01	0	9	ns
						<u>8/</u>		
Disable time, H1 low to STRB to the high-impedance state	t _{dis(H1L-S)}	See ref. 74, figure 4t.				0	9	ns
						<u>8/</u>	<u>8/</u>	
Enable time, H1 low to STRB enabled (active)	t _{en(H1L-S)}	See ref. 75, figure 4t.				0	9	ns
						<u>8/</u>		
Disable time, H1 low to R/W to the high-impedance state	t _{dis(H1L-RW)}	See ref. 76, figure 4t.				0	9	ns
						<u>8/</u>	<u>8/</u>	
Enable time, H1 low to R/W enabled (active)	t _{en(H1L-RW)}	See ref. 77, figure 4t.	0	9	ns			
			<u>8/</u>					
Disable time, H1 low to address to the high-impedance state	t _{dis(H1L-A)}	See ref. 78, figure 4t.	0	10	ns			
			<u>8/</u>	<u>8/</u>				
Enable time, H1 low to address enabled (valid)	t _{en(H1L-A)}	See ref. 79, figure 4t.	0	13	ns			
			<u>8/</u>					
Disable time, H1 high to data to the high-impedance state	t _{dis(H1H-D)}	See ref. 80, figure 4t.	0	9	ns			
			<u>8/</u>	<u>8/</u>				

Timing requirements for peripheral pin general-purpose I/O 16/

Setup time, general-purpose input before H1 low	t _{su(GPIO-H1L)}	See ref. 81, figure 4u.	3.13 V and 3.47 V	-55°C to +125°C	01	10		ns
Hold time, general-purpose input after H1 low	t _{h(H1L-GPIO)}	See ref. 82, figure 4u.				0		ns
Delay time, general-purpose output after H1 high	t _{d(H1H-GPIO)}	See ref. 83, figure 4u.					13	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Timing requirements for peripheral pin changing from general-purpose output to input mode <u>16/</u>								
Hold time, peripheral pin after H1 high	t _{h(H1H)}	See ref. 84, figure 4v.	3.13 V and 3.47 V	-55°C to +125°C	01		13	ns
Setup time, peripheral pin before H1 low	t _{su(GPIO-H1L)}	See ref. 85, figure 4v.				9		ns
Hold time, peripheral pin after H1 low	t _{h(H1L-GPIO)}	See ref. 86, figure 4v.				0		ns
Timing for peripheral pin changing from general-purpose input to output mode <u>16/</u>								
Delay time, H1 high to peripheral pin switching from input to output	t _{d(H1H-GPIO)}	See ref. 87, figure 4w.	3.13 V and 3.47 V	-55°C to +125°C	01		13	ns
Timing for timer pin <u>17/</u>								
Setup time, TCLK external before H1 low	t _{su(TCLK-H1L)}	See ref. 88, figure 4x.	3.13 V and 3.47 V	-55°C to +125°C	01	10		ns
Hold time, TCLK external after H1 low	t _{h(H1L-TCLK)}	See ref. 89, figure 4x.				0		ns
Delay time, H1 high to TCLK internal valid	t _{d(H1H-TCLK)}	See ref. 90, figure 4x.					9	ns
Cycle time, TCLK	t _{c(TCLK)}	See ref. 91, figure 4x.	TCLK ext			t _{c(H)} x2.6		ns
			TCLK int			t _{c(H)} x2	t _{c(H)} x2 ³² 8/	
Pulse duration, TCLK high/low	t _{w(TCLK)}	See ref. 92, figure 4x.	TCLK ext			t _{c(H)} +10		ns
			TCLK int			[t _{c(TCLK)/2]-5}	[t _{c(TCLK)/2]+5}	
Timing parameters for $\overline{\text{SHZ}}$								
Disable time, $\overline{\text{SHZ}}$ low to all O, I/O pins disabled (high impedance)	t _{dis(SHZ)}	See ref. 93, figure 4y.	3.13 V and 3.47 V	-55°C to +125°C	01	0 8/	2P 8/ 9/	ns

See footnotes on next sheet.

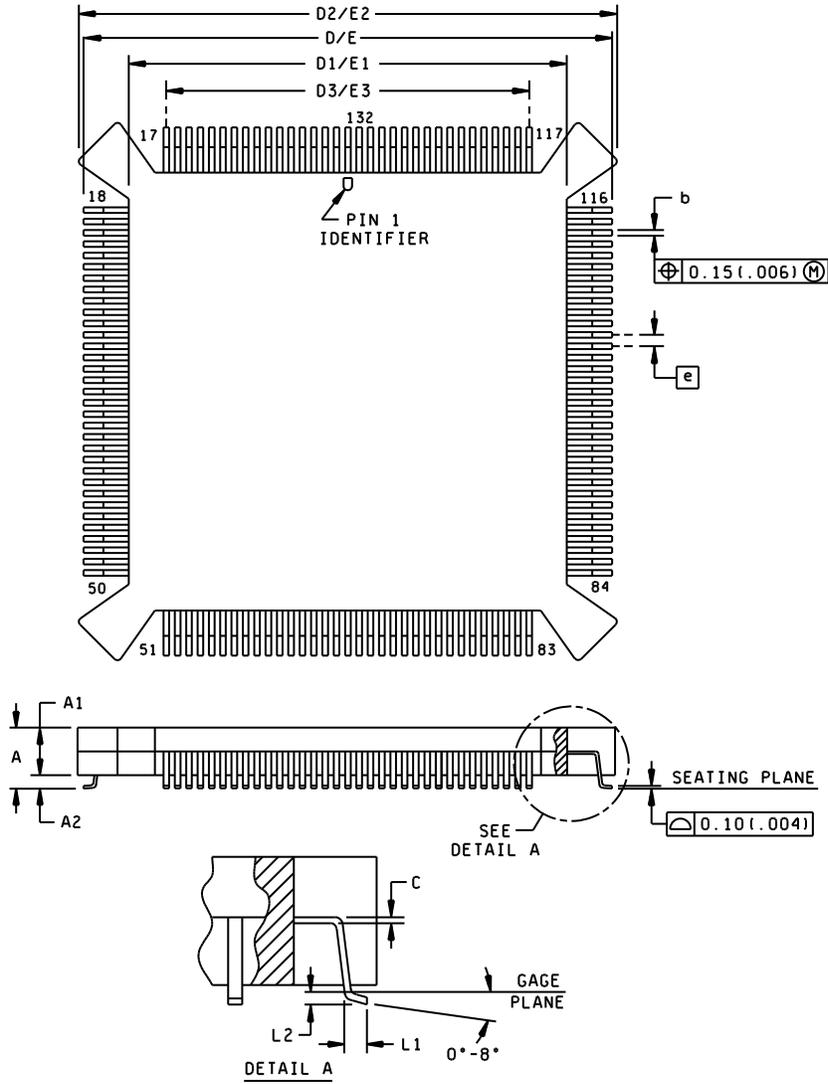
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 12

TABLE I. Electrical performance characteristics - Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ All voltage values are with respect to V_{SS} . All input and output voltage levels are TTL compatible. CLKIN can be driven by a CMOS clock.
- 3/ All input and output voltage levels are TTL compatible.
- 4/ Pins with internal pullup devices: $\overline{INT3} - \overline{INT0}$, MCBL/ \overline{MP} .
- 5/ Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).
- 6/ f_x is the input clock frequency.
- 7/ For LC31, all typical values are at $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.
- 8/ This parameter is not production tested.
- 9/ $P = t_{c(CI)}$
- 10/ See figure 4d for address bus timing variation with load capacitance greater than typical load-circuit capacitance ($C_T = 80\text{ pF}$).
- 11/ XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.
- 12/ See figure 4b for typical temperature dependence.
- 13/ $P = t_{c(H)}$
- 14/ \overline{IACK} goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction. Because of pipeline conflicts, \overline{IACK} remains low for one cycle even if the decode phase of the IACK instruction is extended.
- 15/ \overline{HOLD} is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown in figure 4t occurs; otherwise, an additional delay of one clock cycle is possible.
- 16/ Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.
- 17/ Reference numbers 88 and 89 are applicable for a synchronous input clock. Timing parameters reference numbers 91 and 92 are applicable for an asynchronous input clock.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 13

Case X



NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-069.
3. All linear dimensions are in millimeters (inches).

FIGURE 1. Case outlines.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 14</p>

Case X

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A		4.57		0.180
A1	3.30	3.81	0.130	0.150
A2	0.51		0.020	
b	0.20	0.30	0.008	0.012
C	0.16 NOM		0.006 NOM	
D	27.18	27.69	1.070	1.090
D1	23.72	24.54	0.934	0.966
D2	27.64	28.25	1.088	1.112
D3	20.32 NOM		0.800 NOM	
E	27.18	27.69	1.070	1.090
E1	23.72	24.54	0.934	0.966
E2	27.64	28.25	1.088	1.112
E3	20.32 NOM		0.800 NOM	
e	0.635 TYP		0.025 TYP	
L1	0.91	1.17	0.036	0.046
L2	0.25 TYP		0.010 TYP	

FIGURE 1. Case outlines - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 15

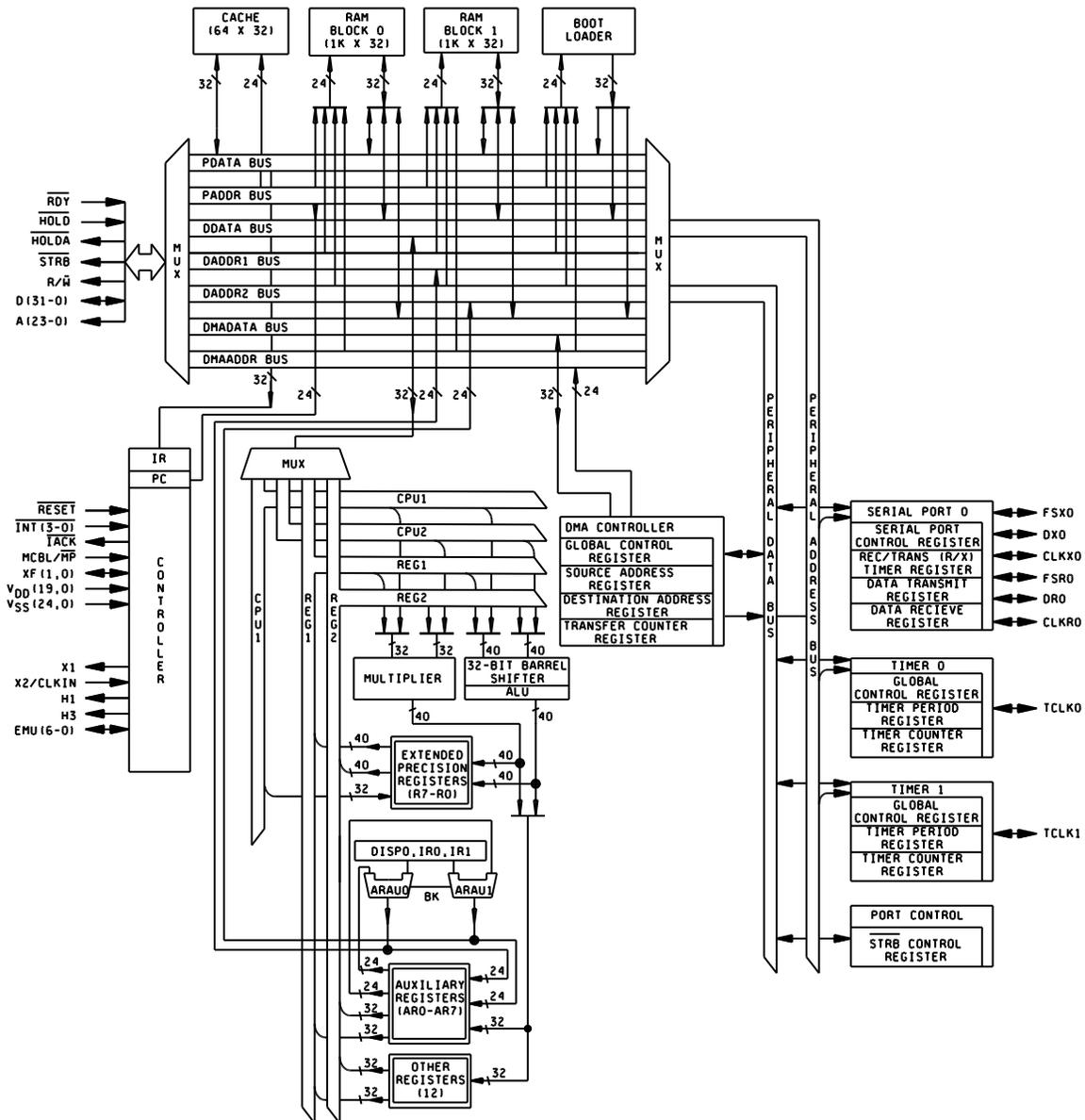


FIGURE 2. Block diagram.

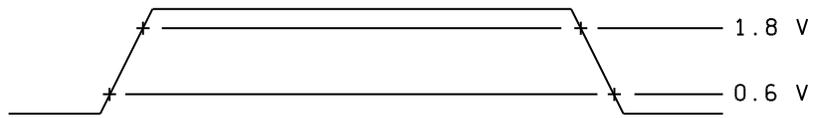
<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 16</p>

Device type		01					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A21	34	D30	67	D9	100	$\overline{\text{INT0}}$
2	A20	35	V _{SSL}	68	D8	101	V _{SSL}
3	DV _{SS}	36	DV _{SS}	69	V _{SSL}	102	CV _{SS}
4	CV _{SS}	37	IV _{SS}	70	V _{SSL}	103	$\overline{\text{INT1}}$
5	A19	38	D29	71	DV _{SS}	104	V _{DDL}
6	AV _{DD}	39	D28	72	D7	105	PV _{DD}
7	A18	40	DV _{DD}	73	D6	106	$\overline{\text{INT2}}$
8	A17	41	D27	74	DV _{DD}	107	$\overline{\text{INT3}}$
9	A16	42	DV _{SS}	75	D5	108	DR0
10	A15	43	D26	76	D4	109	IV _{SS}
11	A14	44	D25	77	D3	110	FSR0
12	A13	45	D24	78	D2	111	CLKR0
13	A12	46	D23	79	D1	112	CLKX0
14	A11	47	D22	80	D0	113	V _{SUBS}
15	AV _{DD}	48	D21	81	$\overline{\text{HOLD}}$	114	FSX0
16	A10	49	DV _{DD}	82	$\overline{\text{HOLDA}}$	115	PV _{DD}
17	DV _{SS}	50	D20	83	CV _{DD}	116	DX0
18	A9	51	CV _{SS}	84	CV _{SS}	117	DV _{SS}
19	CV _{SS}	52	D19	85	IV _{SS}	118	SHZ
20	A8	53	D18	86	DV _{SS}	119	CV _{SS}
21	A7	54	D17	87	XF0	120	TCLK0
22	A6	55	D16	88	X2/CLKIN	121	V _{DDL}
23	A5	56	D15	89	H3	122	TCLK1
24	V _{DDL}	57	IV _{SS}	90	H1	123	EMU3
25	A4	58	D14	91	CV _{DD}	124	EMU0
26	A3	59	V _{DDL}	92	$\overline{\text{R}\overline{\text{W}}}$	125	EMU1
27	A2	60	D13	93	$\overline{\text{STRB}}$	126	EMU2
28	A1	61	DV _{SS}	94	$\overline{\text{RESET}}$	127	MCBL/ $\overline{\text{MP}}$
29	A0	62	D12	95	$\overline{\text{RDY}}$	128	X1
30	V _{SSL}	63	D11	96	XF1	129	A23
31	D31	64	D10	97	V _{DDL}	130	A22
32	V _{DDL}	65	V _{DDL}	98	NC	131	V _{DDL}
33	DV _{DD}	66	DV _{DD}	99	$\overline{\text{IACK}}$	132	V _{SSL}

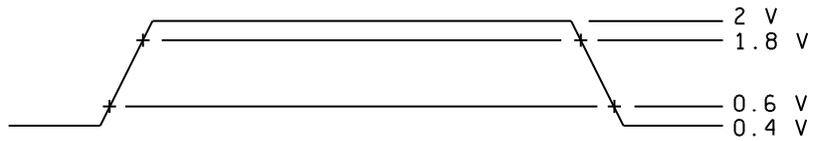
NC = No internal connection.

FIGURE 3. Terminal connections.

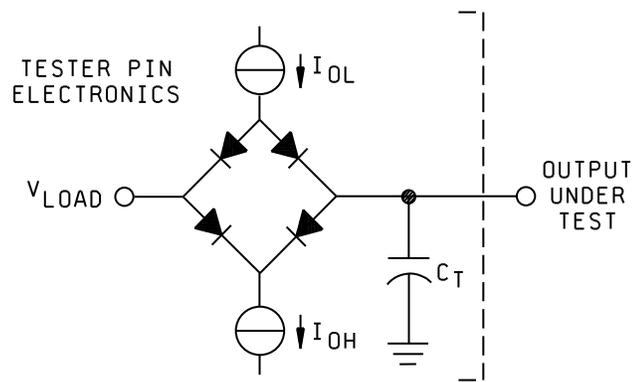
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 17



LC31 INPUT LEVELS



LC31 OUTPUT LEVELS

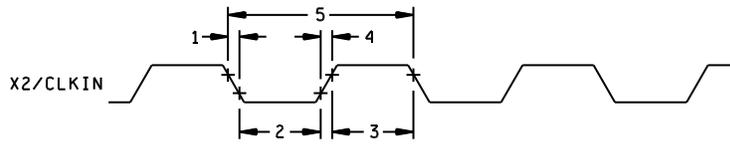


TEST LOAD CIRCUIT

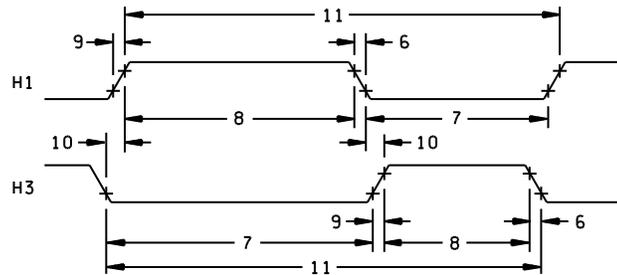
Where: I_{OL} = 2.0 mA (all outputs)
 I_{OH} = 300 μ A (all outputs)
 V_{LOAD} = 2.15 V
 C_T = 80 pF typical load circuit capacitance

FIGURE 4a. Timing waveforms and test circuit.

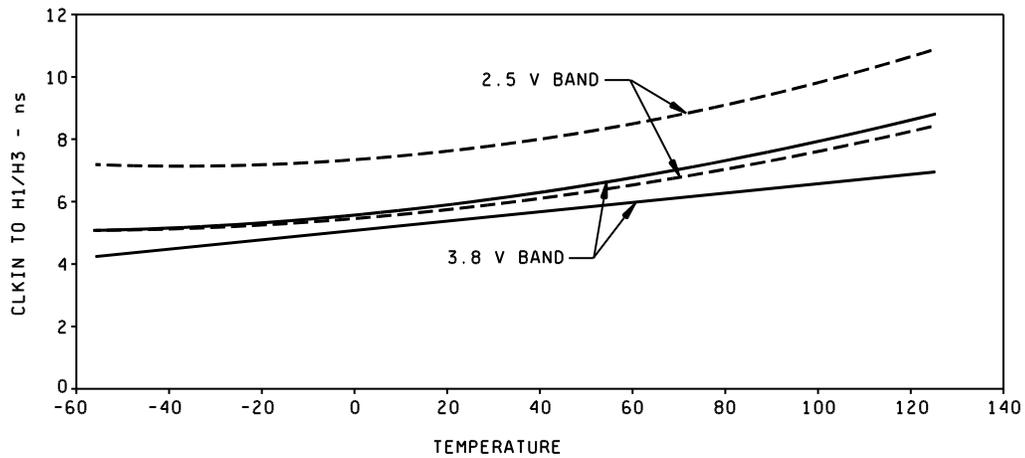
<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 18</p>



TIMING X2/CLKIN



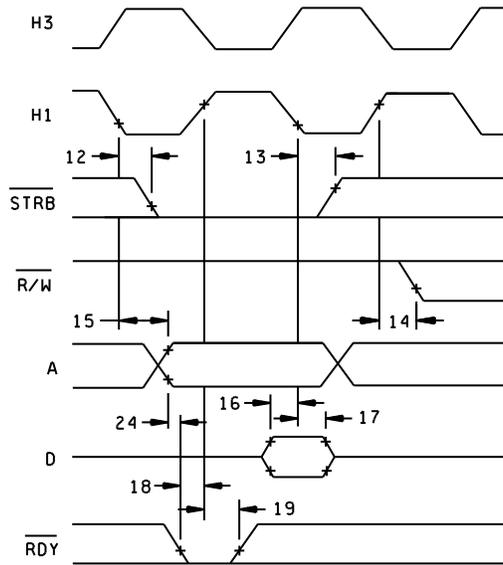
TIMING FOR H1 AND H3



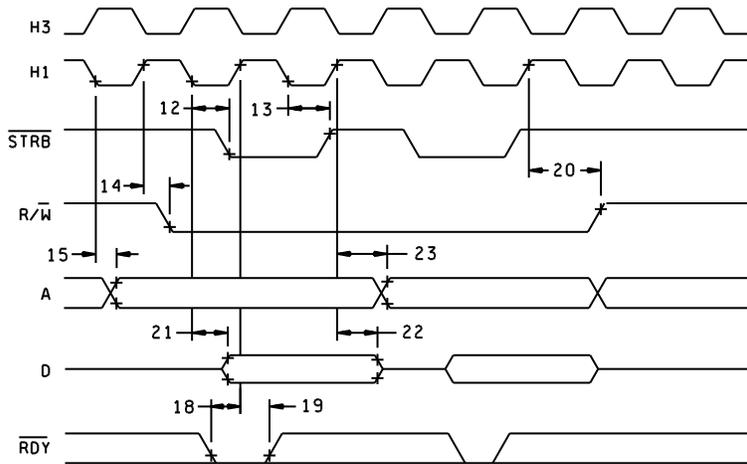
SM320LC31-EP CLKIN TO H1/H3 AS A FUNCTION OF TEMPERATURE (TYPICAL)

FIGURE 4b. Timing waveforms and test circuit.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 19</p>



TIMING FOR MEMORY ($\overline{\text{STRB}}=0$) READ

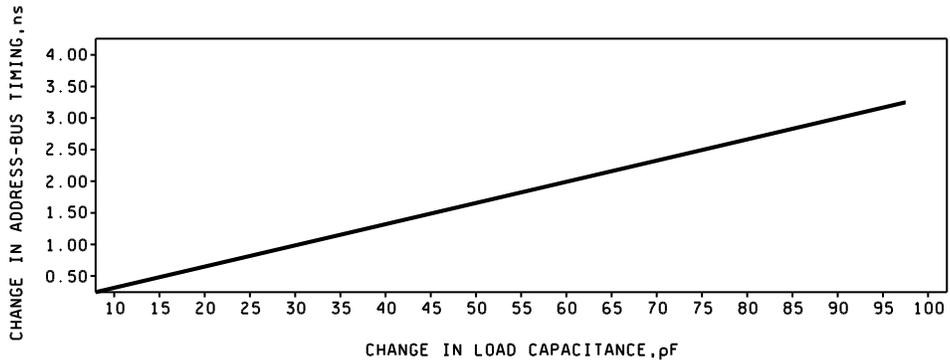


TIMING FOR MEMORY ($\overline{\text{STRB}}=0$) WRITE

NOTE: $\overline{\text{STRB}}$ remains low during back-to-back read operations.

FIGURE 4c. Timing waveforms and test circuit.

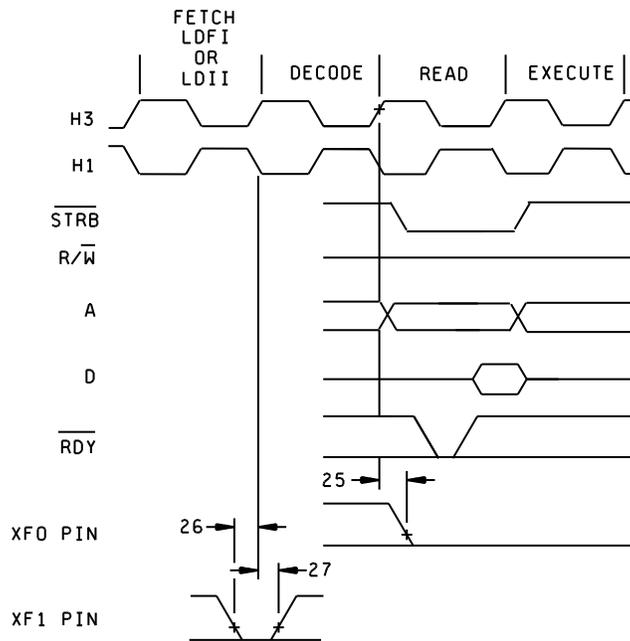
<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 20</p>



ADDRESS-BUS TIMING VARIATION WITH LOAD CAPACITANCE

NOTE: 30 pF/ns slope.

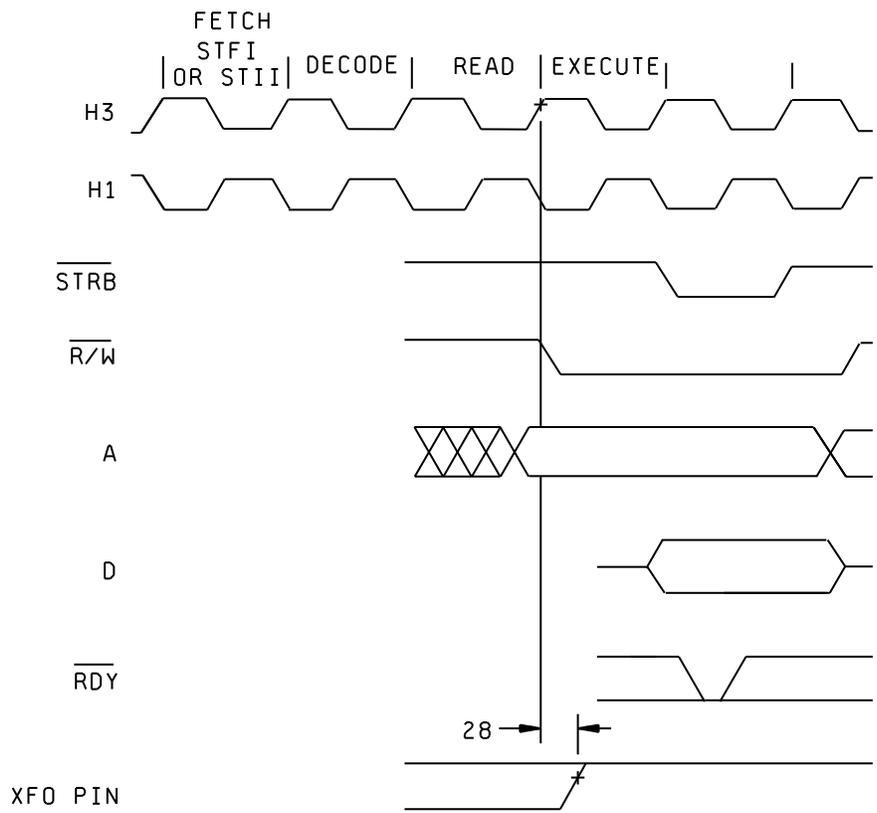
FIGURE 4d. Timing waveforms and test circuit.



TIMING FOR XFO AND XF1 WHEN EXECUTING LDFI OR LDII

FIGURE 4e. Timing waveforms and test circuit.

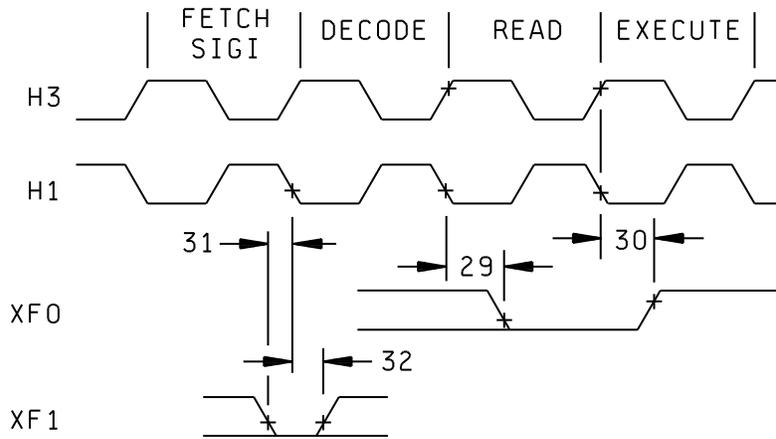
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE	CODE IDENT NO.	DWG NO.
	A	16236	V62/03617
		REV C	PAGE 21



TIMING FOR XFO WHEN EXECUTING STFI OR STII

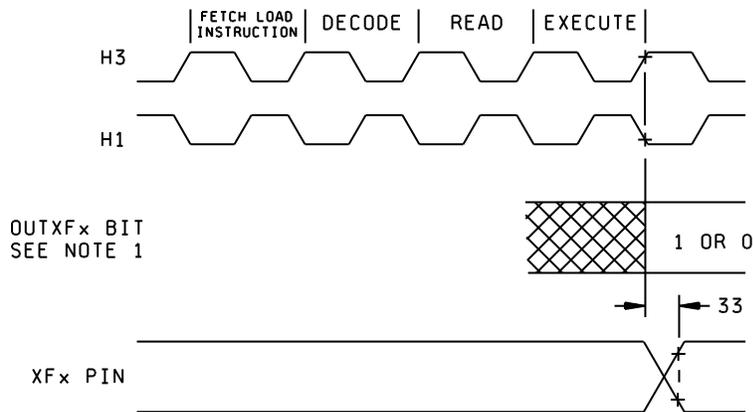
FIGURE 4f. Timing waveforms and test circuit.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 22



TIMING FOR XFO AND XF1 WHEN EXECUTING SIGI

FIGURE 4g. Timing waveforms and test circuit.

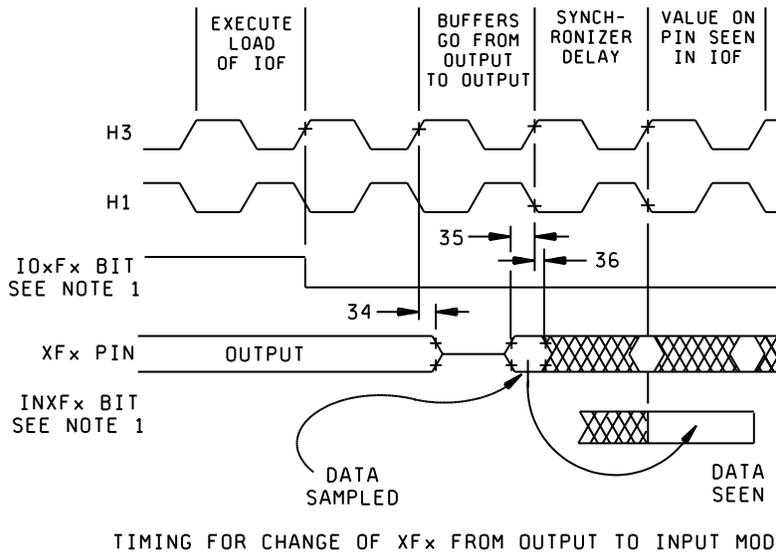


TIMING FOR LOADING XF REGISTER WHEN CONFIGURED AS AN OUTPUT PIN

NOTE 1: OUTXF_x represents either bit 2 or 6 of the IOF register.

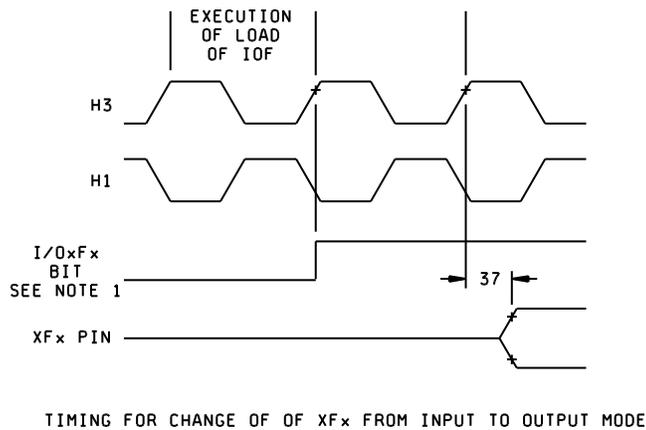
FIGURE 4h. Timing waveforms and test circuit.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 23



NOTE 1: $\bar{I/OxFx}$ represents either bit 1 or bit 5 of the IOF register, and $INxFx$ represents either bit 3 or bit 7 of the IOF register.

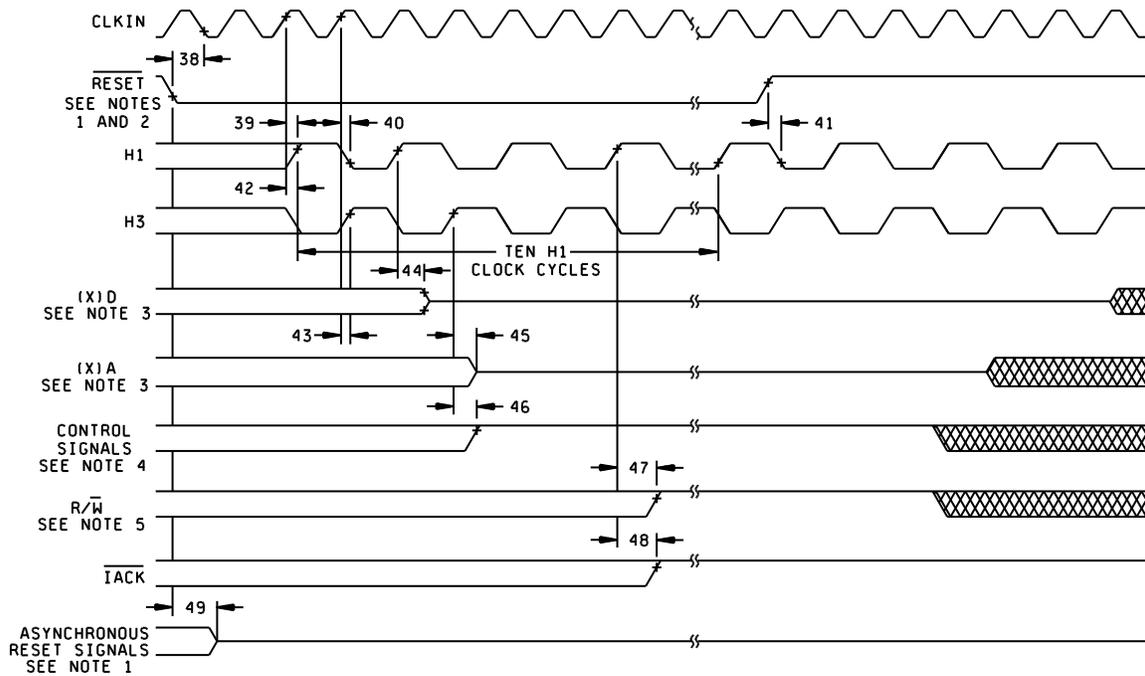
FIGURE 4j. Timing waveforms and test circuit.



NOTE 1: $\bar{I/OxFx}$ represents either bit 1 or bit 5 of the IOF register.

FIGURE 4k. Timing waveforms and test circuit.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 24



TIMING FOR RESET

- NOTES: 1. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
 2. RESET is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, and additional delay of one clock cycle is possible.
 3. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
 4. Control signals include STRB.
 5. The R/W outputs are placed in a high-impedance state during reset and can be provided with a resistive pullup, nominally 18-22 kΩ if undesirable spurious writes are caused when these outputs go low.

FIGURE 4m. Timing waveforms and test circuit.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 25</p>

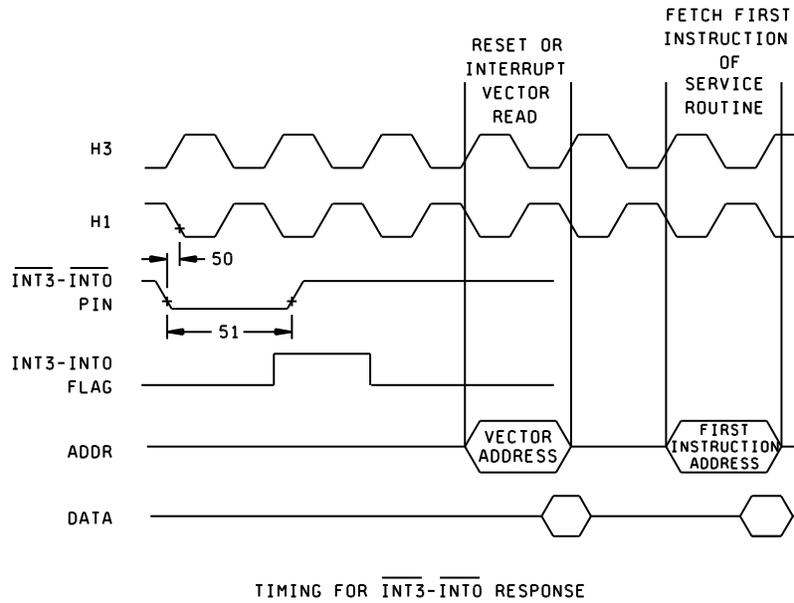


FIGURE 4n. Timing waveforms and test circuit.

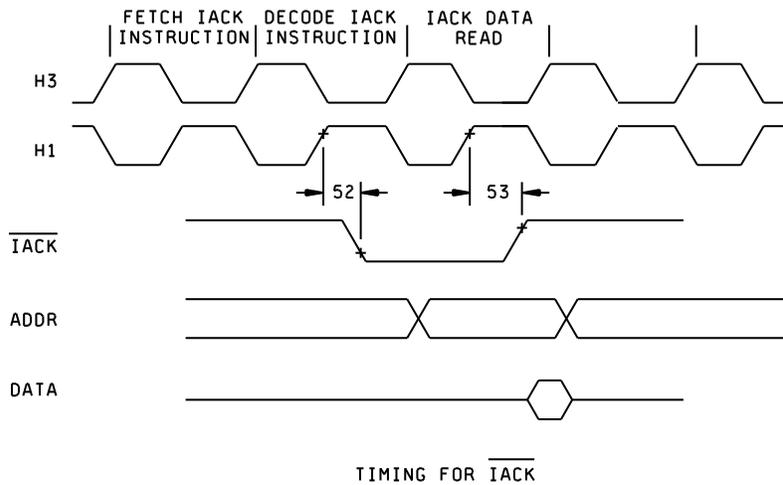
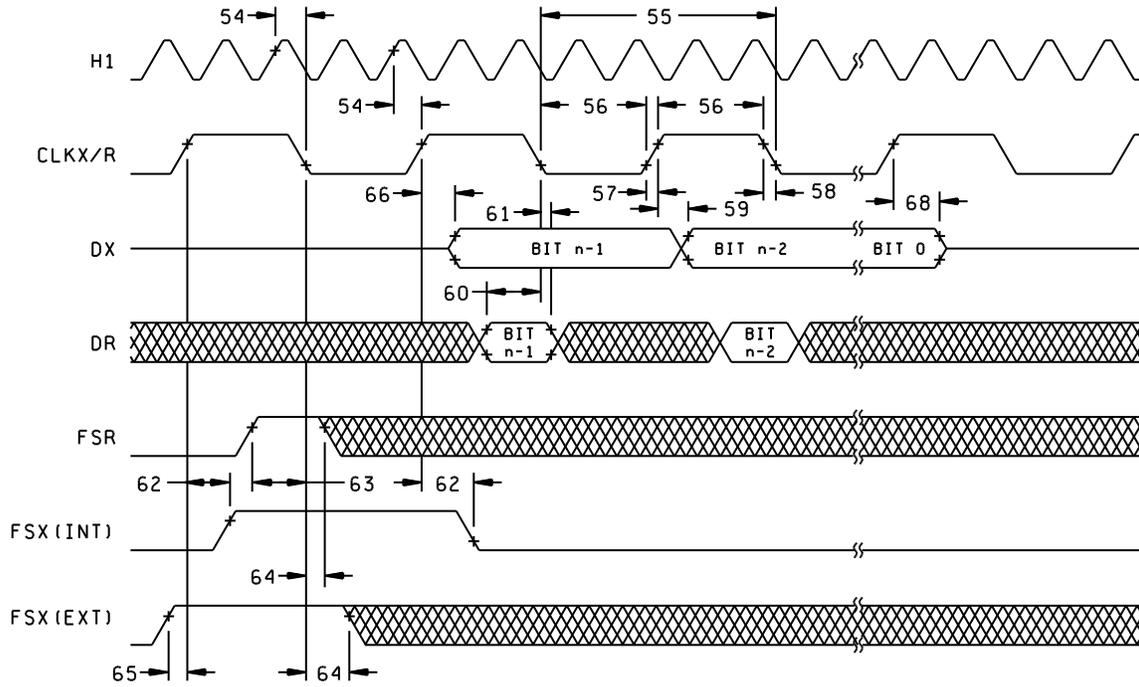


FIGURE 4p. Timing waveforms and test circuit.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 26</p>

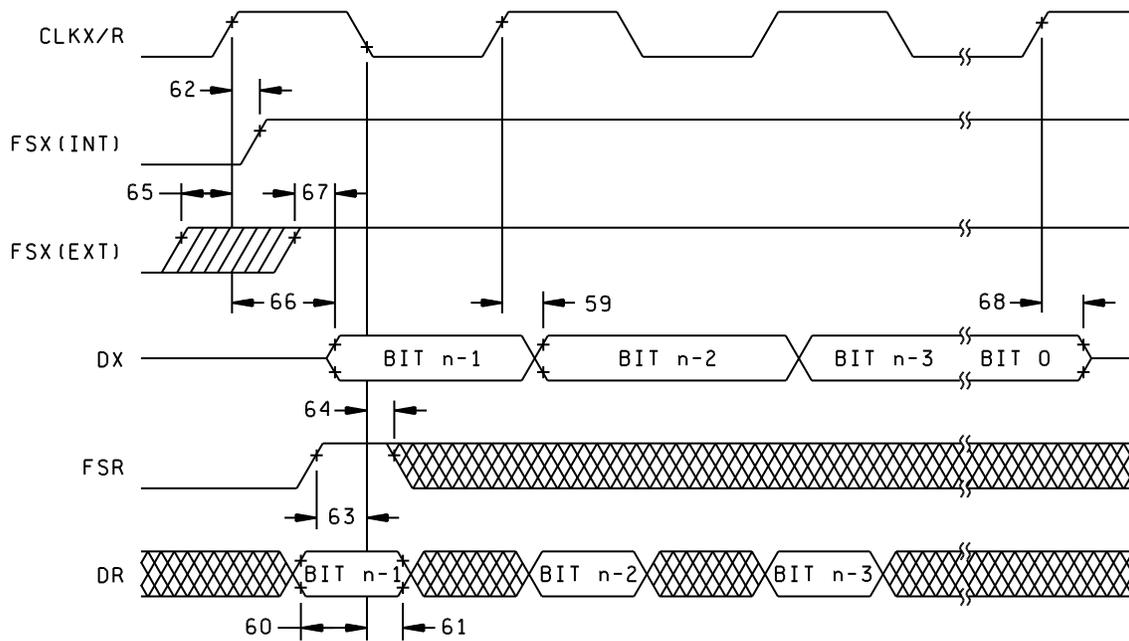


TIMING FOR FIXED DATA-RATE MODE

- NOTES: 1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
 2. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

FIGURE 4q. Timing waveforms and test circuit.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 27</p>

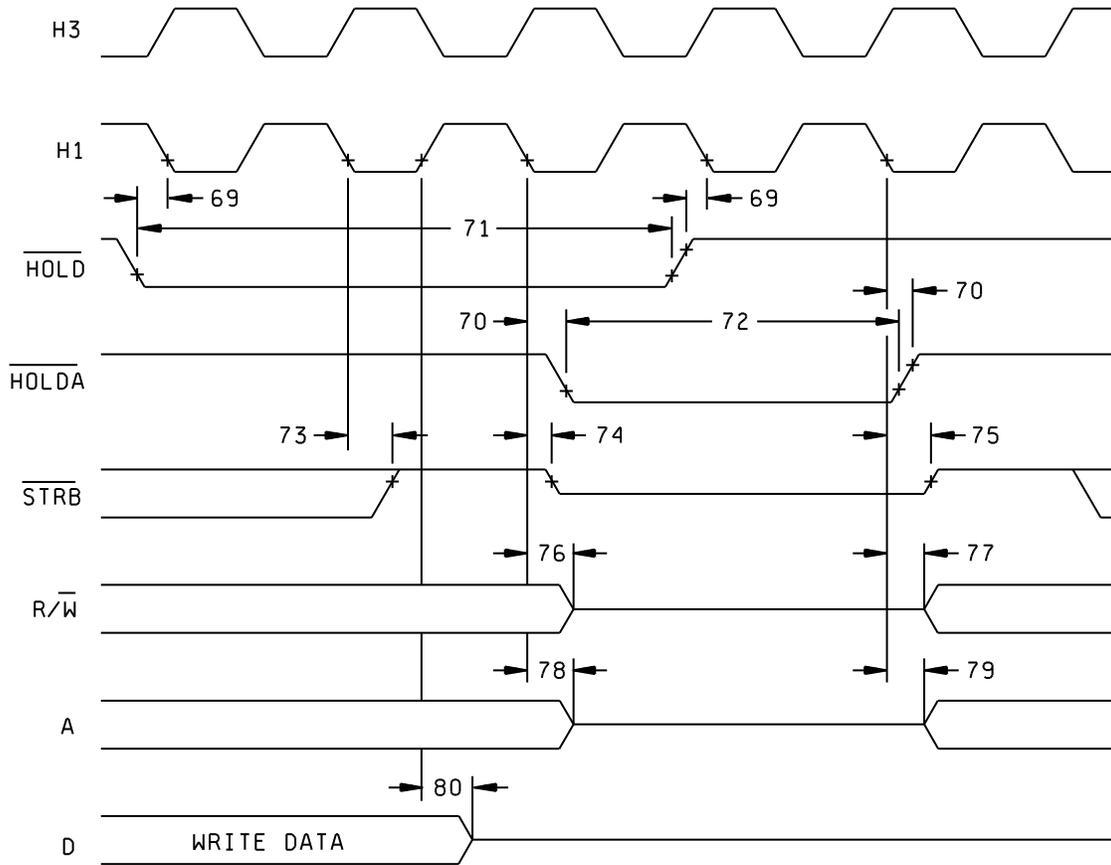


TIMING FOR VARIABLE DATA-RATE MODE

- NOTES: 1. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
 2. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
 3. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

FIGURE 4r. Timing waveforms and test circuit.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 28

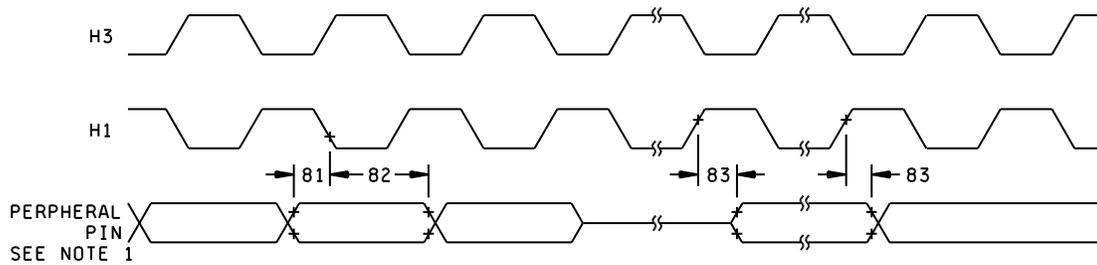


TIMING FOR $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$

NOTE 1. $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

FIGURE 4t. Timing waveforms and test circuit.

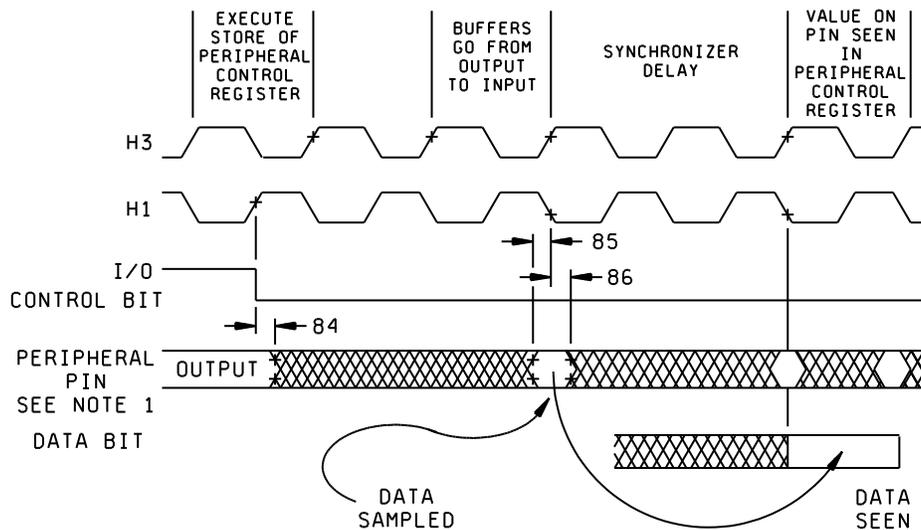
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 29



TIMING FOR PERIPHERAL PIN GENERAL-PURPOSE I/O

NOTE 1. Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

FIGURE 4u. Timing waveforms and test circuit.

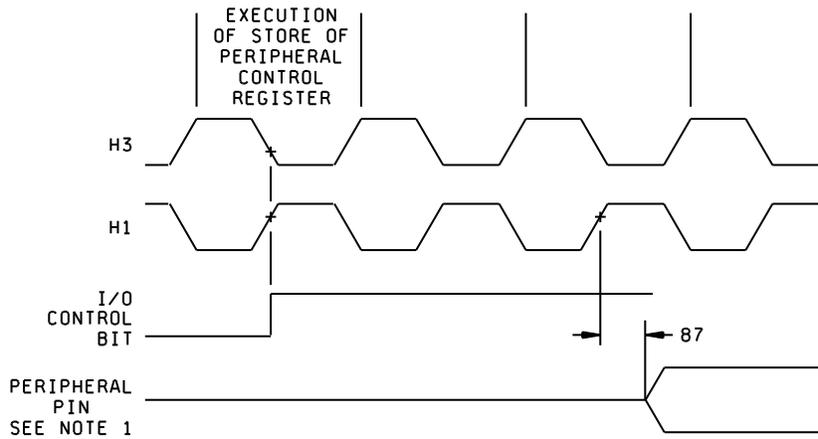


TIMING FOR CHANGE OF PERIPHERAL PIN FROM GENERAL PURPOSE OUTPUT TO INPUT MODE

NOTE 1. Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

FIGURE 4v. Timing waveforms and test circuit.

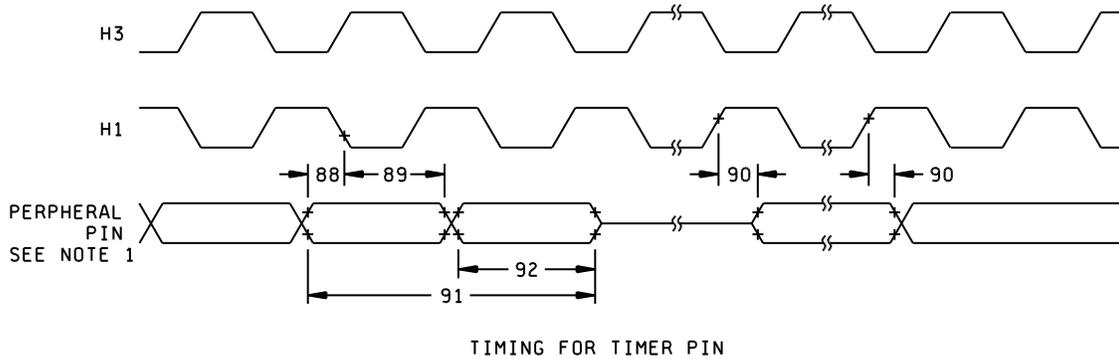
<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 30</p>



TIMING FOR CHANGE OF PERIPHERAL PIN FROM GENERAL PURPOSE INPUT TO OUTPUT MODE

NOTE 1. Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

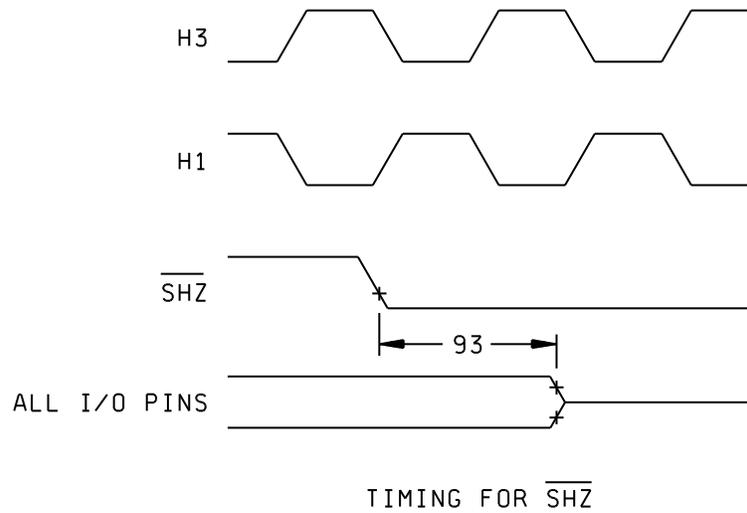
FIGURE 4w. Timing waveforms and test circuit.



NOTE 1. \overline{HOLDA} goes low in response to \overline{HOLD} going low and continues to remain low until one H1 cycle after \overline{HOLD} goes back high.

FIGURE 4x. Timing waveforms and test circuit.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03617</p>
		<p>REV C</p>	<p>PAGE 31</p>



NOTE: Enabling $\overline{\text{SHZ}}$ destroys SM320LC31-EP register and memory contents. Assert $\overline{\text{SHZ}} = 1$ and reset the SM320LC31-EP to restore it to a known condition.

FIGURE 4y. Timing waveforms and test circuit.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 32

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03617-01XE	01295	SM320LC31PQM40EP	SM320LC31-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03617
		REV C	PAGE 33