REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add device type 02. Update boilerplate. Editorial changes throughout. - phn	06-02-22	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	12-03-22	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV	B	B	B	B	B	B	B	B														
PAGE	18	19	20	21	22	23	24	25														

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	**PREPARED BY** Charles F. Saffle	**DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO**
Original date of drawing 02-12-16	**CHECKED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, CMOS, 16-BIT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/03613**
	REV B	**PAGE** 1 **OF** 25

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-bit Digital Signal Processor microcircuit, with an operating temperature range of -55°C to +125°C and of -40°C to +80°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03613	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SM320C50-66EP	16-bit Digital Signal Processor
02	SM320C50-80EP	16-bit Digital Signal Processor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	132	JEDEC MO-069	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD}) ..... -0.3 V to +7.0 V 2/
Input voltage range (V_I) ..... -0.3 V to +7.0 V
Output voltage range (V_O) ..... -0.3 V to +7.0 V
Operating case temperature range (T_C) ..... -55°C to +125°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values are with respect to V_{SS}.

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{DD}) ..... +4.75 V to +5.25 V
Supply voltage (V_{SS})..... 0 V NOM
High level input voltage range (V_{IH}):
CLKIN, CLKIN2 ..... +3.0 V to V_{DD} +0.3 V
CLKX, CLKR, TCLKX, TCLKR ..... +2.5 V to V_{DD} +0.3 V
All others ..... +2.2 V to V_{DD} +0.3 V
Low level input voltage range (V_{IL})..... -0.3 V to +0.6 V
Maximum high level output current (I_{OH}) ..... -300 µA 2/
Maximum low level output current (I_{OL}) ..... +2 mA
Operating case temperature range (T_C):
Device type 01..... -55°C to +125°C 3/
Device type 02..... -40°C to +85°C 3/

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at http://www.ieee.org or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855–1331.

1/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
2/ This I_{OH} can be exceeded when using a 1-kΩ pulldown resistor on the TDM serial port TADD output; however, this output still meets V_{OH} specifications under these conditions.
3/ T_C MAX at maximum rated operating conditions at any point on case. T_C MIN at initial (time zero) power up.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Block diagram. The block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figures 4a – 4q.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 4.75 V ≤ V_{DD} ≤ 5.25 V -55°C ≤ T_C ≤ +125°C 2/ -45°C ≤ T_C ≤ +80°C 3/ unless otherwise specified	Limits		Unit
			Min	Max	
High level output voltage	V_{OH} 4/	I_{OH} = MAX 5/ See figure 4a.	2.4		V
Low level output voltage	V_{OL} 6/	I_{OL} = MAX 5/		0.6	V
High-impedance output current (V_{DD} = MAX)	I_{OZ}	$\overline{BR}$ (with internal pullup)	-500	30	µA
		All others	-30	30	
Input current (V_{IN} = V_{SS} to V_{DD})	I_I	$\overline{TRST}$ (with internal pulldown)	-30	800	µA
		TMS, TCK, TDI (with Internal pullups)	-500	30	
		X2/CLKIN	-50	50	
		All other inputs	-30	30	
Supply current, core CPU	I_{DDC}	Operating, f_x = 66 MHz, V_{DD} = 5.25 V, T_A = 25°C 7/		225	mA
Supply current, pins	I_{DDP}			225	mA
Supply current standby	I_{DD}	IDLE instruction, f_x = 66 MHz, V_{DD} = 5.25 V, T_C = 125°C		30	mA
		IDLE2 instruction, Clocks shut off V_{DD} = 5.25 V, T_C = 125°C		7	µA
Input capacitance	C_i			40	pF
Output capacitance	C_o			40	pF
Internal Divide-by-two Clock Option					
Input clock frequency	f_x		0 8/	66	MHz
Load capacitance	C1, C2	See figure 4b.	10 Typ		pF
External Divide-by-two Clock Option Switching Characteristics [H = 0.5$t_{c(CO)}$]					
Cycle time, CLKOUT1	$t_{c(CO)}$	See figure 4c.	30	9/	ns
Delay time, X2/CLKIN high to CLKOUT1 high/low	$t_{d(CIH-COH/L)}$		3	20	
Fall time, CLKOUT1	$t_{f(CO)}$		5 Typ		
Rise time, CLKOUT1	$t_{r(CO)}$		5 Typ		
Pulse duration, CLKOUT1 low	$t_{w(COL)}$		H–3	H+2	
Pulse duration, CLKOUT1 high	$t_{w(COH)}$		H–3	H+2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions $4.75\ V \le V_{DD} \le 5.25\ V$ $-55°C \le T_C \le +125°C$ 2/ $-45°C \le T_C \le +80°C$ 3/ unless otherwise specified	Limits		Unit
			Min	Max	
External Divide-by-two Clock Option Timing Requirements					
Cycle time, X2/CLKIN	$t_{c(CI)}$	See figure 4c.	15	9/	ns
Fall time, X2/CLKIN	$t_{f(CI)}$			5 10/	ns
Rise time, X2/CLKIN	$t_{r(CI)}$			5 10/	ns
Pulse duration, X2/CLKIN low	$t_{w(CIL)}$		7	9/	ns
Pulse duration, X2/CLKIN high	$t_{w(CIH)}$		7	9/	ns
External Divide-by-one Clock Option Switching Characteristics [H = $0.5t_{c(CO)}$]					
Cycle time, CLKOUT1	$t_{c(CO)}$	See figure 4c	30	75 10/	ns
Delay time, CLKIN2 high to CLKOUT1 high	$t_{d(C2H-COH)}$		2	16	ns
Fall time, CLKOUT1	$t_{f(CO)}$		5 Typ		ns
Rise time, CLKOUT1	$t_{r(CO)}$		5 Typ		ns
Pulse duration, CLKOUT1 low	$t_{w(COL)}$		H–3 10/	H+2 10/	ns
Pulse duration, CLKOUT1 high	$t_{w(COH)}$		H–3 10/	H+2 10/	ns
Delay time, transitory phase – PLL synchronized after CLKIN2 supplied	$t_{d(TP)}$			$1000t_{c(C2)}$ 10/	ns
External Divide-by-one Clock Option Timing Requirements					
Cycle time, CLKIN2	$t_{c(C2)}$		30	75 11/	ns
Fall time, CLKIN2	$t_{f(C2)}$			5 10/	
Rise time, CLKIN2	$t_{r(C2)}$			5 10/	
Pulse duration, CLKIN2 low	$t_{w(C2L)}$		9	$t_{c(C2)}$ - 9	
Pulse duration, CLKIN2 high	$t_{w(C2H)}$		9	$t_{c(C2)}$ - 9	
Memory and Parallel I/O Interface Read Switching Characteristics [H = $0.5t_{c(CO)}$]					
Setup time, address valid before $\overline{RD}$ low	$t_{su(AV-RDL)}$	See figure 4e.	H-10 12/ 13/		ns
Hold time, address valid after $\overline{RD}$ high	$t_{h(RDH-AV)}$		0 12/ 13/		
Pulse duration, $\overline{RD}$ low	$t_{w(RDL)}$		H–2 10/ 14/		
Pulse duration, $\overline{RD}$ high	$t_{w(RDH)}$		H–2 10/ 14/		
Delay time, $\overline{RD}$ high to $\overline{WE}$ low	$t_{d(RDH-WEL)}$		2H-5		
Memory and Parallel I/O Interface Read Timing Requirements [H = $0.5t_{c(CO)}$]					
Access time, read data valid from address valid	$t_{a(RDAV)}$	See figure 4e.		2H-15 13/	ns
Access time, read data valid after $\overline{RD}$ low	$t_{a(RDL-RD)}$			H-10	
Setup time, read data valid before $\overline{RD}$ high	$t_{su(RD-RDH)}$		10		
Hold time, read data valid after $\overline{RD}$ high	$t_{h(RDH-RD)}$		0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 4.75 V ≤ V_{DD} ≤ 5.25 V -55°C ≤ T_C ≤ +125°C 2/ -45°C ≤ T_C ≤ +80°C 3/ unless otherwise specified	Limits		Unit
			Min	Max	
Memory and Parallel I/O Interface Write Switching Characteristics [H = 0.5$t_{c(CO)}$]					
Setup time, address valid before $\overline{WE}$ low	$t_{su(AV-WEL)}$		H-5 12/ 13/		ns
Hold time, address valid after $\overline{WE}$ high	$t_{h(WEH-AV)}$		H-10 12/ 13/		ns
Pulse duration, $\overline{WE}$ low	$t_{w(WEL)}$		2H-4 10/ 15/	2H+2 10/ 15/	ns
Pulse duration, $\overline{WE}$ high	$t_{w(WEH)}$		2H-2 15/		ns
Delay time, $\overline{WE}$ high to $\overline{RD}$ low	$t_{d(WEH-RDL)}$		3H-10		ns
Setup time, write data valid before $\overline{WE}$ high	$t_{su(WDV-WEH)}$		2H-20 10/ 15/	2H 10/ 15/ 16/	ns
Hold time, write data valid after $\overline{WE}$ high	$t_{h(WEH-WDV)}$		H-5 10/ 15/	H+10 10/ 15/	ns
Enable time, $\overline{WE}$ to data bus driven	$t_{en(WE-Bud)}$		-5 10/		ns
Ready Timing for Externally Generated Wait States Timing Requirements [H = 0.5$t_{c(CO)}$]					
Setup time, READY before CLKOUT1 rises	$t_{su(RY-COH)}$	See figure 4g.	10		ns
Hold time, READY after CLKOUT1 rises	$t_{h(CO-RYH)}$		0		ns
Setup time, READY before $\overline{RD}$ falls	$t_{su(RY-RDL)}$		10		ns
Hold time, READY after $\overline{RD}$ falls	$t_{h(RDL-RY)}$		0		ns
Valid time, READY after $\overline{WE}$ falls	$t_{v(WEL-RY)}$		H-15		ns
Hold time, READY after $\overline{WE}$ falls	$t_{h(WEL-RY)}$		H+5		ns
Reset, Interrupt, and BIO Timing Requirements [H = 0.5$t_{c(CO)}$]					
Setup time, $\overline{INT1}$-$\overline{INT4}$, $\overline{NMI}$, before CLKOUT1 low 14/	$t_{su(IN-COL)}$	See figure 4h.	15		ns
Hold time, $\overline{INT1}$-$\overline{INT4}$, $\overline{NMI}$, after CLKOUT1 low 14/	$t_{h(COL-IN)}$		0		ns
Pulse duration $\overline{INT1}$-$\overline{INT4}$, $\overline{NMI}$ low, synchronous	$t_{w(INL)SYN}$		4H+15 18/		ns
Pulse duration, $\overline{INT1}$-$\overline{INT4}$, $\overline{NMI}$ high, synchronous	$t_{w(INH)SYN}$		2H+15 10/ 18/		ns
Pulse duration, $\overline{INT1}$-$\overline{INT4}$, $\overline{NMI}$ low, asynchronous	$t_{w(INL)ASY}$		6H+15 10/ 18/		ns
Pulse duration, $\overline{INT1}$-$\overline{INT4}$, $\overline{NMI}$ high, asynchronous	$t_{w(INH)ASY}$		4H+15 10/ 18/		ns
Setup time, $\overline{RS}$ before X2/CLKIN low	$t_{su(RS-X2L)}$		10		ns
Pulse duration, $\overline{RS}$ low	$t_{w(RSL)}$		12H		ns
Delay time, $\overline{RS}$ high to reset vector fetch	$t_{d(RSH)}$		34H		ns
Pulse duration, $\overline{BIO}$ low, synchronous	$t_{w(BIL)SYN}$		15		ns
Pulse duration, $\overline{BIO}$ low, asynchronous	$t_{w(BIL)ASY}$		H+15 10/		ns
Setup time, $\overline{BIO}$ before CLKOUT1 low	$t_{su(BI-COL)}$		15		ns
Hold time, $\overline{BIO}$ after CLKOUT1 low	$t_{h(COL-BI)}$		0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 4.75 V ≤ V_{DD} ≤ 5.25 V -55°C ≤ T_C ≤ +125°C 2/ -45°C ≤ T_C ≤ +80°C 3/ unless otherwise specified	Limits		Unit
			Min	Max	
Instruction Acquisition (IAQ), Interrupt Acknowledge (IACK), External Flag(XF) and TOUT Switching Characteristics [H = 0.5$t_{c(CO)}$]					
Setup time, address valid before $\overline{IAQ}$ low 19/	$t_{su(AV-IQL)}$	See figure 4i.	H-12 20/		ns
Hold time, address valid after $\overline{IAQ}$ low	$t_{h(IQL-AV)}$		H-10 20/		ns
Pulse duration, $\overline{IAQ}$ low	$t_{w(IQL)}$		H-10 20/		ns
Delay time, CLKOUT1 falling to TOUT	$t_{d(CO-TU)}$		-6	6	ns
Setup time, address valid before $\overline{IACK}$ low 21/	$t_{su(AV-IKL)}$		H-12 20/		ns
Hold time, address valid after $\overline{IAQ}$ high 21/	$t_{h(IKH-AV)}$		H-10 20/		ns
Pulse duration, $\overline{IAQ}$ low	$t_{w(IKL)}$		H-10 20/		ns
Pulse duration, TOUT high	$t_{w(TUH)}$		2H-12		ns
Delay time, XF valid after CLKOUT1	$t_{d(CO-XFV)}$		0	12	ns
External DMA Timing Switching Characteristics [H = 0.5$t_{c(CO)}$] 22/					
Delay time, $\overline{HOLD}$ low to $\overline{HOLDA}$ low	$t_{d(HOL-HAL)}$	See figure 4j.	4H	23/	ns
Delay time, $\overline{HOLD}$ high before $\overline{HOLDA}$ high	$t_{d(HOH-HAH)}$		2H		ns
Disable time, address in the high- impedance state before $\overline{HOLDA}$ low	$t_{dis(AZ-HAL)}$		H-15 10/ 24/		ns
Enable time, $\overline{HOLDA}$ high to address driven	$t_{en(HAH-Ad)}$		H-5 10/		ns
Delay time, $\overline{XBR}$ low to $\overline{IAQ}$ low	$t_{d(XBL-IQL)}$		4H 10/	6H 10/	ns
Delay time, $\overline{XBR}$ high to $\overline{IAQ}$ high	$t_{d(XBH-IQH)}$		2H 10/	4H 10/	ns
Delay time, read data valid after $\overline{XSTRB}$ low	$t_{d(XSL-RDV)}$			40	ns
Hold time, read data after $\overline{XSTRB}$ high	$t_{h(XSH-RD)}$		0		ns
Enable time, $\overline{IAQ}$ low to read data driven	$t_{en(IQL-RDd)}$		0 10/ 25/	2H 10/	ns
Disable time, XR/$\overline{W}$ low to data in the high-impedance state	$t_{dis(W)}$		0 10/	15 10/	ns
Disable time, $\overline{IAQ}$ high to data in the high-impedance state	$t_{dis(I-D)}$			H 10/	ns
Enable time, data from XR/$\overline{W}$ going high	$t_{en(D-XRH)}$			4 10/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $4.75\ V \le V_{DD} \le 5.25\ V$ $-55°C \le T_C \le +125°C$ 2/ $-45°C \le T_C \le +80°C$ 3/ unless otherwise specified	Limits		Unit
			Min	Max	
External DMA Timing, Timing Requirements 22/					
Delay time, $\overline{HOLDA}$ low to $\overline{XBR}$ low	$t_{d(HAL-XBL)}$	See figure 4j.	0 26/		ns
Delay time, $\overline{IAQ}$ low to $\overline{XSTRB}$ low	$t_{d(IQL-XSL)}$		0 26/		ns
Setup time, Xaddress valid before $\overline{XSTRB}$ low	$t_{su(AV-XSL)}$		15		ns
Setup time, Xdata valid before $\overline{XSTRB}$ low	$t_{su(DV-XSL)}$		15		ns
Hold time, Xdata hold after $\overline{XSTRB}$ low	$t_{h(XSL-D)}$		15		ns
Hold time, write Xaddress hold after $\overline{XSTRB}$ low	$t_{h(XSL-WA)}$		15		ns
Pulse duration, $\overline{XSTRB}$ low	$t_{w(XSL)}$		45		ns
Pulse duration, $\overline{XSTRB}$ high	$t_{w(XSH)}$		45		ns
Setup time, R/$\overline{W}$ valid before $\overline{XSTRB}$ low	$t_{su(RW-XSL)}$		20		ns
Hold time, read Xaddress after $\overline{XSTRB}$ high	$t_{h(XSH-RA)}$		0		ns
Serial-Port Receive Timing Requirements [$H = 0.5t_{c(CO)}$]					
Cycle time, serial-port clock	$t_{c(SCK)}$	See figure 4k.	5.2H	27/	ns
Fall time, serial-port clock	$t_{f(SCK)}$			8 10/	ns
Rise time, serial-port clock	$t_{r(SCK)}$			8 10/	ns
Pulse duration, serial-port clock low/high	$t_{w(SCK)}$		2.1H		ns
Setup time, FSR before CLKR falling edge	$t_{su(FS-CK)}$		10		ns
Hold time, FSR after CLKR falling edge	$t_{h(CK-FS)}$		10		ns
Setup time, DR before CLKR falling edge	$t_{su(DR-CK)}$		10		ns
Hold time, DR after CLKR falling edge	$t_{h(CK-DR)}$		10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 4.75 V ≤ V_{DD} ≤ 5.25 V -55°C ≤ T_C ≤ +125°C 2/ -45°C ≤ T_C ≤ +80°C 3/ unless otherwise specified	Limits		Unit
			Min	Max	
Serial-Port Transmit, External Clocks and External Frames Switching Characteristics 28/					
Delay time, DX valid after CLKX high	$t_{d(CXH-DXV)}$	See figure 4m.		25	ns
Disable time, DX valid after CLKX high	$t_{dis(CXH-DX)}$			40 10/	ns
Hold time, DX valid after CLKX high	$t_{h(CXH-DXV)}$		-5		ns
Serial-Port Transmit, External Clocks and External Frames Timing Requirements [H = 0.5$t_{c(CO)}$] 28/					
Cycle time, serial-port clock	$t_{c(SCK)}$	See figure 4m.	5.2H	27/	ns
Fall time, serial-port clock	$t_{f(SCK)}$			8 10/	ns
Rise time, serial-port clock	$t_{r(SCK)}$			8 10/	ns
Pulse duration, serial-port clock low/high	$t_{w(SCK)}$		2.1H		ns
Delay time, FSX after CLKX high edge	$t_{d(CXH-FXH)}$			2H-8	ns
Hold time, FSX after CLKX falling edge	$t_{h(CXL-FXL)}$		10		ns
Hold time, FSX after CLKX high edge	$t_{h(CXH-FXL)}$			2H-8 10/ 29/	ns
Serial-Port Transmit, Internal Clocks and Internal Frames Switching Characteristics [H = 0.5$t_{c(CO)}$] 28/					
Delay time, CLKX rising to FSX	$t_{d(CX-FX)}$	See figure 4n.		25	ns
Delay time, CLKX rising to DX	$t_{d(CX-DX)}$			25	ns
Disable time, CLKX rising to DX	$t_{dis(CX-DX)}$			40 10/	ns
Cycle time, serial-port clock	$t_{c(SCK)}$		8H Typ		ns
Fall time, serial-port clock	$t_{f(SCK)}$		5 Typ		ns
Rise time, serial-port clock	$t_{r(SCK)}$		5 Typ		ns
Pulse duration, serial-port clock low/high	$t_{w(SCK)}$		4H-20		ns
Hold time, DX valid after CLKX high	$t_{h(CXH-DXV)}$		-6		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 4.75 V ≤ V_{DD} ≤ 5.25 V -55°C ≤ T_C ≤ +125°C 2/ -45°C ≤ T_C ≤ +80°C 3/ unless otherwise specified	Limits		Unit
			Min	Max	
Serial-Port Receive Timing in TDM Mode Timing Requirements [H = 0.5$t_{c(CO)}$]					
Cycle time, serial-port clock	$t_{c(SCK)}$	See figure 4p.	5.2H	27/	ns
Fall time, serial-port clock	$t_{f(SCK)}$			8 10/	ns
Rise time, serial-port clock	$t_{r(SCK)}$			8 10/	ns
Pulse duration, serial-port clock low/high	$t_{w(SCK)}$		2.1H		ns
Setup time, TDAT/TADD before TCLK rising	$t_{su(TD-TCH)}$		30		ns
Hold time, TDAT/TADD after TCLK rising	$t_{h(TCH-TD)}$		-3		ns
Setup time, TDAT/TADD before TCLK rising 30/	$t_{su(TA-TCH)}$		20		ns
Hold time, TDAT/TADD after TCLK rising 30/	$t_{h(TCH-TA)}$		-3		ns
Setup time, TFRM before TCLK rising edge 31/	$t_{su(TF-TCH)}$		10		ns
Hold time, TFRM after TCLK rising edge 31/	$t_{h(TCH-TF)}$		10		ns
Serial-Port Transmit Timing in TDM Mode Switching Characteristics [H = 0.5$t_{c(CO)}$]					
Hold time, TDAT/TADD valid after TCLK rising	$t_{h(TCH-TDV)}$		0		ns
Delay time, TFRM valid after TCLK rising 32/	$t_{d(TCH-TFV)}$		H	3H+10	ns
Delay time, TCLK to valid TDAT/TADD	$t_{d(TC-TDV)}$			20	ns
Serial-Port Transmit Timing in TDM Mode Timing Requirements [H = 0.5$t_{c(CO)}$]					
Cycle time, serial-port clock	$t_{c(SCK)}$		5.2H	24/	ns
Fall time, serial-port clock	$t_{f(SCK)}$			8 10/	ns
Rise time, serial-port clock	$t_{r(SCK)}$			8 10/	ns
Pulse duration, serial-port clock low/high	$t_{w(SCK)}$		2.1H		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ For device type 01
3/ For device type 02.
4/ All input and output voltage levels are TTL compatible. Figure 4a shows the test load circuit and the voltage reference levels.
5/ For conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.
6/ All typical or nominal values are at V_{DD} = 5 V, T_A (ambient air temperature) = 25°C.
7/ This test is performed at T_A (ambient air temperature) = 25°C.
8/ This device uses a fully static design and, therefore, can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 3.3 MHz to meet device test time requirements.
9/ This device uses a fully static design and, therefore, can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 6.7 MHz to meet device test time requirements.
10/ This parameter is not production tested.
11/ Clocks can be stopped only while the device executes IDLE2 when using the external divide-by-one clock option. Note that tp (the transitory phase) occurs when restarting clock from IDLE2 in this mode.
12/ A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as address.
13/ See figure 4f for address-bus timing variation with load capacitance.
14/ $\overline{STRB}$ and $\overline{RD}$ timing is –3/+5 ns from CLKOUT1 timing on read cycles, following the first cycle after reset, which is always a seven wait-state cycle.
15/ $\overline{STRB}$ and $\overline{WE}$ edges are 0-4 ns from CLKOUT1 edges on writes. Rising and falling edges of these signals track each other; tolerance of resulting pulse durations is ±2 ns, not ±4 ns.
16/ This value holds true for zero or one wait state only.
17/ These parameters must be met to use the synchronous timings. Both reset and the interrupts can operate asynchronously. The pulse durations require an extra half-cycle to assure internal synchronization.
18/ If in IDLE2, add 4H to these timings.
19/ $\overline{IAQ}$ goes low during an instruction acquisition. It goes low only on the first cycle of the read when wait states are used. The falling edge should be used to latch the valid address. The AVIS bit in the PMST register must be set to zero for the address to be valid when the instruction being addressed resides in on-chip memory.
20/ Valid only if the external address reflects the current instruction activity (that is, code is executing on-chip with no external bus cycles and AVIS is on, or code is executing off-chip).
21/ $\overline{IACK}$ goes low during the fetch of the first word of the interrupt vector. It goes low only on the first cycle of the read when wait states are used. Address pins A1-A4 can be decoded at the falling edge to identify the interrupt being acknowledged. The AVIS bit in the PMST register must be set to zero for the address to be valid when the vectors reside in on-chip memory.
22/ X preceding a name refers to the external drive of the signal.
23/ $\overline{HOLD}$ is not acknowledged until current external access request is complete.
24/ This parameter includes all memory control lines.
25/ This parameter refers to the delay between the time the condition ($\overline{IAQ}$ = 0 and XR/$\overline{W}$ = 1) is satisfied and the time that the 320C50x data lines become valid.
26/ XBR, XR/$\overline{W}$, and $\overline{XSTRB}$ lines should be pulled up with a 10-kΩ resistor to assure that they are in an inactive (high) state during the transition period between the 320C50x driving them and the external circuit driving them.
27/ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
28/ Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX are always defined depending on the source of FSX, and CLKX timings are always dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.
29/ If the FSX pulse does not meet this specification, the first bit of serial data is driven on the DX pin until the falling edge of FSX. After the falling edge of FSX, data is shifted out on the DX pin. The transmit-buffer-empty interrupt is generated when the $t_{h(FS)}$ and $t_{h(FS)H}$ specification is met.
30/ These parameters apply only to the first bits in the serial bit string.
31/ TFRM timing and waveforms shown in figure 4p are for external TFRM. TFRM also can be configured as internal. The TFRM internal case is illustrated in the transmit timing diagram in figure 4q.
32/ TFRM timing and waveforms shown in figure 4q are for internal TFRM. TFRM also can be configured as external. The TFRM external case is illustrated in the receive timing diagram in figure 4p.

Case X

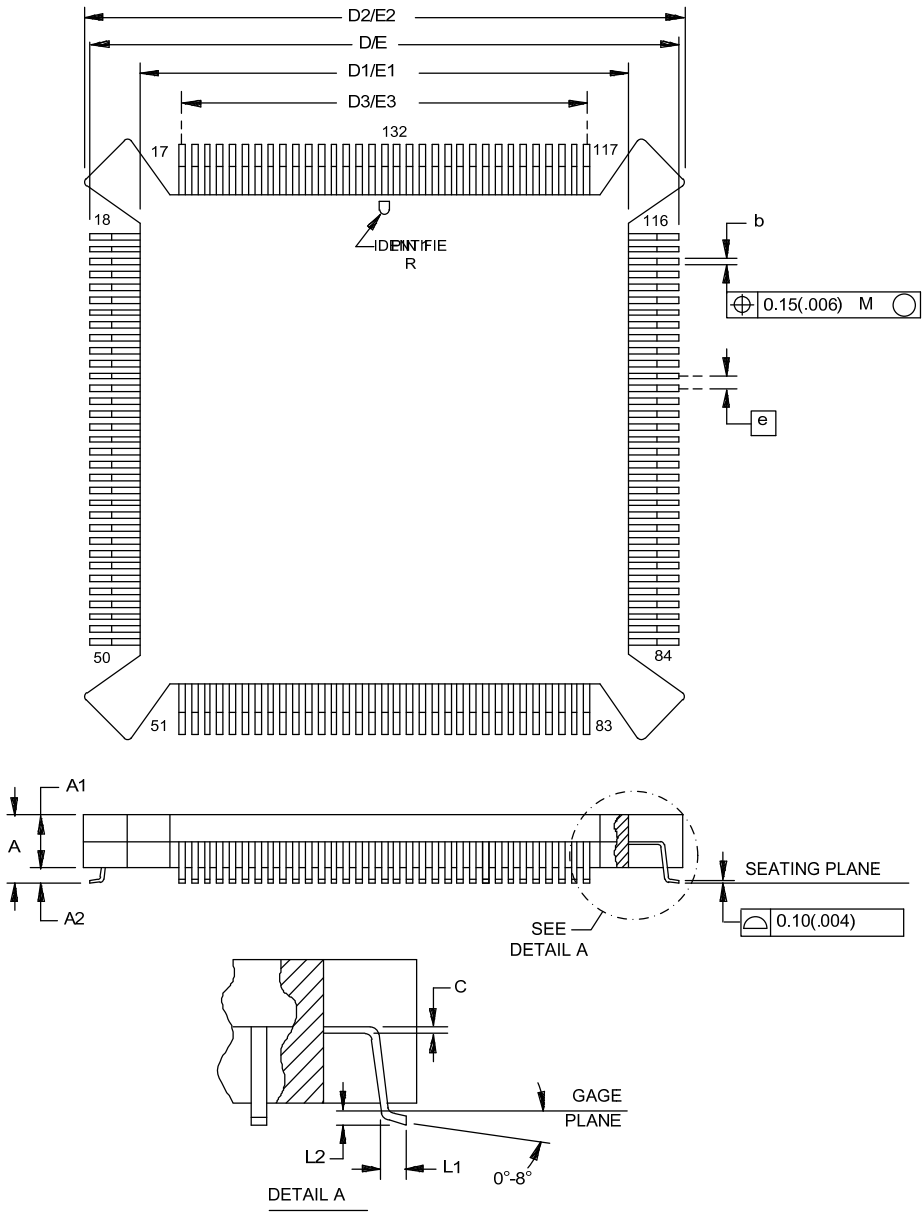


FIGURE 1. Case outlines.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03613
		REV B	PAGE 13

Case X - Continued

Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		4.57		0.180	D3	20.32 NOM		0.800 NOM	
A1	3.30	3.81	0.130	0.150	E	27.18	27.69	1.070	1.090
A2	0.51		0.020		E1	23.72	24.54	0.934	0.966
b	0.20	0.30	0.008	0.012	E2	27.64	28.25	1.088	1.112
C	0.16 NOM		0.006 NOM		E3	20.32 NOM		0.800 NOM	
D	27.18	27.69	1.070	1.090	e	0.635 TYP		0.025 TYP	
D1	23.72	24.54	0.934	0.966	L1	0.91	1.17	0.036	0.046
D2	27.64	28.25	1.088	1.112	L2	0.25 TYP		0.010 TYP	

NOTES:
1. This drawing is subject to change without notice.
2. Falls within JEDEC MO-069.
3. All linear dimensions are in millimeters (inches).

FIGURE 1. Case outlines – Continued.

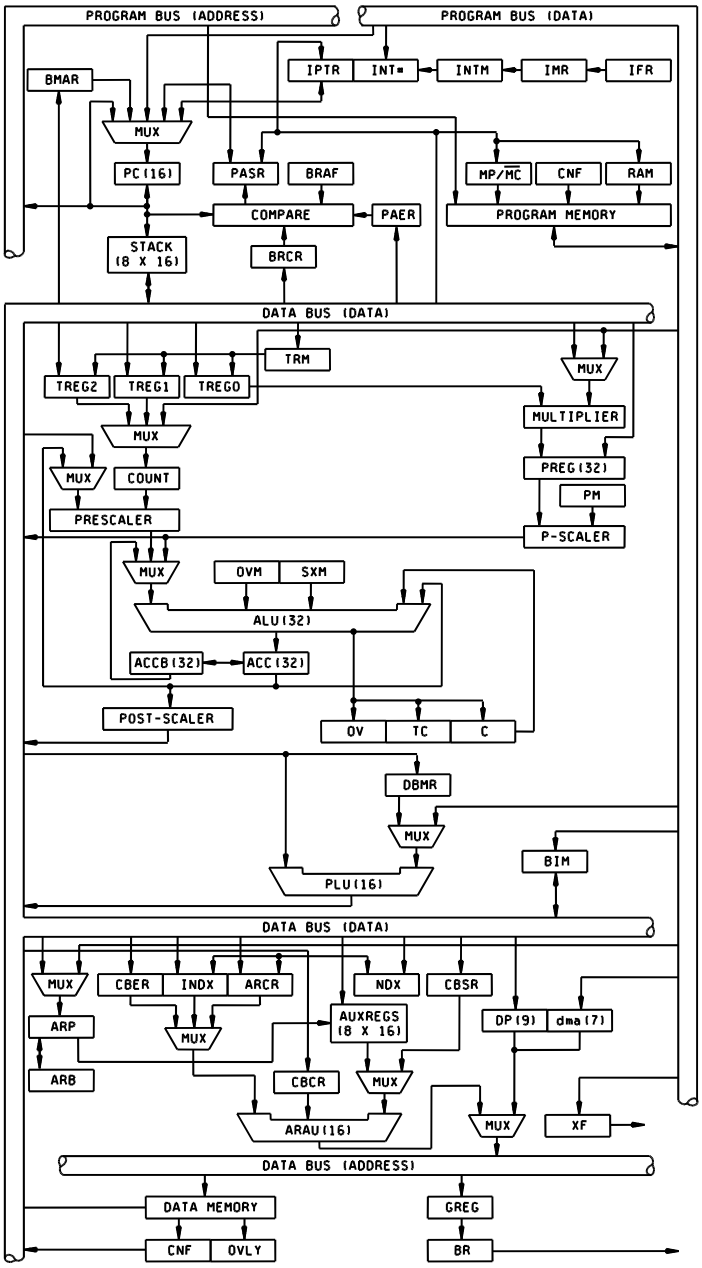
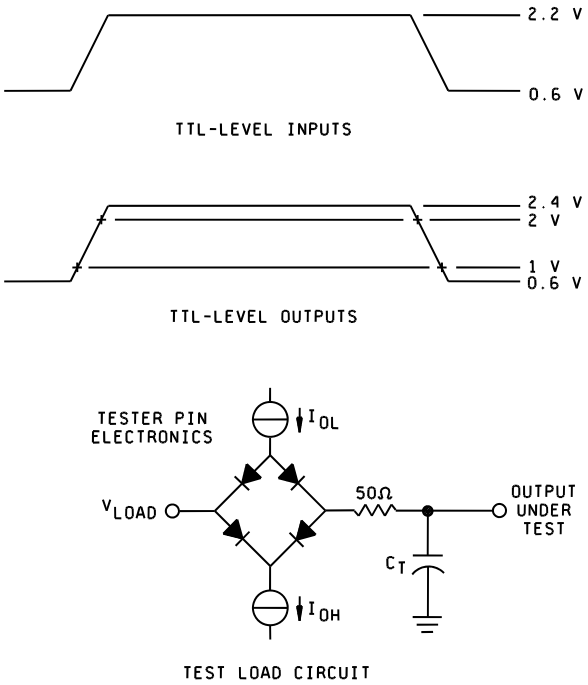


FIGURE 2. Block diagram.

Device type		01					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{IAQ}$	34	TCK	67	TDI	100	TDO
2	$\overline{TRST}$	35	V_{SS5}	68	V_{SS9}	101	V_{SS13}
3	V_{SS1}	36	V_{SS6}	69	V_{SS10}	102	V_{SS14}
4	V_{SS2}	37	NC	70	NC	103	CLKMD2
5	MP/$\overline{MC}$	38	$\overline{INT1}$	71	CLKMD1	104	FSX
6	D15(MSB)	39	$\overline{INT2}$	72	A10	105	TFSX/TFRM
7	D14	40	$\overline{INT3}$	73	A11	106	DX
8	D13	41	$\overline{INT4}$	74	A12	107	TDX
9	D12	42	$\overline{NMI}$	75	A13	108	$\overline{HOLDA}$
10	D11	43	DR	76	A14	109	XF
11	D10	44	TDR	77	A15(MSB)	110	CLKOUT1
12	D9	45	FSR	78	NC	111	NC
13	D8	46	CLKR	79	NC	112	$\overline{IACK}$
14	V_{DD1}	47	V_{DD5}	80	V_{DD9}	113	V_{DD13}
15	V_{DD2}	48	V_{DD6}	81	V_{DD10}	114	V_{DD14}
16	NC	49	NC	82	$\overline{RD}$	115	NC
17	NC	50	NC	83	$\overline{WE}$	116	NC
18	NC	51	NC	84	NC	117	NC
19	NC	52	NC	85	NC	118	EMU0
20	V_{SS3}	53	V_{SS7}	86	V_{SS11}	119	EMU1/$\overline{OFF}$
21	V_{SS4}	54	V_{SS8}	87	V_{SS12}	120	V_{SS15}
22	NC	55	A0	88	NC	121	V_{SS16}
23	D7	56	A1	89	$\overline{DS}$	122	TOUT
24	D6	57	A2	90	$\overline{IS}$	123	TCLKX
25	D5	58	A3	91	$\overline{PS}$	124	CLKX
26	D4	59	A4	92	R/$\overline{W}$	125	TFSR/TADD
27	D3	60	A5	93	$\overline{STRB}$	126	TCLKR
28	D2	61	A6	94	$\overline{BR}$	127	$\overline{RS}$
29	D1	62	A7	95	CLKIN2	128	READY
30	D0(LSB)	63	A8	96	X2/CLKIN	129	$\overline{HOLD}$
31	TMS	64	A9	97	X1	130	$\overline{BIO}$
32	V_{DD3}	65	V_{DD7}	98	V_{DD11}	131	V_{DD15}
33	V_{DD4}	66	V_{DD8}	99	V_{DD12}	132	V_{DD16}

NC = No internal connection.

FIGURE 3. Terminal connections.



Where: I_{OL}
I_{OH} = 500 µA (all outputs)
V_{LOAD} = 1.5 V
C_T = 80 pF typical load circuit capacitance

FIGURE 4a. Timing waveforms and test circuit.

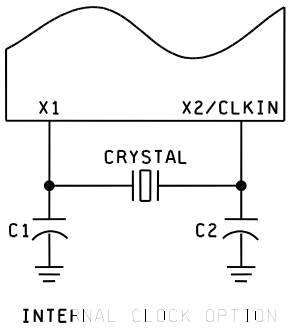


FIGURE 4b. Timing waveforms and test circuit.

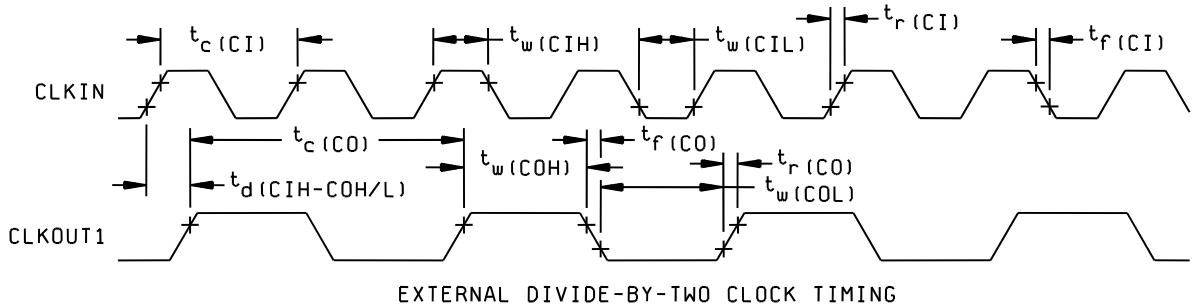


FIGURE 4c. Timing waveforms and test circuit.

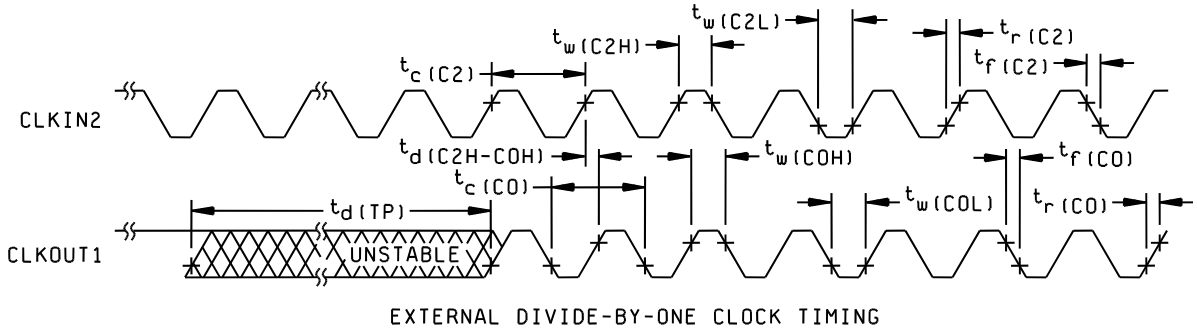
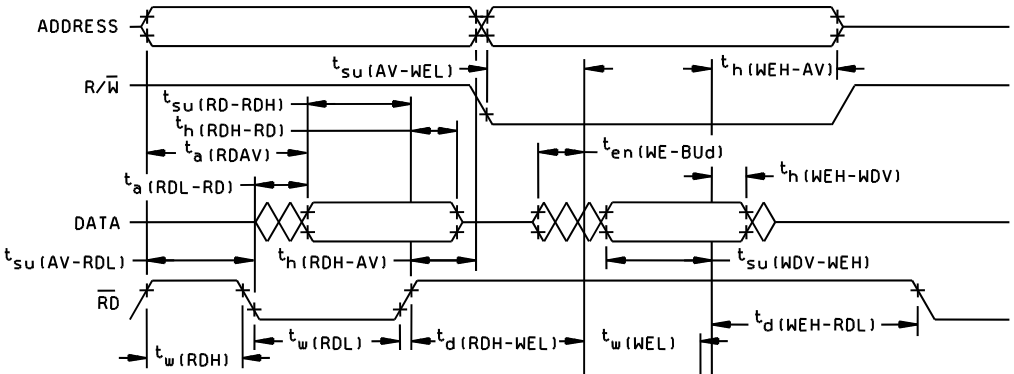
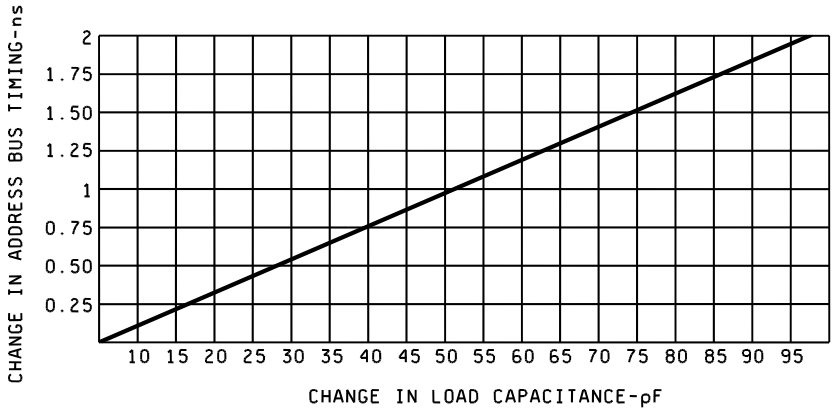


FIGURE 4d. Timing waveforms and test circuit.



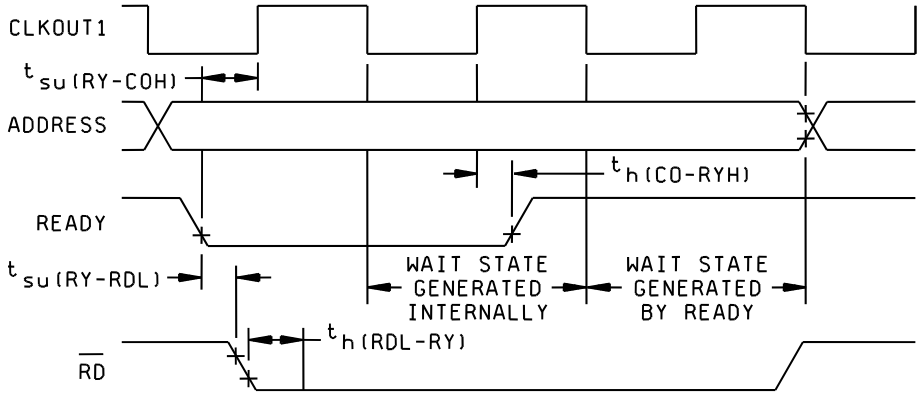
NOTE A: All timings are for 0 wait states. However, external writes always require two cycles to prevent external bus conflicts. The above diagram illustrates a one-cycle read and a two-cycle write and is not drawn to scale. All external writes immediately preceded by an external read or immediately followed by an external read require three machine cycles.

FIGURE 4e. Timing waveforms and test circuit.

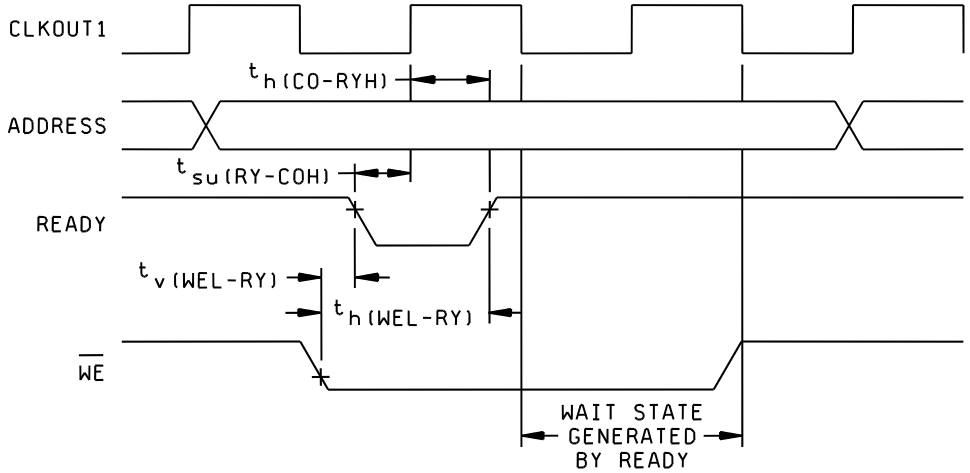


ADDRESS BUS TIMING VARIATION WITH LOAD CAPACITANCE

FIGURE 4f. Timing waveforms and test circuit.



READY TIMING FOR EXTERNALLY GENERATED WAIT STATES DURING AN EXTERNAL READ CYCLE



READY TIMING FOR EXTERNALLY GENERATED WAIT STATES DURING AN EXTERNAL WRITE CYCLE

FIGURE 4g. Timing waveforms and test circuit.

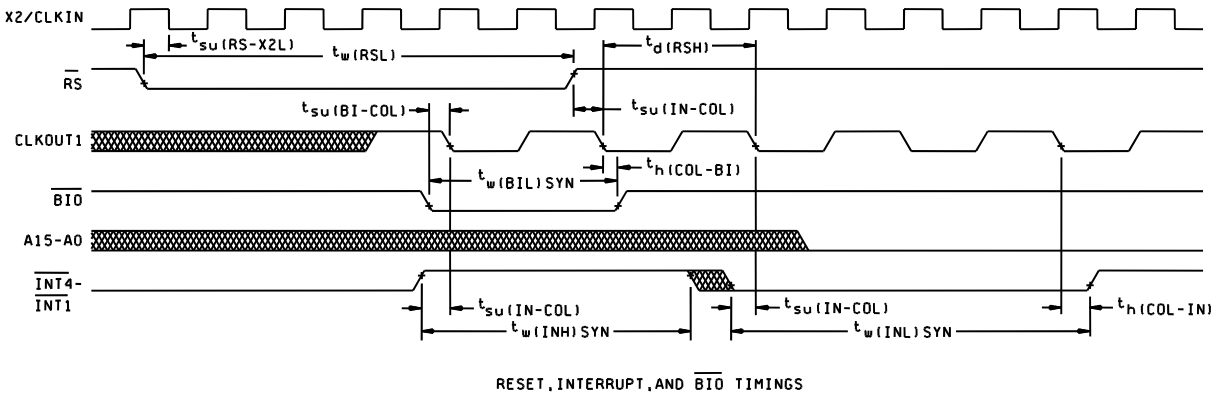
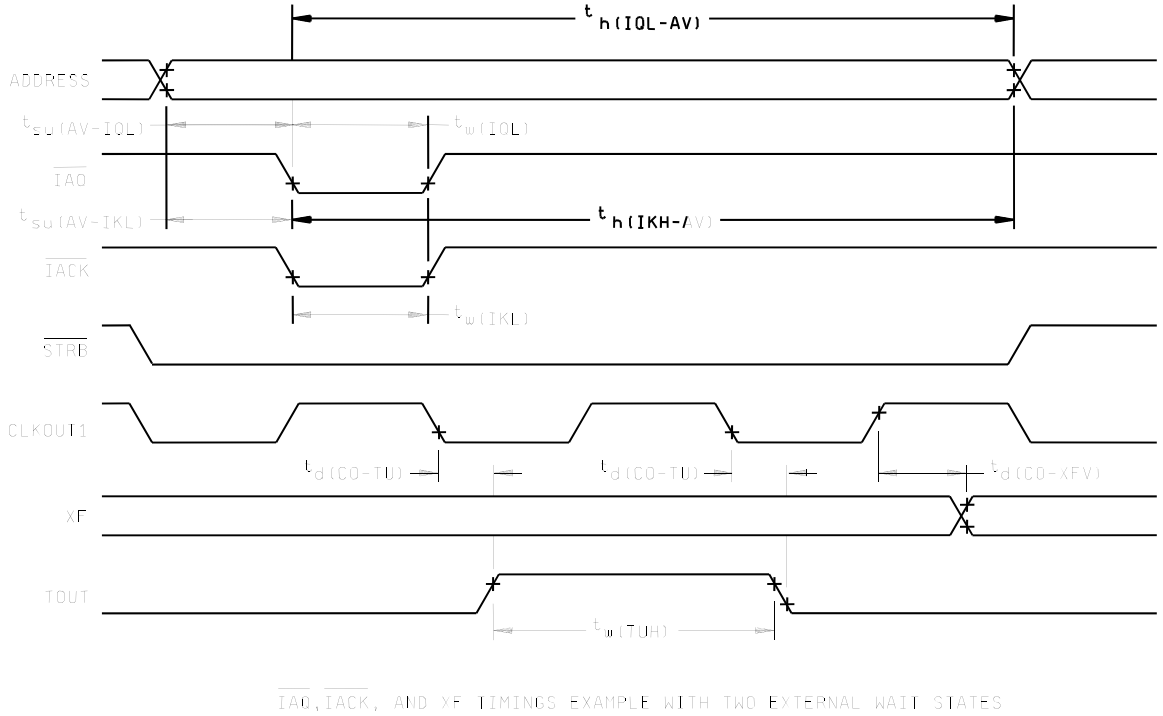
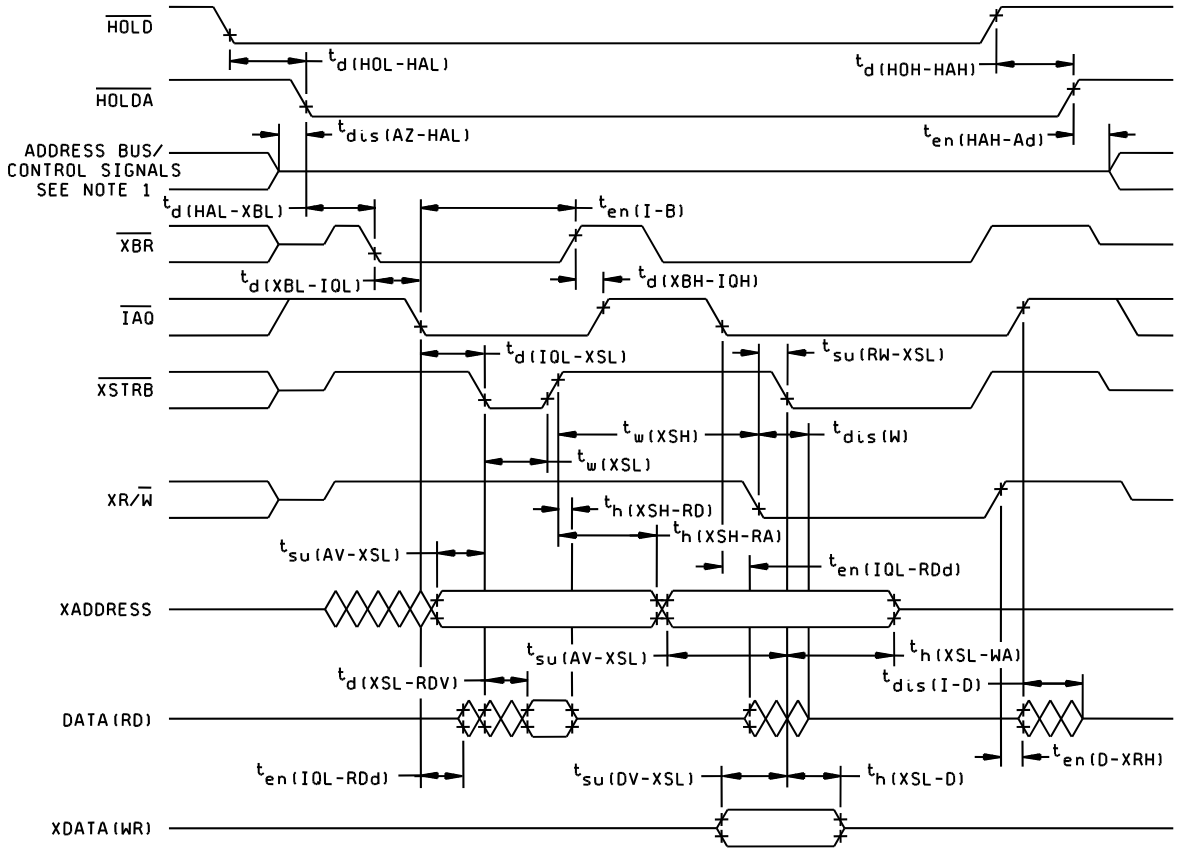


FIGURE 4h. Timing waveforms and test circuit.



NOTE: IAQ and IACK are not affected by wait states.

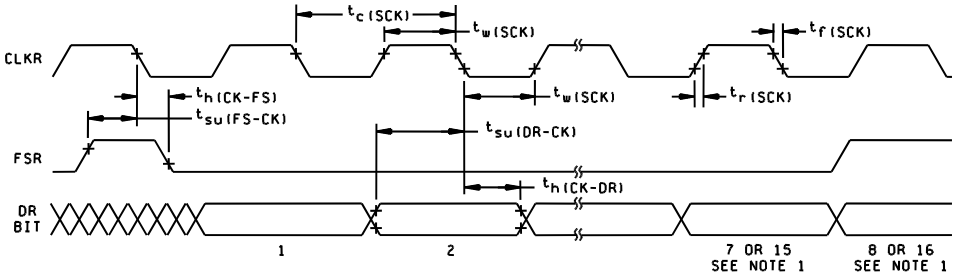
FIGURE 4i. Timing waveforms and test circuit.



EXTERNAL DMA TIMING

NOTE 1: A15-A0, PS, DS, IS, R/W, and BR timings are all included in timings referenced as address bus/control signals.

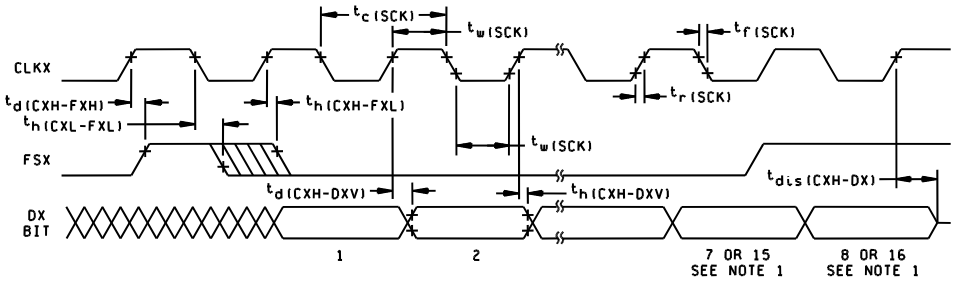
FIGURE 4j. Timing waveforms and test circuit.



SERIAL PORT RECEIVE TIMING

NOTE 1: Depending on whether information is sent in an 8-bit or 16-bit packet.

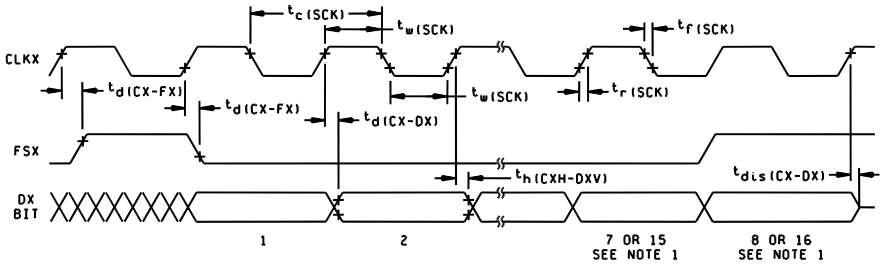
FIGURE 4k. Timing waveforms and test circuit.



SERIAL-PORT TRANSMIT TIMING OF EXTERNAL CLOCKS AND EXTERNAL FRAMES

NOTE 1: Depending on whether information is sent in an 8-bit or 16-bit packet.

FIGURE 4m. Timing waveforms and test circuit.



SERIAL-PORT TRANSMIT TIMING OF INTERNAL CLOCKS AND INTERNAL FRAMES

NOTE 1: Depending on whether information is sent in an 8-bit or 16-bit packet.

FIGURE 4n. Timing waveforms and test circuit.

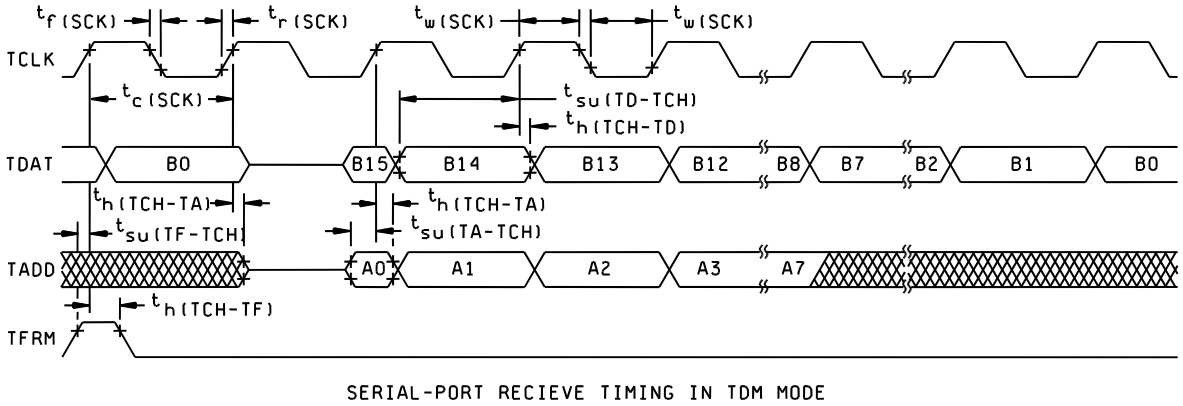


FIGURE 4p. Timing waveforms and test circuit.

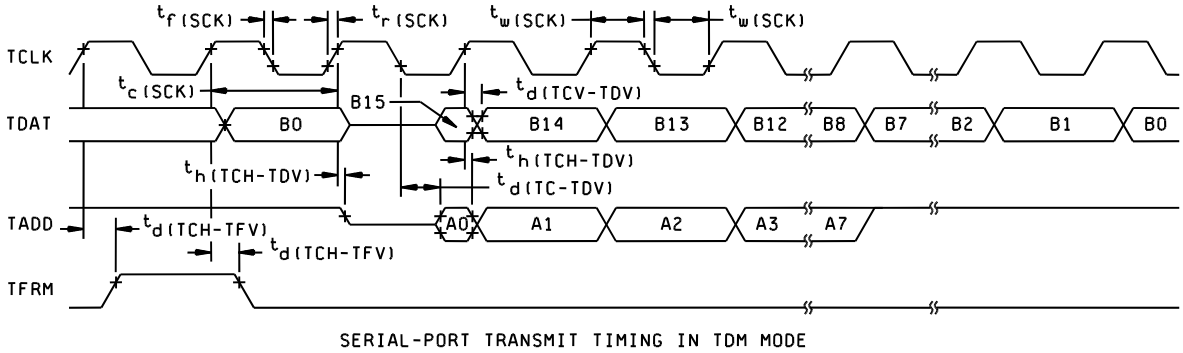


FIGURE 4q. Timing waveforms and test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03613-01XE	01295	SM320C50PQM66EP	SM320C50-EP
V62/03613-02XE	01295	SM320C50PQI80EP	SM320C50-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493