REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate paragraphs to current requirements. - PHN	09-02-04	Charles F. Saffle
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	15-07-28	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B									
	PAGE	1	2	3	4	5	6	7	8	9	10									

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 02-11-05	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, ADVANCED CMOS, 16-BIT BUS TRANSCEIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** V62/03601
	REV B	**PAGE** 1 **OF** 10

AMSC N/A

5962-V075-15

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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-bit bus transceiver with three-state outputs, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03601	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device Type	Generic	Circuit function
01	SN74ACT16245Q-EP	16-Bit Bus Transceiver with three-state outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline Letter	Number of pins	JEDEC PUB 95	Package style
X	48	JEDEC MO-118	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material:
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 7 V
Input voltage range (V_I) ..... -0.5 V to V_{CC} +0.5 V 2/
Output voltage range (V_O) ..... -0.5 V to V_{CC} +0.5 V 2/
Input clamp current (I_{IK}) ($V_I < 0$ V or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current (I_{OK}) ($V_I < 0$ V or $V_I > V_{CC}$) ..... ± 24 mA
Continuous output current (I_O) ($V_O = 0$ V to V_{CC}) ..... ± 24 mA
Continuous current through V_{CC} or GND ..... ± 260 mA
Maximum power dissipation at $T_A = 55^oC$ (in still air) ..... 1.2 W 3/
Storage temperature range, T_{stg} ..... -65^oC to 150^oC

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1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output voltage ratings may be exceeded if the input and output ratings are observed.
3/ The maximum package power dissipation is calculated using a junction temperature of 150^oC and a broad trace length of 750 mils.

1.4 Recommended operating conditions 4/ 5/

Supply voltage range (V_{CC}).	+4.5 V to +5.5 V 6/
Input voltage range (V_{IN})	+0.0 V to V_{CC}
Output voltage range (V_{OUT})	+0.0 V to V_{CC}
Minimum high-level input voltage (V_{IH})	2.0 V
Maximum low level input voltage (V_{IL})	0.8 V
Maximum high level output current (I_{OH})	-16 mA
Maximum low level output current (I_{OL})	16 mA
Input transition rise or fall rate ($\Delta t/\Delta v$)	0 to 10 ns/V
Ambient operating temperature (T_A)	-40°C to 125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4 and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline (s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Block diagram. The block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

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4/ Unused inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater to keep them from floating. Refer to the device manufacturer's application report.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
6/ All V_{CC} and GND pins must be connected to the proper-voltage power supply.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified		V_{CC}	T_A at	Device type	Limits		Unit
							Min	Max	
High level output voltage	V_{OH}	I_{OH} = -50 μA		4.5 V	25°C	01	4.40		V
					-40°C to +125°C		4.40		
				5.5 V	25°C		5.40		
					-40°C to +125°C		5.40		
		I_{OH} = -16 mA		4.5 V	25°C		3.94		
					-40°C to +125°C		3.94		
				5.5 V	25°C		4.94		
					-40°C to +125°C		4.94		
		I_{OH} = -24 mA 2/		5.5 V	-40°C to +125°C		3.85		
Low level output voltage		I_{OL} = 50 μA		4.5 V	25°C			0.10	V
					-40°C to +125°C			0.10	
				5.5 V	25°C			0.10	
					-40°C to +125°C			0.10	
		I_{OL} = 16 mA		4.5 V	25°C			0.36	
					-40°C to +125°C			0.50	
				5.5 V	25°C			0.36	
					-40°C to +125°C			0.50	
		I_{OL} = 24 mA 2/		5.5 V	-40°C to +125°C			0.50	
Input current (Control inputs)	I_I	V_I = V_{CC} or GND		5.5 V	25°C			± 0.10	μA
					-40°C to +125°C			± 1	
Three-state output leakage current (A 0r B ports) 3/	I_{OZ}	V_O = V_{CC} or GND		5.5 V	25°C			± 0.50	μA
					-40°C to +125°C			± 10	
Quiescent supply current	I_{CC}	V_I = V_{CC} or GND , I_O = 0		5.5 V	25°C			8	μA
					-40°C to +125°C			160	
Quiescent supply current delta 4/	ΔI_{CC}	One input at 3.4 V, Other inputs at GND or V_{CC}		5.5 V	25°C			0.9	mA
					-40°C to +125°C			1	
Input capacitance (Control inputs)	C_I	V_I = V_{CC} or GND		5.0 V	25°C		4.5 TYP		pF
Output capacitance (A or B ports)	C_{IO}	V_O = V_{CC} or GND		5.0 V	25°C		16 TYP		pF
Power capacitance per transceiver	C_{PD}	C_L = 50 pF f = 1 MHz	Output enabled	5.0 V	25°C		52 TYP		pF
			Output disabled				10 TYP		

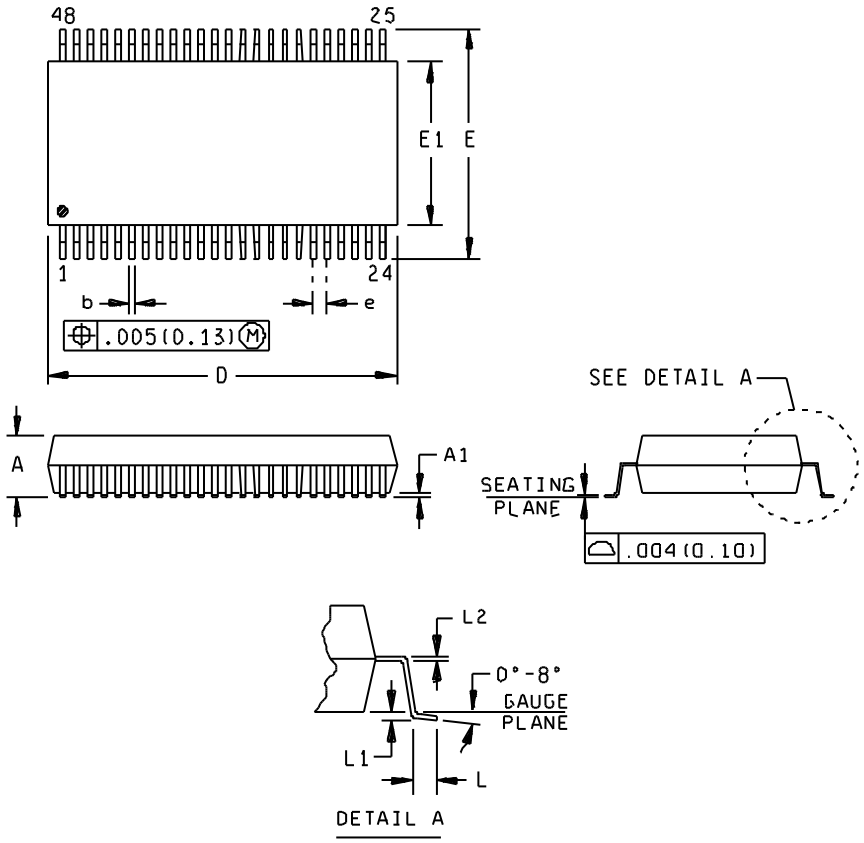
See footnotes at end of table.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified		V_{CC}	T_A at	Device type	Limits		Unit
		From (Input)	To (Output)				Min	Max	
Propagation delay time	t_{PLH}	A or B	B or A	5/	25°C	01	3.2	9.3	ns
					-40°C to +125°C		3.2	11.5	
	t_{PHL}			5/	25°C		2.6	9.2	
					-40°C to +125°C		2.6	11.1	
	t_{PZH}	$\overline{G}$	B or A	5/	25°C		2.7	9.1	
					-40°C to +125°C		2.7	10.9	
	t_{PZL}			5/	25°C		3.4	10.5	
					-40°C to +125°C		3.4	12.6	
	t_{PHZ}	$\overline{G}$	B or A	5/	25°C		5.8	11.6	
					-40°C to +125°C		5.8	13.4	
	t_{PLZ}			5/	25°C		5.5	10.8	
					-40°C to +125°C		5.5	12.7	

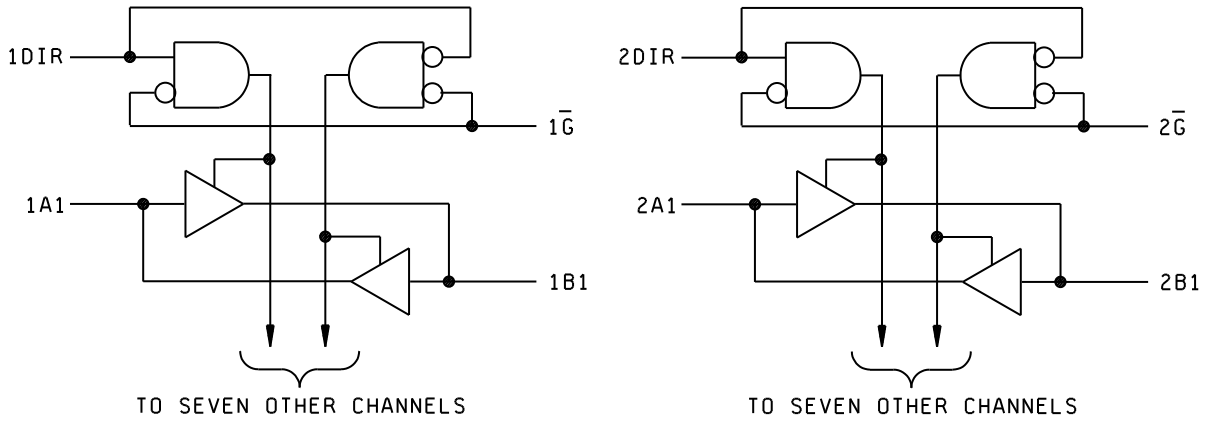
Notes:
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
3/ For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.
4/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
5/ V_{CC} = 4.5 V to 5.5 V

Case X



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		0.110		2.79
A1	0.008		0.20	
b	0.008	0.013	0.20	0.34
D	0.620	0.630	15.75	16.00
E	0.395	0.420	10.03	10.67
E1	0.291	0.299	7.39	7.59
e	0.025 Typ		0.635 Typ	
L	0.020	0.040	0.51	1.02
L1	0.010		0.25	
L2	0.005	0.010	0.13	0.25

FIGURE 1. Case outline.



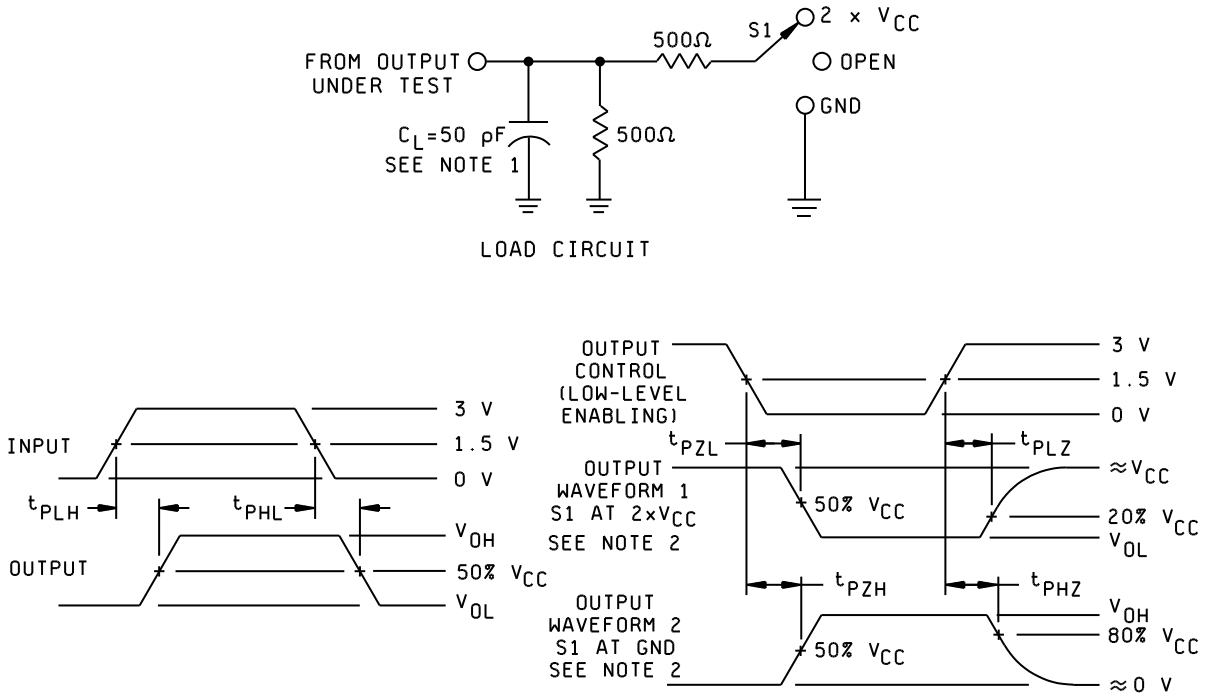
Function table		
Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

L = Low
H = High
X = Don't care

FIGURE 2. Block diagram.

Terminal number	Terminal Symbol	Terminal number	Terminal Symbol
1	1DIR	25	$2\overline{G}$
2	1B1	26	2A8
3	1B2	27	2A7
4	GND	28	GND
5	1B3	29	2A6
6	1B4	30	2A5
7	V_{CC}	31	V_{CC}
8	1B5	32	2A4
9	1B6	33	2A3
10	GND	34	GND
11	1B7	35	2A2
12	1B8	36	2A1
13	2B1	37	1A8
14	2B2	38	1A7
15	GND	39	GND
16	2B3	40	1A6
17	2B4	41	1A5
18	V_{CC}	42	V_{CC}
19	2B5	43	1A4
20	2B6	44	1A3
21	GND	45	GND
22	2B7	46	1A2
23	2B8	47	1A1
24	2DIR	48	$1\overline{G}$

FIGURE 3. Terminal connections.



Test	S1
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	2 x V_{CC}
t_{PHZ} / t_{PZH}	GND

Notes:
1/ CL includes probe and jig capacitance.
2/ Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control
3/ All impulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
4/ The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03601-01XE	01295	SN74ACT16245QDLREP	ACT16245QEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493