REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make change to peak pull-up current test as specified in table I. - ro	00-02-08	R. MONNIN
B	Make changes to paragraph 1.5. Paragraph 4.4.4.3 Dose rate upset testing deleted. Drawing updated to reflect current requirements. – gt	02-08-30	R. MONNIN
C	Add device type 02, case outline X, paragraph 2.2, and Table IB. Delete figure 3, Irradiation exposure circuit and paragraph 4.4.4.2 Dose rate latch up testing. Make correction to Turn on and off input pulse width limits from 700 ns to 70 ns. Delete device class M references.- ro	14-06-16	C. SAFFLE

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C									
SHEET	15	16	17	18	19	20	21	22	23	24	25									

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
RAYMOND MONNIN

DRAWING APPROVAL DATE
00-01-12

REVISION LEVEL
C

MICROCIRCUIT, LINEAR, RADIATION HARDENED, FULL BRIDGE N-CHANNEL FET DRIVER, MONOLITHIC SILICON

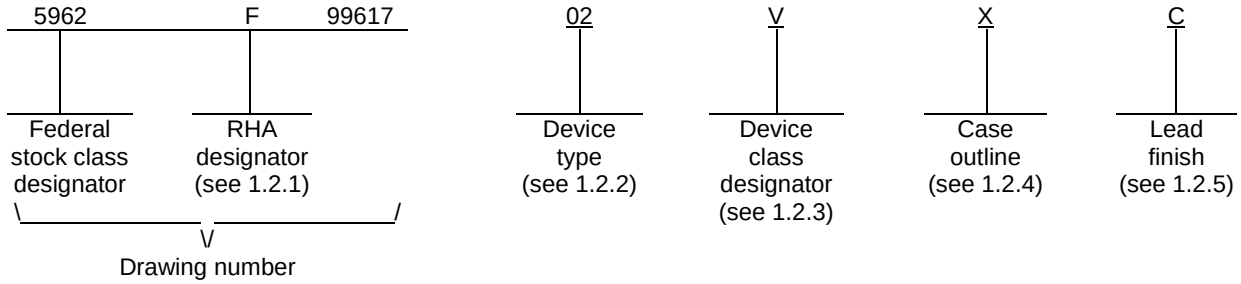
SIZE	CAGE CODE	
A	**67268**	**5962-99617**

SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-4080ARH	Radiation hardened, DI, full bridge N-channel FET driver
02	HS-4080AEH	Radiation hardened, DI, full bridge N-channel FET driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
S	CDFP3-F20	20	Flat pack
X	CDFP4-F20	20	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage (V_{DD} and V_{CC})	-0.3 V to 16 V
Logic I / O voltages	-0.3 V to V_{DD} +0.3 V
Voltage on AHS, BHS	-6.0 V (transient) to 80 V (-55°C to +125°C)
Voltage on ALS, BLS	-2.0 V (transient) to + 2.0 V (transient)
Voltage on AHB, BHB	$V_{AHS, BHS}$ –0.3 V to $V_{AHS, BHS}$ +V_{DD}
Voltage on ALO, BLO	$V_{ALS, BLS}$ –0.3 V to V_{CC} +0.3 V
Voltage on AHO, BHO	$V_{AHS, BHS}$ –0.3 V to $V_{AHB, BHB}$ +0.3 V
Input current, HDEL and LDEL	-5 mA to 0 mA
Maximum power dissipation (P_D) ($T_A \leq +25°C$)	1.8 W
Junction temperature (T_J)	+175°C
Storage temperature range	-55°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	7°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	80°C/W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage (V_{DD} and V_{CC})	+12.0 V to +15.0 V
Voltage on ALS, BLS	-1.0 V to +1.0 V
Voltage on AHB, BHB	$V_{AHS, BHS}$ + 5 V to $V_{AHS, BHS}$ +15 V
Input current, HDEL and LDEL	-500 μA to –50 μA
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):

Device type 01:	
Device classes Q and V	300 krads(Si) 4/
Device class T	100 krads(Si) 4/
Device type 02	300 krads(Si) 5/

Maximum total dose available (dose rate ≤ 0.01 rad(Si)/s):

Device types 02	50 krads(Si) 5/

———

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and ambient temperature range of -55°C to +125°C unless otherwise noted.

4/ Device type 01 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si) for class Q or V and 100 krads(Si) for class T.

5/ Device type 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si), and condition D to a maximum total dose of 50 krads(Si).

1.5 Radiation features – continued.

Single event phenomenon (SEP) :

No single event latch up (SEL) up to effective LET (see 4.4.4.3) ..... ≤ 90.9 MeV/mg/cm^2
No Single event burnout (SEB) occurs at effective LET (see 4.4.4.3) ..... ≤ 90.9 MeV/mg/cm^2
No LOW to HIGH transients on ALO, BLO, AHO and BHO outputs
occur at effective LET (see 4.4.4.3 and table below) ..... ≤ 70 Mev/mg/cm^2 6/

HEN state	Outputs	Input	Output LOW-HIGH transients
HIGH	ALO, BHO	+IN > -IN	None
HIGH	AHO, BLO	-IN > +IN	None
LOW	BHO	+IN > -IN	None
LOW	AHO	-IN > +IN	None

Notes:
1. Samples operated under dynamic conditions.
2. DIS pin is LOW for all tests.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, P.O. Box C700, 100 Bar Harbor Drive, West Conshohocken, PA 19428-2959).

6/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested unless specified by the customer through the purchase order or contract. See manufacturer's SEE test report for more information.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply currents and charge pumps section							
V_{DD} quiescent current	I_{DD}	-IN = 2.5 V, no load, other inputs = 0 V	1,2,3	01,02		13	mA
		M,D,P,L,R,F 2/	1			13	
V_{DD} operating current	I_{DOD}	Outputs switching f = 500 kHz, no load	1,2,3	01,02		15	mA
		M,D,P,L,R,F 2/	1			15	
V_{CC} quiescent current	I_{CC}	-IN = 2.5 V, no load, other inputs = 0 V	1,2,3	01,02		160	µA
		M,D,P,L,R,F 2/	1			160	
V_{CC} operating current	I_{CCO}	f = 500 kHz, no load	1,2,3	01		7	mA
		M,D,P,L,R,F 2/	1			7	
		f = 500 kHz, no load	1,2,3	02		10	
		M,D,P,L,R,F 2/	1			10	
AHB, BHB quiescent current, Q pump output current	I_{AHB}, I_{BHB}	-IN = 2.5 V, no load, other inputs = 0 V, V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12 V	1,2,3	01,02	-15		µA
		M,D,P,L,R,F 2/	1		-15		
AHB, BHB operating current	I_{AHBO}, I_{BHBO}	f = 500 kHz, no load	1,2,3	01,02		5	mA
		M,D,P,L,R,F 2/	1			5	
AHS, BHS, AHB, BHB 3/ leakage current	I_{HLK}	V_{AHS} = V_{BHS} = 95 V, V_{AHB} = V_{BHB} = 95 V	1,2,3	01,02		1	µA
		M,D,P,L,R,F 2/	1			1	
AHB - AHS, BHB - BHS Q pump output voltage	V_{AHB} - V_{AHS}, V_{BHB} - V_{BHS}	No load	1,2,3	01,02	11.3	13.3	V
		M,D,P,L,R,F 2/	1		11.3	13.3	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input comparator pins: +INPUT, -INPUT, OUTPUT section							
Offset voltage	V_{OS}	Over common mode voltage range	1,2,3	01,02	-15	+15	mV
		M,D,P,L,R,F 2/	1		-15	+15	
Input bias current	I_{IB}		1,2,3	01,02	0	2	µA
		M,D,P,L,R,F 2/	1		0	3	
Input offset current	I_{OS}		1,2,3	01,02	-2	+2	µA
		M,D,P,L,R,F 2/	1		-2	+2	
Input common mode voltage range	CMVR		1,2,3	01,02	1	4.50	V
		M,D,P,L,R,F 2/	1		1	4.50	
OUTPUT high level output voltage	V_{OH}	+IN > -IN, I_{OH} = -250 µA	1,2,3	01,02	V_{DD} –0.4 V		V
		M,D,P,L,R,F 2/	1		V_{DD} –0.4 V		
OUTPUT low level output voltage	V_{OL}	+IN < -IN, I_{OL} = 250 µA	1,2,3	01,02		0.4	V
		M,D,P,L,R,F 2/	1			0.4	
High level output current	I_{OH}	V_{OUT} = 6 V	1,2,3	01,02		-1.5	mA
		M,D,P,L,R,F 2/	1			-1.5	
Low level output current	I_{OL}	V_{OUT} = 6 V	1,2,3	01,02	2.5		mA
		M,D,P,L,R,F 2/	1		2.5		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
INPUT pins: DIS section								
Low level input voltage	V_{IL}			1,2,3	01,02		0.8	V
			M,D,P,L,R,F 2/	1			0.8	
High level input voltage	V_{IH}			1,2,3	01,02	3.0		V
			M,D,P,L,R,F 2/	1		3.0		
Low level input current	I_{IL}	V_{IN} = 0 V		1,2,3	01,02	-160		µA
			M,D,P,L,R,F 2/	1		-160		
High level input current	I_{IH}	V_{IN} = 5 V		1,2,3	01,02	-150		µA
			M,D,P,L,R,F 2/	1		-150		
INPUT pins: HEN section								
Low level input voltage	V_{IL}			1,2,3	01,02		0.8	V
			M,D,P,L,R,F 2/	1			0.8	
High level input voltage	V_{IH}			1,2,3	01,02	3.0		V
			M,D,P,L,R,F 2/	1		3.0		
Low level input current	I_{IL}	V_{IN} = 0 V		1,2,3	01,02	-160		µA
			M,D,P,L,R,F 2/	1		-160		
High level input current	I_{IH}	V_{IN} = 5 V		1,2,3	01,02	-150		µA
			M,D,P,L,R,F 2/	1		-150		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Turn-on delay pins: LDEL and HDEL section							
LDEL, HDEL voltage	V_{HDEL}, V_{LDEL}	$I_{HDEL} = I_{LDEL} = -100\ \mu A$	1,2,3	01,02	5.0	5.5	V
		M,D,P,L,R,F 2/	1		5.0	5.5	
Gate driver output pins; ALO, BLO AHO, and BHO section							
Low level output voltage	V_{OL}	$I_{OUT} = 100$ mA	1,2,3	01,02		1.4	V
		M,D,P,L,R,F 2/	1			1.4	
High level output voltage	V_{CC} - V_{OH}	$I_{OUT} = -100$ mA	1,2,3	01,02		1.6	V
		M,D,P,L,R,F 2/	1			1.6	
Peak pull-up current	$+I_O$	$V_{OUT} = 0$ V	1,2,3	01,02	0.4		A
		M,D,P,L,R,F 2/	1		0.4		
Peak pull-down current	$-I_O$	$V_{OUT} = 12$ V	1,2,3	01,02	0.4		A
		M,D,P,L,R,F 2/	1		0.4		
Under voltage, rising threshold	+UV		1,2,3	01,02	8.0	10.0	V
		M,D,P,L,R,F 2/	1		8.0	10.0	
Under voltage, falling threshold	-UV		1,2,3	01,02	7.5	9.5	V
		M,D,P,L,R,F 2/	1		7.5	9.5	
Under voltage, hystersis	HYS		1,2,3	01,02	0.5	0.9	V
		M,D,P,L,R,F 2/	1		0.5	0.9	
Switching section							
Lower turn-off propagation delay (+IN / -IN to ALO)	t_{LPHL}	4/	9,10,11	01,02		450	ns
		M,D,P,L,R,F 2/	9			450	
Upper turn-off propagation delay (+IN / -IN to AHO)	t_{LPHL}	4/	9,10,11	01,02		1200	ns
		M,D,P,L,R,F 2/	9			1200	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switching section – Continued.							
Lower turn-off propagation delay (+IN / -IN to BLO)	t_{LPHL}	4/	9,10,11	01,02		1200	ns
		M,D,P,L,R,F 2/	9			1200	
Upper turn-off propagation delay (+IN / -IN to BHO)	t_{LPHL}	4/	9,10,11	01,02		500	ns
		M,D,P,L,R,F 2/	9			500	
Lower turn-on propagation delay (+IN / -IN to BLO)	t_{LPLH}	4/	9,10,11	01,02		650	ns
		M,D,P,L,R,F 2/	9			650	
Lower turn-on propagation delay (+IN / -IN to BHO)	t_{HPLH}	4/	9,10,11	01,02		1200	ns
		M,D,P,L,R,F 2/	9			1200	
Lower turn-on propagation delay (+IN / -IN to ALO)	t_{LPLH}	4/	9,10,11	01,02		1200	ns
		M,D,P,L,R,F 2/	9			1200	
Upper turn-on propagation delay (+IN / -IN to AHO)	t_{HPLH}	4/	9,10,11	01,02		600	ns
		M,D,P,L,R,F 2/	9			600	
Rise time	t_R	4/	9,10,11	01,02		65	ns
		M,D,P,L,R,F 2/	9			65	
Fall time	t_F	4/	9,10,11	01,02		60	ns
		M,D,P,L,R,F 2/	9			60	
Turn-on input pulse width	$t_{PWIN-ON}$	4/	9,10,11	01,02	70		ns
		M,D,P,L,R,F 2/	9		70		
Turn-off input pulse width	$t_{PWIN-OFF}$	4/	9,10,11	01,02	70		ns
		M,D,P,L,R,F 2/	9		70		
Disable turn-off propagation delay (DIS – lower outputs)	t_{DISLOW}	4/	9,10,11	01,02		500	ns
		M,D,P,L,R,F 2/	9			500	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switching section – Continued.							
Disable turn-off propagation delay (DIS – upper outputs)	$t_{DISHIGH}$	4/	9,10,11	01,02		450	ns
		M,D,P,L,R,F 2/	9			450	
Disable to lower turn-on propagation delay (DIS – ALO and BLO)	t_{DLPHL}	4/	9,10,11	01,02		750	ns
		M,D,P,L,R,F 2/	9			750	
Refresh pulse width (ALO and BLO)	t_{REF-PW}	4/	9,10,11	01,02		450	ns
		M,D,P,L,R,F 2/	9			450	
Disable to upper enable (DIS – AHO and BHO)	t_{UEN}	4/	9,10,11	01,02		1250	ns
		M,D,P,L,R,F 2/	9			1250	
HEN-AHO, BHO turn-off, propagation delay	$t_{HEN-PHL}$	4/	9,10,11	01,02		450	ns
		M,D,P,L,R,F 2/	9			450	
HEN-AHO, BHO turn-on, propagation delay	$t_{HEN-PLH}$	4/	9,10,11	01,02		500	ns
		M,D,P,L,R,F 2/	9			500	

1/ Unless otherwise specified, $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12$ V and $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0$ V.

2/ RHA device type 01 supplied to this drawing will meet all levels M, D, P, L, R and F of irradiation for device class Q or V and levels M, D, P, L, and R of irradiation for device class T. However, device type 01 is only tested at the "F" level for device class Q or V and the "R" level for device class T in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein).

RHA device type 02 supplied to this drawing will meet all levels M, D, P, L, R, and F of irradiation for condition A and irradiation of M, D, P, and L levels for condition D. However, device type 02 is only tested at the "F" level in accordance with MIL-STD-883, method 1019, condition A, and tested at the "L" level in condition D (see 1.5 herein).

Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

3/ The I_{HLK} test, measures the leakage current through the high side output drivers when those drivers are biased at 95 V and disabled with 0 V across them.

4/ $R_{HDEL} = R_{LDEL} = 10\ k\Omega$ and $C_L = 1000$ pF.

TABLE IB. SEP test limits. 1/ 2/

Device type	SEP	Temperature (T_A)	V_{DD}	Effective linear energy transfer (LET)
01	No SEL	125°C	20 V	≤ 90.9 MeV/mg/cm^2
	No SEB	125°C	20 V	≤ 90.9 MeV/mg/cm^2
	No SET 3/	25°C	20 V	≤ 70 MeV/mg/cm^2

1/ For single event phenomena (SEP) test conditions, see 4.4.4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by technical review board and qualifying activity.

3/ No LOW to HIGH transients on ALO, BLO, AHO and BHO outputs occur at effective LET ≤ 70 MeV/mg/cm^2 (see 4.4.4.3 and table below, see manufacturer's SEE test report for more information)

HEN state	Outputs	Input	Output LOW-HIGH transients
HIGH	ALO, BHO	IN+ > IN-	None
HIGH	AHO, BLO	IN- > IN+	None
LOW	BHO	IN+ > IN-	None
LOW	AHO	IN- > IN+	None

Notes:
1. Samples operated under dynamic conditions.
2. DIS pin is LOW for all tests.

Device types	01 and 02
Case outlines	S and X
Terminal number	Terminal symbol
1	BHB
2	HEN
3	DIS
4	V_{SS}
5	OUT
6	+IN
7	-IN
8	HDEL
9	LDEL
10	AHB
11	AHO
12	AHS
13	ALO
14	ALS
15	V_{CC}
16	V_{DD}
17	BLS
18	BLO
19	BHS
20	BHO

FIGURE 1. Terminal connections.

PIN number	SYMBOL	DESCRIPTION
1	BHB	B high-side bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 15 μA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 15.0 V maximum.
2	HEN	High-side enable input. Logic level input that when low overrides +IN/-IN. (Pins 6 and 7) to put AHO and BHO drivers (pins 11 and 20) in low output state. When HEN is high AHO and BHO are controlled by +IN/-IN inputs. The pin can be driven by signal levels of 0 V to 15 V (no greater than V_{DD}). An internal 100 μA pull-up to V_{DD} will hold HEN high , so no connection is required if high-side and low-side outputs are to be controlled by +IN/-IN inputs.
3	DIS	Disable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0 V to 15 V (no greater than V_{DD}). An internal 100 μA pull-up to V_{DD} will hold DIS high if this pin is not driven.
4	V_{SS}	Chip negative supply, generally will be ground.
5	OUT	Output of the input control comparator. This output can be used for feedback and hysteresis.
6	+IN	Noninverting input of control comparator. This pin can only be driven by signal levels of 0 V to 4.5 V. If +IN is greater than –IN (pin 7), than ALO and BHO are low level outputs and BLO and AHO are high level outputs. If +IN is less than –IN than ALO and BHO are high level outputs and BLO and AHO are low level outputs. DIS (pin 3) high level will override +IN/-IN control for all outputs. HEN (pin 2) low level will override +IN/-IN control of AHO and BHO. When switching in four quadrant mode, dead time in a half bridge leg is controlled by HDEL and LDEL (pins 8 and 9).
7	-IN	Inverting input of control comparator. This pin can only be driven by signal levels of 0 V to 4.5 V. See +IN (pin 6) description.
8	HDEL	High-side turn-on delay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.2 V.
9	LDEL	Low-side turn-on delay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low- side drivers. LDEL reference voltage is approximately 5.2 V.

FIGURE 1. Terminal connections – Continued.

PIN number	SYMBOL	DESCRIPTION
10	AHB	A high-side bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 15 μA out of this pin to maintain bootstrap supply. Internal circuitry clamps the supply to approximately 15.0 V.
11	AHO	A high-side output. Connect to gate of A high-side power MOSFET.
12	AHS	A high-side source connection. Connect to source of A high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A low-side output. Connect to gate of A low-side power MOSFET.
14	ALS	A low-side source connection. Connection to source of A low-side power MOSFET.
15	V_{CC}	Positive supply to gate drivers. Must be same potential as V_{DD} (pin 16). Connect to anode of two bootstrap diodes.
16	V_{DD}	Positive supply to lower gate drivers. Must be same potential as V_{CC} (pin 15). De-couple this pin to V_{SS} (pin 4).
17	BLS	B low-side. Source connection. Connect to source of B low-side power MOSFET.
18	BLO	B low-side output. Connect to gate of B low-side power MOSFET.
19	BHS	B high-side source connection. Connect to source of B high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	BHO	B high-side output. Connect to gate of B high-side power MOSFET.

FIGURE 1. Terminal connections – Continued.

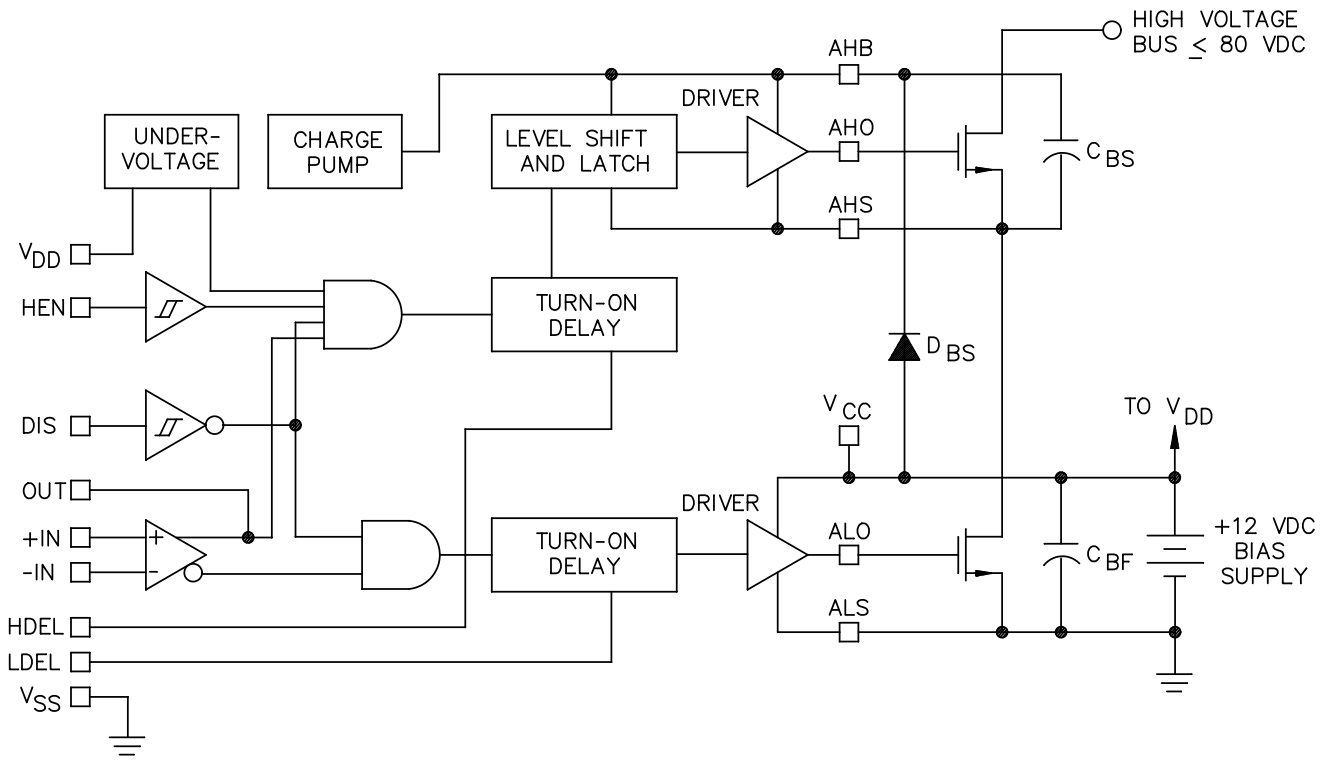


FIGURE 2. Logic diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1	1	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,9, 1/ 10,11	1,2,3, 2/ 3/ 9,10,11	As specified in QM plan
Group A test requirements (see 4.4)	1,2,3,9,10,11	1,2,3,9,10,11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1,2,3,9,10,11	1,2,3,9, 3/ 10,11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1	1	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1,9	1,9	As specified in QM plan

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 9, and Δ's.
3/ Delta limits as specified in table IIB herein shall be required where specified, and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test, Delta parameters (+25°C).

Parameters 1/	Delta limits
V_{DD} quiescent current (I_{DD})	±300 μA
AHS, BHS, AHB, BHB leakage current (I_{HLK})	±100 nA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01 and 02. In addition, for device type 02 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.2.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. Test four devices with zero failures.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b. Occurance of latchups (SEL).

c. Number of burnouts (SEB).

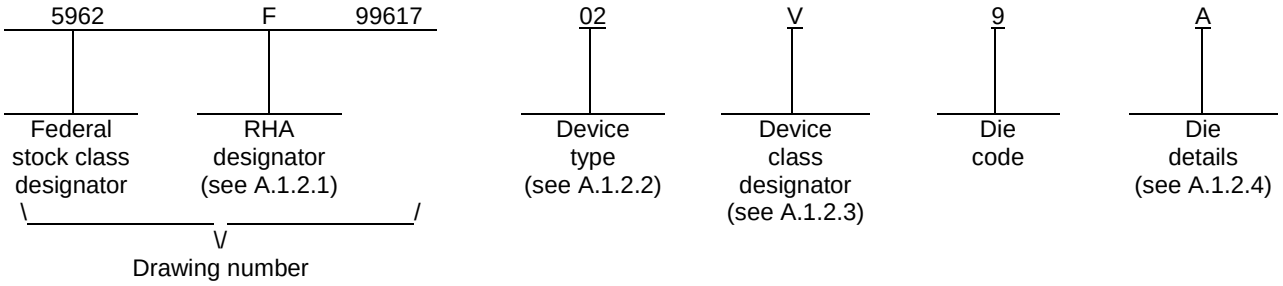
d. Number of transients (SET).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99617

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-4080ARH	Radiation hardened DI full bridge N-channel FET driver
02	HS-4080AEH	Radiation hardened, DI, full bridge N-channel FET driver

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.2.1, and 4.4.4.3 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

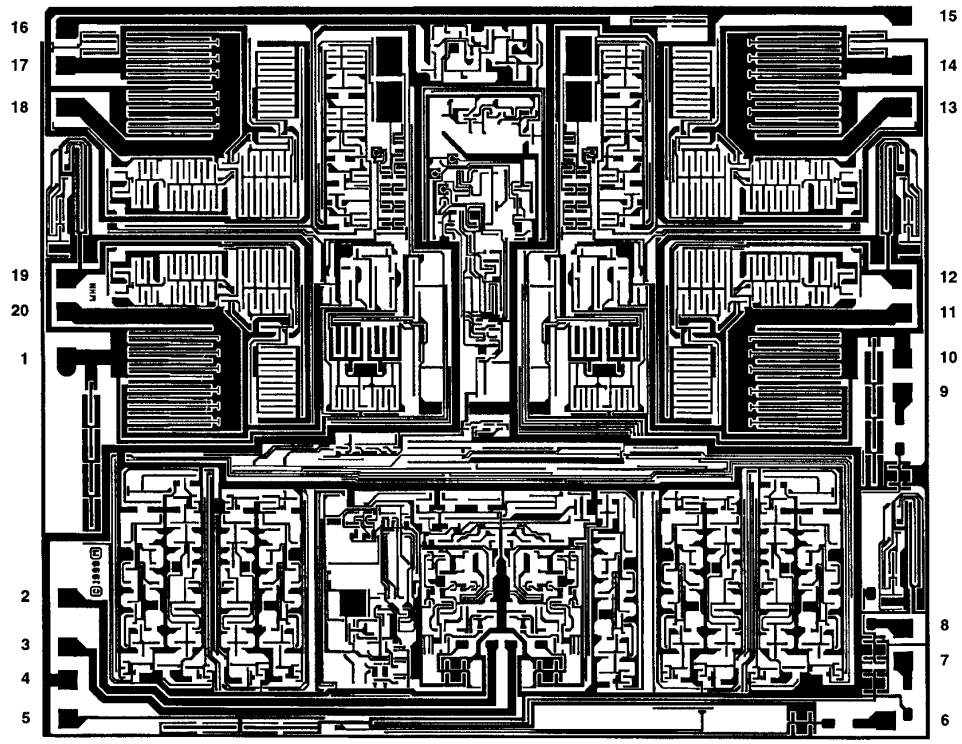
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



Die bonding pad locations and electrical functions

NOTE: Pad numbers reflect terminal numbers when placed in case outlines S and X (see figure 1).

Die physical dimensions.
Die size: 4760 microns X 5660 microns.
Die thickness: 19 ± 1 mils.

Interface materials.
Top metallization: Al Si Cu 16.0 kÅ ± 2.0 kÅ
Backside metallization: Silicon.

Glassivation.
Type: Phosphorus silicon glass (PSG)
Thickness: 8.0 kÅ ± 1.0 kÅ.

Substrate: Radiation hardened silicon gate, Dielectrically Isolated (DI).

Assembly related information.
Substrate potential: Unbiased.
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-06-16

Approved sources of supply for SMD 5962-99617 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9961701QSC	3/	HS9-4080ARH-8
5962R9961701TSC	3/	HS9-4080ARH-T
5962F9961701VSC	3/	HS9-4080ARH-Q
5962F9961701V9A	3/	HS0-4080ARH-Q
5962F9961702VXC	34371	HS9-4080AEH-Q
5962F9961702V9A	34371	HS0-4080AEH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803