| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Drawing updated to reflect current requirements. – gt | 02-06-20 | R. Monnin |
| B | Changes to paragraph 1.4, table I, and figure 3. - gt | 02-09-06 | R. Monnin |
| C | Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw | 15-02-19 | Charles F. Saffle |
| D | Update paragraphs to current MIL-PRF-38535 requirements. - drw | 20-09-03 | James R. Eschmeyer |

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | |
| REV | D | D | D | D | D | D | D | D | D | D | D | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | | | | | | | | |

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV STATUS | REV | D | D | D | D | D | D | D | D | D | D | D | D | D | D |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
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**DLA LAND AND MARITIME**
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**https://www.dla.mil/LandandMaritime**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
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APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
99-12-16

REVISION LEVEL
D

MICROCIRCUIT, DIGITAL-LINEAR, 12-BIT, 8-CHANNEL, SERIAL A/D CONVERTER, MONOLITHIC SILICON

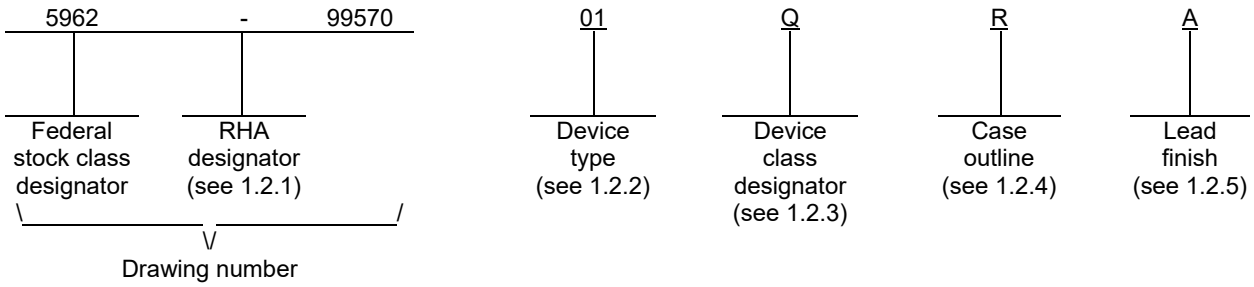
| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-99570** |

SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | TLV2548 | 12-Bit, 8-Channel, Serial A/D converter |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| R | GDIP1-T20 or CDIP2-T20 | 20 | Dual-in-line |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range, GND to $V_{CC}$ ..... -0.3 V to 6.5 V
Analog input voltage range ..... -0.3 V to $V_{CC}$ + 0.3 V
Reference input voltage ..... $V_{CC}$ + 0.3 V
Digital input voltage range ..... -0.3 V to $V_{CC}$ + 0.3 V
Maximum power dissipation, $P_D$ ($T_A \leq 25°C$):
  Case R ..... 1894 mW 2/
  Case 2 ..... 1375 mW 2/
Operating junction temperature range, $T_J$ ..... -55°C to 150°C
Storage temperature range ..... -65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Case R, derate at 15.2 mW/°C for $T_A > 25°C$. Case 2, derate at 11.0 mW/°C for $T_A > 25°C$.

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage, $V_{CC}$ | 3.0 V min to 5.5 V max |
| Positive external reference voltage input, $V_{REFP}$ | 2 V min to $V_{CC}$ max 3/ |
| Negative external reference voltage input, $V_{REFM}$ | 0 V min to 2 V max 3/ |
| Differential reference voltage input, $V_{REFP}$ - $V_{REFM}$ | 2 V min to $V_{CC}$ max 3/ |
| Analog input voltage | 0 V min to $V_{CC}$ max 3/ |
| High level control input voltage, $V_{IH}$ | 2.1 V min |
| Low level control input voltage, $V_{IL}$ | 0.6 V max |
| Setup time, CS falling edge before SCLK rising edge (FS = 1) or before SCLK falling edge (when FS is active), $t_{su(CS-SCLK)}$ | |
| $V_{CC}$ = 4.5 V | 20 ns min |
| $V_{CC}$ = 3.0 V | 30 ns min |
| Hold time, CS rising edge after SCLK rising edge (FS = 1) or after SCLK falling edge (when FS is active), $t_{h(SCLK-CS)}$ | |
| $V_{CC}$ = 4.5 V | 10 ns min |
| $V_{CC}$ = 3.0 V | 15 ns min |
| Delay time, delay from CS falling edge to FS rising edge, $t_{d(CSL-FSH)}$ | 0.5 SCLK min |
| Delay time, delay time from 16th SCLK falling edge to CS rising edge (FS = 1), $t_{d(SCLK16L-CSH)}$ | 0.5 SCLK min |
| Setup time, FS rising edge before SCLK falling edge, $t_{su(FSH-SCLKL)}$ | 20 ns min |
| Hold time, FS hold high after SCLK falling edge, $t_{h(FSH-SCLKL)}$ | 30 ns min to 37 ns max |
| Pulse width, CS high time, $t_{wH(CS)}$ | 100 ns min |
| SCLK cycle time, $V_{CC}$ = 3.0 V to 3.6 V, $t_{c(SCLK)}$ | 67 ns min |
| SCLK cycle time, $V_{CC}$ = 4.5 V to 5.5 V, $t_{c(SCLK)}$ | 50 ns min |
| Pulse width, SCLK low time, $t_{wL(SCLK)}$ | |
| $V_{CC}$ = 4.5 V | 22 ns min |
| $V_{CC}$ = 3.0 V | 27 ns min |
| Pulse width, SCLK high time, $t_{wH(SCLK)}$ | |
| $V_{CC}$ = 4.5 V | 22 ns min |
| $V_{CC}$ = 3.0 V | 27 ns min |
| Setup time, SDI valid before falling edge of SCLK (FS is active) or the rising edge of SCLK (FS = 1), $t_{su(DI-SCLK)}$ | 25 ns min |
| Hold time, SDI hold valid after falling edge of SCLK (FS is active) or the rising edge of SCLK (FS = 1), $t_{h(DI-SCLK)}$ | 5 ns min |
| Delay time, delay from CS falling edge to SDO valid, $t_{d(CSL-DOV)}$ | 25 ns max |
| Delay time, delay from FS falling edge to SDO valid, $t_{d(FSL-DOV)}$ | 25 ns max |
| Delay time, delay from SCLK falling edge (FS is active) or SCLK rising edge (FS = 1) to SDO valid, $t_{d(SCLK-DOV)}$ | |
| $V_{CC}$ = 5.5 V, SDO = 60 pF | 0.5 times SCLK + 24 ns max |
| $V_{CC}$ = 3.3 V, SDO = 60 pF | 0.5 times SCLK + 33 ns max |
| Delay time, delay from 16th SCLK falling edge to INT falling edge (FS = 1) or from the 17th rising edge SCLK to INT falling edge (when FS active), $t_{d(SCLK-INTL)}$ | Min $t_{(conv)}$ |
| Delay time, delay from CS falling edge to INT rising edge, $t_{d(CSL-INTH)}$ | 50 ns max |
| Delay time, delay from CS rising edge to CSTART falling edge, $t_{d(CSH-CSTARTL)}$ | 100 ns min |
| Delay time, delay from CSTART rising edge to EOC falling edge, $t_{d(CSTARTH-EOCL)}$ | 50 ns max |
| Pulse width, CSTART low time, $t_{wL(CSTART)}$ | Min $t_{(sample)}$ |
| Delay time, delay from CSTART rising edge to CSTART falling edge, $t_{d(CSTARTH-CSTARTL)}$ | $t_{(conv)}$ max |
| Ambient operating temperature range, $T_A$ | -55°C ≤ $T_A$ ≤ 125°C |

3/ When binary output format is used, analog input voltages greater than that applied to REFP convert as all ones (111111111111), while input voltages less than that applied to REFM convert as all zeros (000000000000). The device is functional with reference down to 2 V ($V_{REFP}$ – $V_{REFM}$ – 1); however, the electrical specifications are no longer applicable.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| High level output voltage | $V_{OH}$ | $V_{CC}$ = 5.5 V, $I_{OH}$ = -0.2 mA at 30 pF load | 1, 2, 3 | 01 | 2.4 | | V |
| | | $V_{CC}$ = 3.0 V, $I_{OH}$ = -20 µA at 30 pF load | | | $V_{CC}$ – 0.2 | | |
| Low level output voltage | $V_{OL}$ | $V_{CC}$ = 5.5 V, $I_{OL}$ = 0.8 mA at 30 pF load | 1, 2, 3 | 01 | | 0.4 | V |
| | | $V_{CC}$ = 3.0 V, $I_{OL}$ = 20 µA at 30 pF load | | | | 0.1 | |
| Off state output current (high impedance state) | $I_{OZ}$ | $V_{OUT}$ = $V_{CC}$, $\overline{CS}$ = $V_{CC}$ | 1, 2, 3 | 01 | | 2.5 | µA |
| | | $V_{OUT}$ = 0 V, $\overline{CS}$ = $V_{CC}$ | | | -2.5 | | |
| High level input current | $I_{IH}$ | $V_{IN}$ = $V_{CC}$ | 1, 2, 3 | 01 | | 2.5 | µA |
| Low level input current | $I_{IL}$ | $V_{IN}$ = 0 V | 1, 2, 3 | 01 | | 2.5 | µA |
| Operating supply current, normal sampling (short) | $I_{CC}$ | $\overline{CS}$ at 0 V, External reference, $V_{CC}$ = 4.5 V to 5.5 V | 1, 2, 3 | 01 | | 2.0 | mA |
| | | $\overline{CS}$ at 0 V, External reference, $V_{CC}$ = 3.0 V to 3.3 V | | | | 1.0 | mA |
| | | $\overline{CS}$ at 0 V, Internal reference, $V_{CC}$ = 4.5 V to 5.5 V | | | | 2.4 | mA |
| | | $\overline{CS}$ at 0 V, Internal reference, $V_{CC}$ = 3.0 V to 3.3 V | | | | 1.7 | mA |
| Internal reference supply current | | $\overline{CS}$ at 0 V, $V_{CC}$ = 4.5 V to 5.5 V | 1, 2, 3 | 01 | | 1.0 | mA |
| | | $V_{CC}$ = 3.0 V to 3.3 V | | | | 0.7 | |
| Power down supply current 2/ | $I_{CC(PD)}$ | For all digital inputs, $0 V \le V_{IN} \le 0.3 V$ or $V_{IN} \ge V_{CC} – 0.3 V$, SCLK = 0, $V_{CC}$ = 4.5 V to 5.5 V, External clock | 1, 2, 3 | 01 | | 1.5 | mA |
| | | $V_{CC}$ = 3.0 V to 3.3 V, External clock | | | | 1.5 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Auto power down current 2/ | $I_{CC(AUTOPWDN)}$ | For all digital inputs, $0 V \le V_{IN} \le 0.3 V$ or $V_{IN} \ge V_{CC} - 0.3 V$, SCLK = 0, $V_{CC}$ = 4.5 V to 5.5 V, External clock, External reference | 1, 2, 3 | 01 | | 2.5 | mA |
| | | $V_{CC}$ = 3.0 V to 3.3 V, External reference, External clock | | | | 2.5 | |
| Selected channel leakage current | | Selected channel at $V_{CC}$ | 1, 2, 3 | 01 | | 2.5 | µA |
| | | Selected channel at 0 V | | | | 2.5 | |
| Maximum static analog reference current into REFP (use external reference, | | $V_{REFP} = V_{CC}$ 5.5 V, $V_{REFM}$ = GND | 1, 2, 3 | 01 | | 20 | µA |
| Input capacitance | $C_{IN}$ | Analog inputs, See 4.4.1c 2/ | 1, 2, 3 | 01 | | 50 | pF |
| | | Control inputs, See 4.4.1c 2/ | | | | 25 | |
| Input MUX ON resistance | $Z_{IN}$ | $V_{CC}$ = 5.5 V 2/ | 1, 2, 3 | 01 | | 500 | Ω |
| | | $V_{CC}$ = 3.0 V 2/ | | | | 600 | |
| Signal-to-noise ratio +distortion | SINAD | $f_{IN}$ = 12 kHz at 200 KSPS | 4, 5, 6 | 01 | 65 | | dB |
| Total harmonic distortion | THD | $f_{IN}$ = 12 kHz at 200 KSPS | 4, 5 | 01 | | -75 | dB |
| | | | 6 | | | -73 | dB |
| Spurious free dynamic range | SFDR | $f_{IN}$ = 12 kHz at 200 KSPS | 4, 5, 6 | 01 | | -75 | dB |
| Reference input voltage | REFP | $V_{CC}$ = 3.0 V to 5.5 V 3/ | 1, 2, 3 | 01 | | $V_{CC}$ | V |
| Input impedance | | $V_{CC}$ = 5.5 V, CS = 1, 2/, 3/ SCLK = 0, (off) | 1, 2, 3 | 01 | 100 | | MΩ |
| | | $V_{CC}$ = 5.5 V, CS = 0, 2/, 3/ SCLK = 20 MHz, (on) | | | 20 | | kΩ |
| | | $V_{CC}$ = 3.0 V, CS = 1, 2/, 3/ SCLK = 0, (off) | | | 100 | | MΩ |
| | | $V_{CC}$ = 3.0 V, CS = 0, 2/, 3/ SCLK = 20 MHz, (on) | | | 20 | | kΩ |
| Input voltage difference | REFP – REFM | $V_{CC}$ = 3.0 V to 5.5 V 3/ | 1, 2, 3 | 01 | 2 | $V_{CC}$ | V |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Internal reference voltage | REFP – REFM | $V_{CC}$ = 5.5 V, 3/ VREFSELECT = 4 V | 1, 2, 3 | 01 | 3.85 | 4.15 | V |
| | | $V_{CC}$ = 5.5 V, 3/ VREFSELECT = 2 V | | | 1.925 | 2.075 | |
| | | $V_{CC}$ = 3.0 V, 3/ VREFSELECT = 2 V | | | 1.925 | 2.075 | |
| Reference temperature coefficient | | $V_{CC}$ = 3.0 V to 5.5 V 2/, 3/ | 1, 2, 3 | 01 | | 40 | ppm/°C |
| Integral linearity error | $E_L$ | 4/, 5/ | 1, 2, 3 | 01 | | ±1.2 | LSB |
| Differential linearity error | $E_D$ | 4/, 6/ | 1, 2, 3 | 01 | | ±1 | LSB |
| Offset error | $E_O$ | 4/, 6/, 7/ | 1, 2 | 01 | -4 | +6 | LSB |
| | | | 3 | | -4 | +6.2 | |
| Full scale error | $E_{FS}$ | 4/, 7/ | 1, 2 | 01 | -4 | +6 | LSB |
| | | | 3 | | -4 | +7.6 | |
| Conversion time | $t_{CONV}$ | Internal OSC, 4/ OSC = 3 MHz to 6 MHz, See figure 3 | 9, 10, 11 | 01 | | 4.65 | µs |
| Sampling time | $t_{SAMPLE}$ | At 1 kΩ, 4/ See figure 3 | 9, 10, 11 | 01 | 600 | | ns |
| Transition time for EOC, $\overline{INT}$ | $t_{t(I/O)}$ | See figure 3 2/, 4/ | 9, 10, 11 | 01 | | 50 | ns |
| Transition time for SDI, SDO | $t_{t(CLK)}$ | See figure 3 2/, 4/ | 9, 10, 11 | 01 | | 25 | ns |

1/ $V_{CC}$ = $V_{REFP}$ = 3.0 V to 5.5 V, SCLK frequency = 20 MHz at 5 V, 15 MHz at 3 V unless otherwise specified.

2/ Not production tested.

3/ 0.1 µF and 10 µF between REFP and REFM pins.

4/ $V_{CC}$ = $V_{REFP}$ = 3.0 V to 5.5 V, SCLK frequency = 20 MHz.

5/ Linear error is the maximum deviation from the best straight line through the A/D transfer characteristics.

6/ Analog input voltages greater than that applied to REFP convert as all ones (111111111111), while input voltages less than that applied to REFM convert as all zeros (0000000000). The device is functional with reference down to 2 V (VREFP – VREFM); however, the electrical specifications are no longer applicable.

7/ Zero error is the difference between 000000000000 and the converted output for zero input voltage: full scale error is the difference between 111111111111 and the converted output for full-scale input voltage.

| Device type | 01 |
|---|---|
| Case outline | R and 2 |
| Terminal number | Terminal symbol |
| 1 | SDO |
| 2 | SDI |
| 3 | SCLK |
| 4 | EOC/($\overline{\text{INT}}$) |
| 5 | $V_{CC}$ |
| 6 | A0 |
| 7 | A1 |
| 8 | A2 |
| 9 | A3 |
| 10 | A4 |
| 11 | A5 |
| 12 | A6 |
| 13 | A7 |
| 14 | $\overline{\text{CSTART}}$ |
| 15 | GND |
| 16 | $\overline{\text{PWDN}}$ |
| 17 | FS |
| 18 | REFM |
| 19 | REFP |
| 20 | $\overline{\text{CS}}$ |

FIGURE 1. Terminal connections.

| Terminal symbol | Terminal number | I/O | Description |
|---|---|---|---|
| A0<br>A1<br>A2<br>A3<br>A4<br>A5<br>A6<br>A7 | 6<br>7<br>8<br>9<br>10<br>11<br>12<br>13 | I | Analog signal inputs. The analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 kΩ. For a source impedance greater than 1 kΩ, use the asynchronous conversion start signal $\overline{\text{CSTART}}$ ($\overline{\text{CSTART}}$ low time controls the sampling period) or program long sampling period to increase the sampling time. |
| $\overline{\text{CS}}$ | 20 | I | Chip select. A high-to-low transition on the $\overline{\text{CS}}$ input resets the internal 4-bit counter, enables SDI, and removes SDO from 3-state within a maximum setup time. SDI is disabled within a setup time after the 4-bit counter counts to 16 (clock edges) or a low-to-high transition of $\overline{\text{CS}}$ whichever happens first. SDO is 3-stated after the rising edge of $\overline{\text{CS}}$. $\overline{\text{CS}}$ can be used as the FS pin when a dedicated serial port is used. |
| $\overline{\text{CSTART}}$ | 14 | I | This terminal controls the start of sampling of the analog input from a selected multiplex channel. A high-to-low transition starts sampling of the analog input signal. A low-to-high transition puts the S/H in hold mode and starts the conversion. This input is independent from SCLK and works when $\overline{\text{CS}}$ is high (inactive). The low time of $\overline{\text{CSTART}}$ controls the duration of the sampling period of the converter (extended sampling). Tie this terminal to $V_{CC}$ if not used. |
| EOC/($\overline{\text{INT}}$) | 4 | O | End of conversion or interrupt to host processor.<br>Programmed as EOC: This output goes from a high-to-low logic level at the end of the sampling period and remains low until the conversion is complete and data are ready for transfer. EOC is used in conversion mode 00 only.<br>Programmed as $\overline{\text{INT}}$ : This pin can also be programmed as an interrupt output signal to the host processor. The falling edge of $\overline{\text{INT}}$ indicates data are ready for output. The following $\overline{\text{CS}}\downarrow$ or $\overline{\text{FS}}\uparrow$ clears $\overline{\text{INT}}$. The falling edge of $\overline{\text{INT}}$ puts SDO back to 3-state even if $\overline{\text{CS}}$ is still active. |
| FS | 17 | I | DSP frame sync input. Indication of the start of a serial data frame in or out of the device. If FS remains low at the falling edge of $\overline{\text{CS}}$ SDO is driven to zeros first and SDI is not enabled. A high-to-low transition on the FS input resets the internal 4-bit counter, enables SDI, and removes SDO from 3-state within a maximum setup time. SDI is disabled within a setup time after the 4-bit counter counts to 16 (clock edges) or a low-to-high transition of $\overline{\text{CS}}$ whichever happens first. SDO is 3-stated after the $16^{th}$ bit is presented. Tie this terminal to $V_{CC}$ if not used. |
| GND | 15 | I | Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND. |
| $\overline{\text{PWDN}}$ | 16 | I | Both analog and reference circuits are powered down when this pin is at logic zero. The device can be restarted by active $\overline{\text{CS}}$ or $\overline{\text{CSTART}}$ after this pin is pulled back to logic one. |

FIGURE 1. Terminal connections - continued.

| | | | |
|---|---|---|---|
| SCLK | 3 | I | Input serial clock. This terminal receives the serial SCLK from the host processor. SCLK is used to clock the input SDI to the input register. When programmed, it may also be used as the source of the conversion clock. This input is disabled when $\overline{CS}$ is not active ($\overline{CS}$ = high) if the conversion clock source is programmed as INTERNAL OSC [CFR.D(8,7) = 00]. |
| SDI | 2 | I | Serial data input. The input data is presented with the MSB (D15) first. The first 4-bit MSBs, D(15-12) are decoded as one of the 16 commands. All trailing blanks are filled with zeros. The configure write commands require an additional 12 bits of data. When FS is not used (FS = 1), the first MSB (D15) is expected after the falling edge of CS and is shifted in on the rising edges of SCLK (after CS↓). When FS is used (typical with an active FS from a DSP) the first MSB (D15) is expected after the falling edge of FS and is shifted in on the falling edges of SCLK. |
| SDO | 1 | O | The 3-state serial output for the A/D conversion result. SDO is kept in the high impedance state when $\overline{CS}$ is high and after the $\overline{CS}$ falling edge and until the MSB (D15) is presented. The output format is MSB (D15) first. When FS is not used (FS = 1 at the falling edge of $\overline{CS}$), the MSB (D15) is presented to SDO pin after the $\overline{CS}$ falling edge, and output data changes on the falling edge of SCLK. When FS is used (FS = 0 at the falling edge of $\overline{CS}$), the MSB (D15) is presented to SDO after the falling edge of $\overline{CS}$ and FS = 0 is detected. Data changes at the rising edge of SCLK. (This is typically used with an active FS from a DSP). For conversion and FIFO read cycle, the first 12 bits are result from previous conversion (data) followed by 4 trailing zeros. The first four bits from SDO for CFR read cycles should be ignored. The register content is in the last 12 bits. SDO is 3 stated after the 16$^{th}$ bit. |
| REFM | 18 | I | External reference input or internal reference decoupling. |
| REFP | 19 | I | External reference input or internal reference decoupling. (Shunt capacitors of 10 μF and 0.1 μF between REFP and REFM). The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the REFM terminal when an external reference is used. |
| $V_{CC}$ | 5 | I | Positive supply voltage. |

FIGURE 1. Terminal connections - continued.

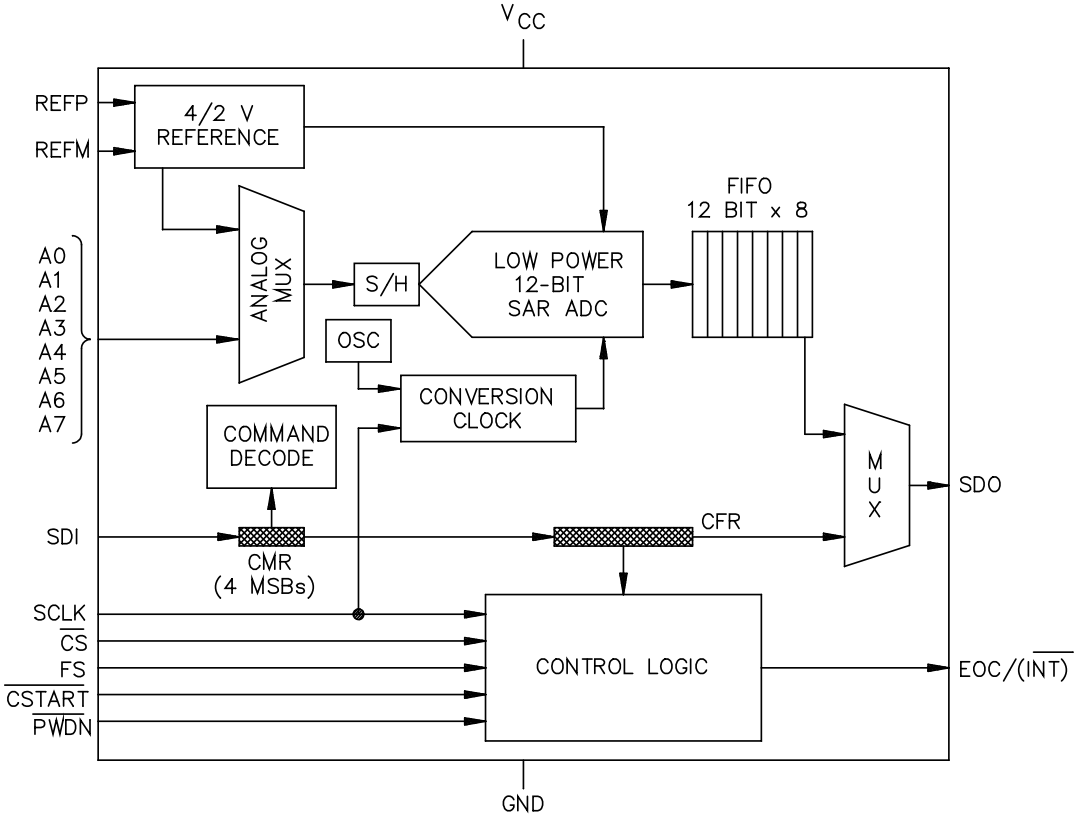



FIGURE 2. Block diagram.

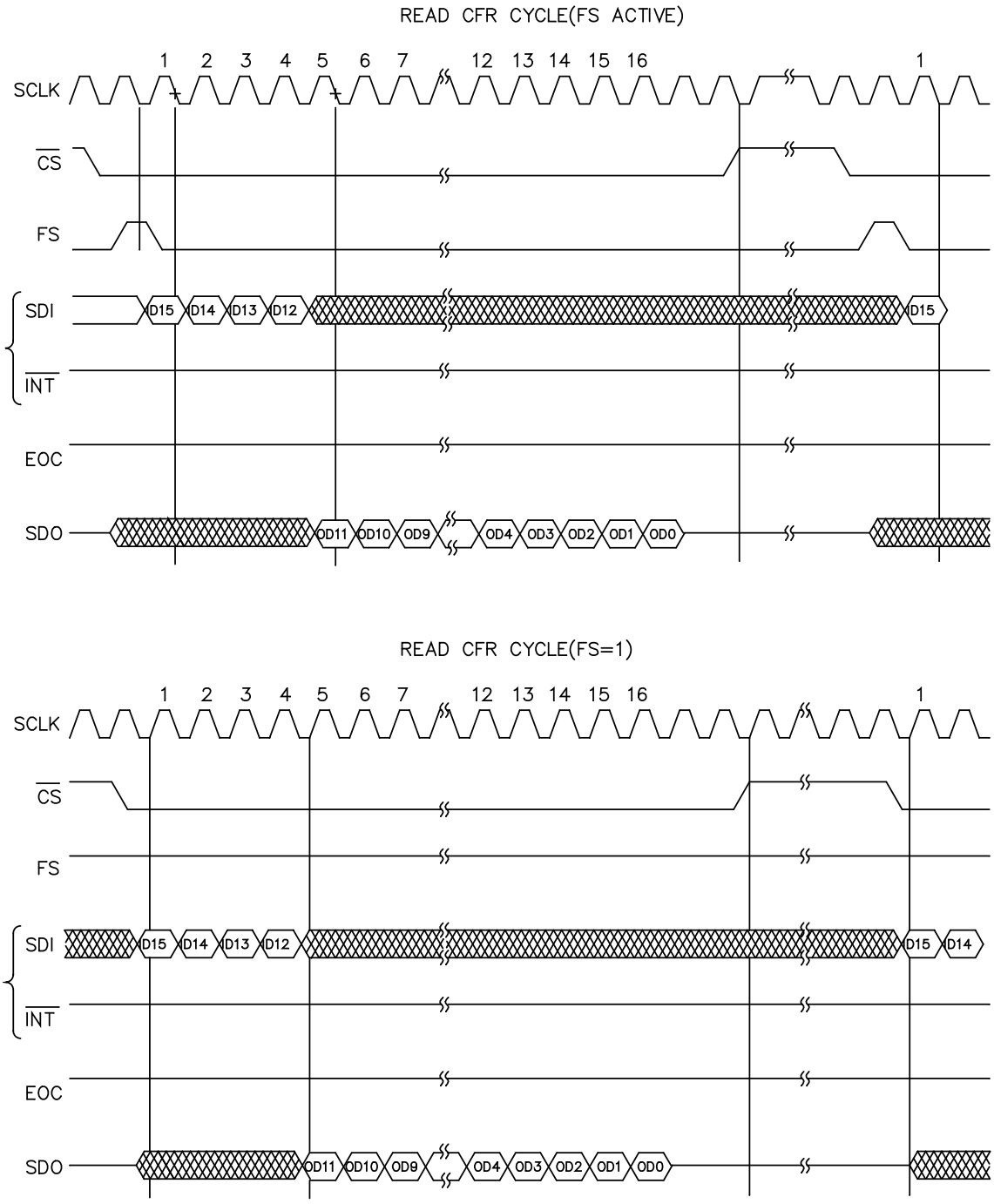



FIGURE 3. Timing waveforms.

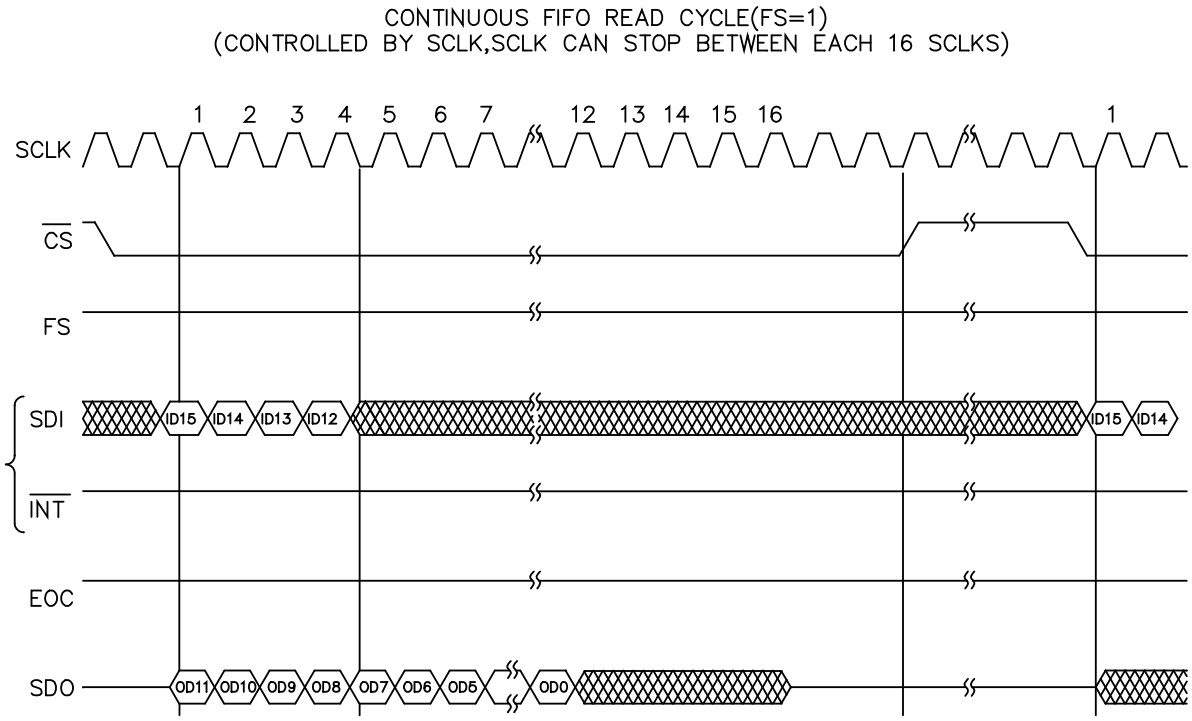



FIGURE 3. Timing waveforms - continued.

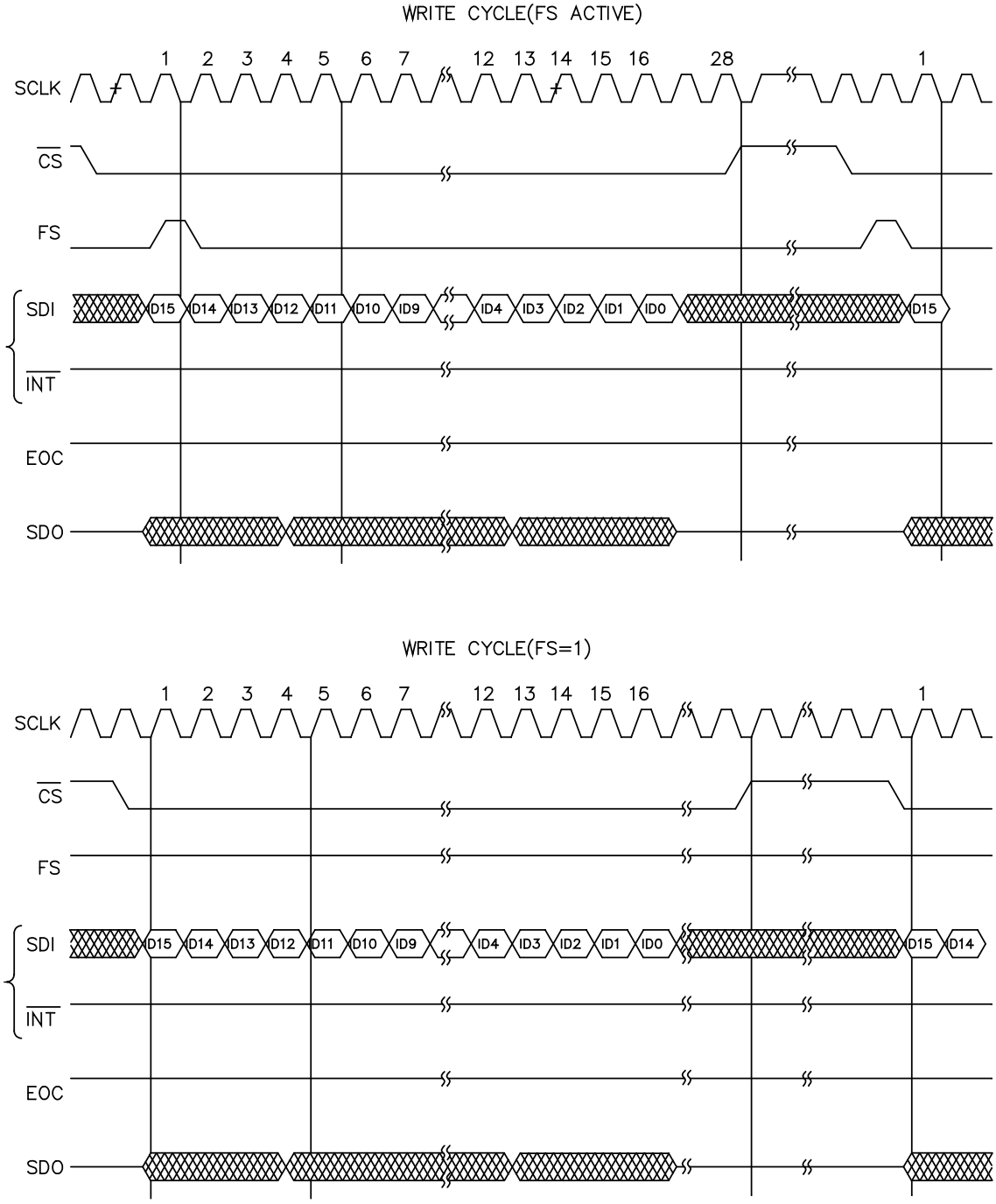



FIGURE 3. Timing waveforms - continued.

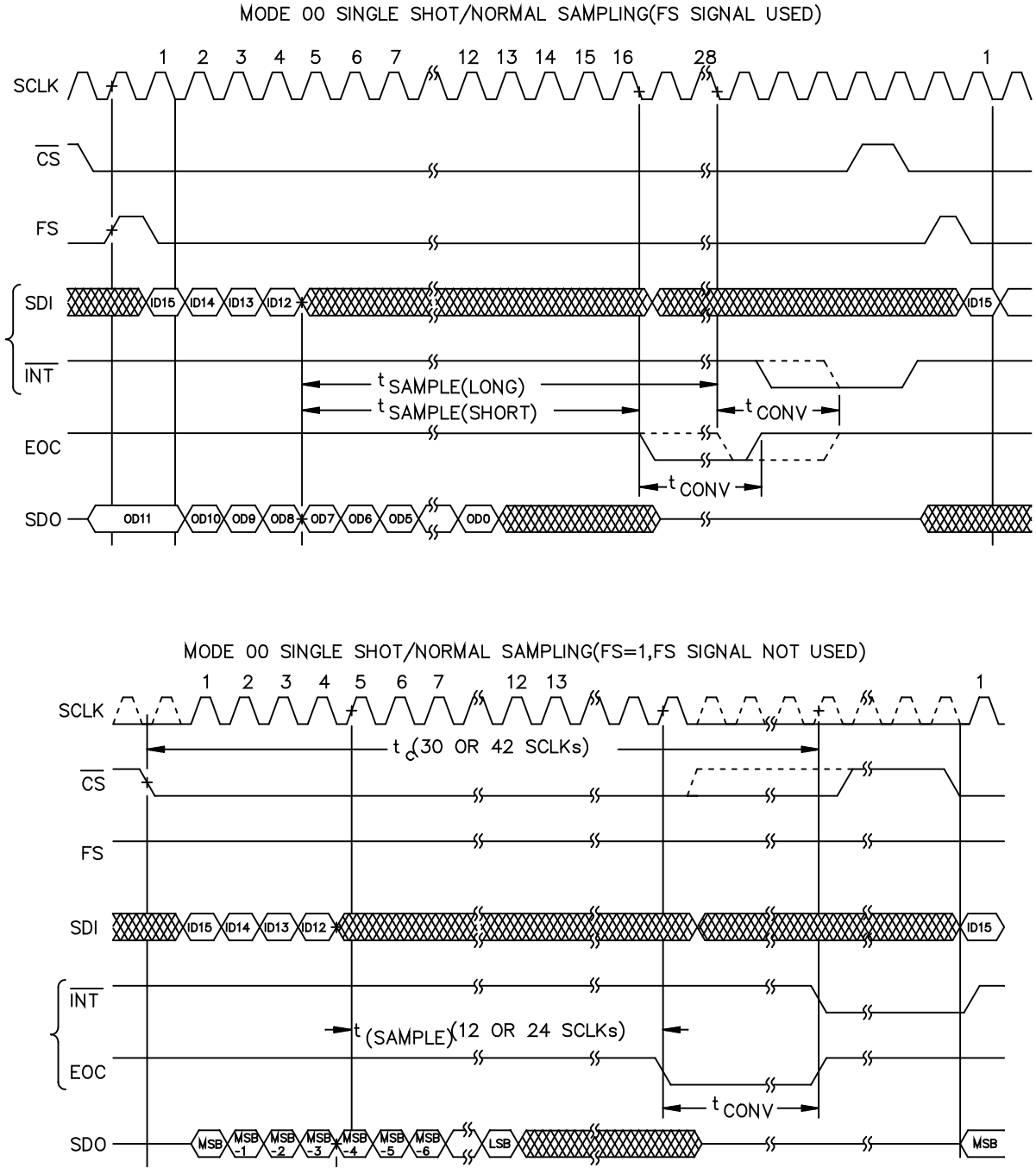
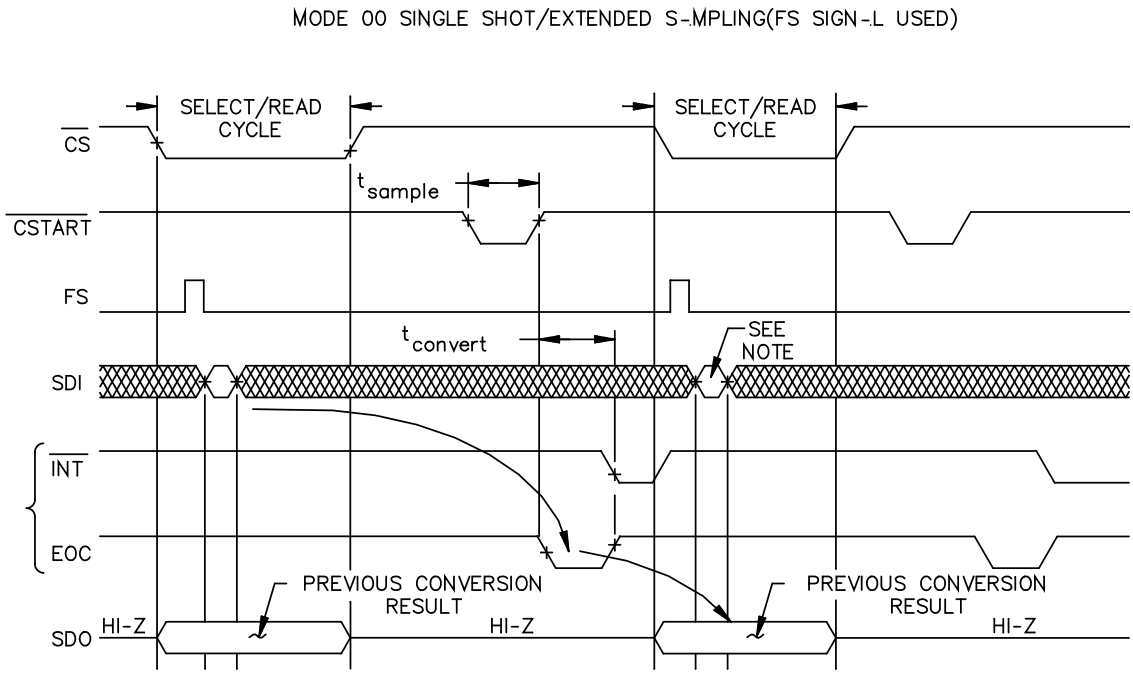
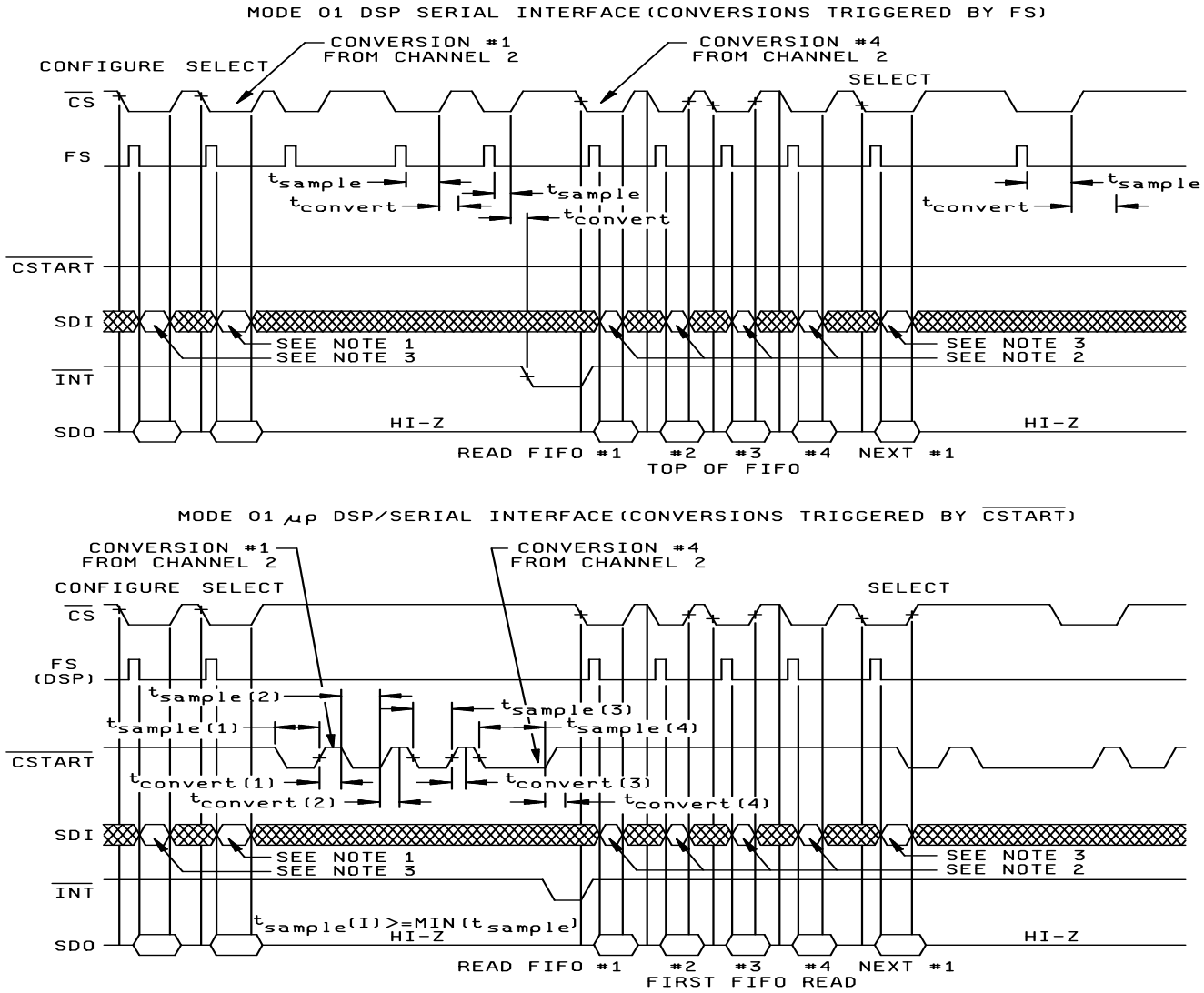



FIGURE 3. Timing waveforms - continued.



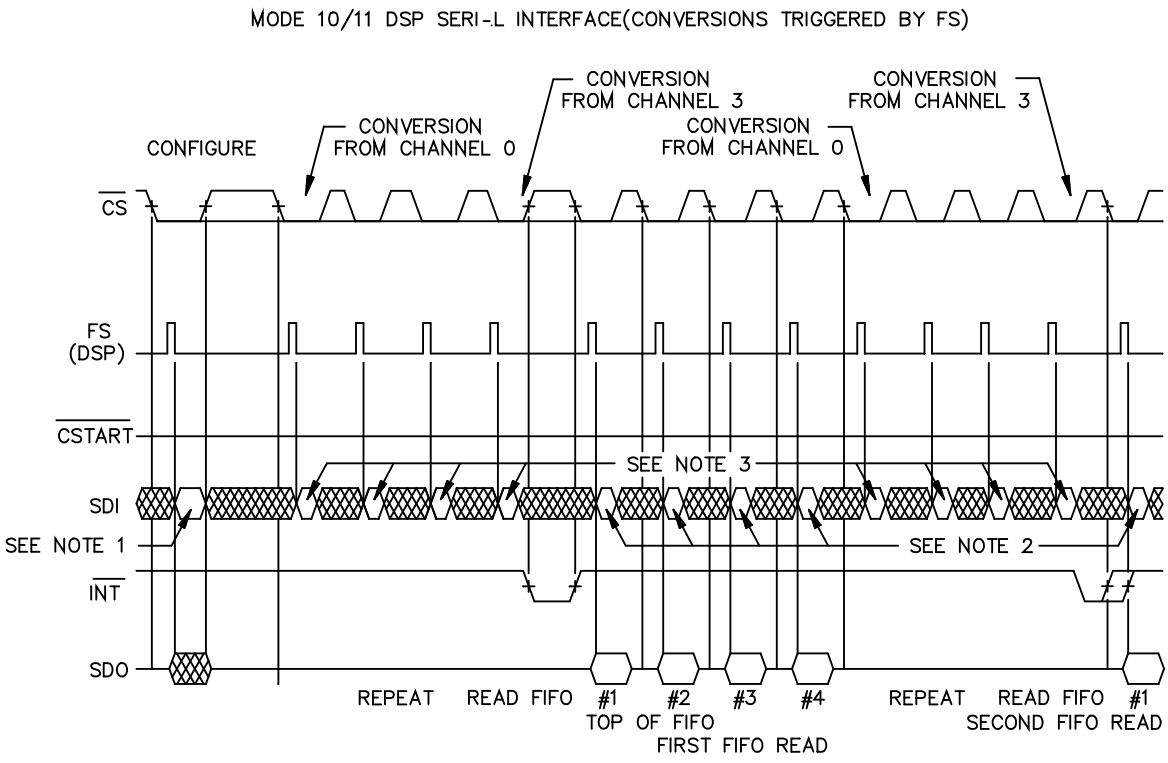

NOTE: This is one of the single shot commands. Conversion starts on next rising edge of $\overline{\text{CSTART}}$.

FIGURE 3. Timing waveforms - continued.




NOTE 1: Command = Configure write for mode 01, FIFO threshold = ½.
NOTE 2: Command = Read FIFO, 1st FIFO read.
NOTE 3: Command = Select channel 2.

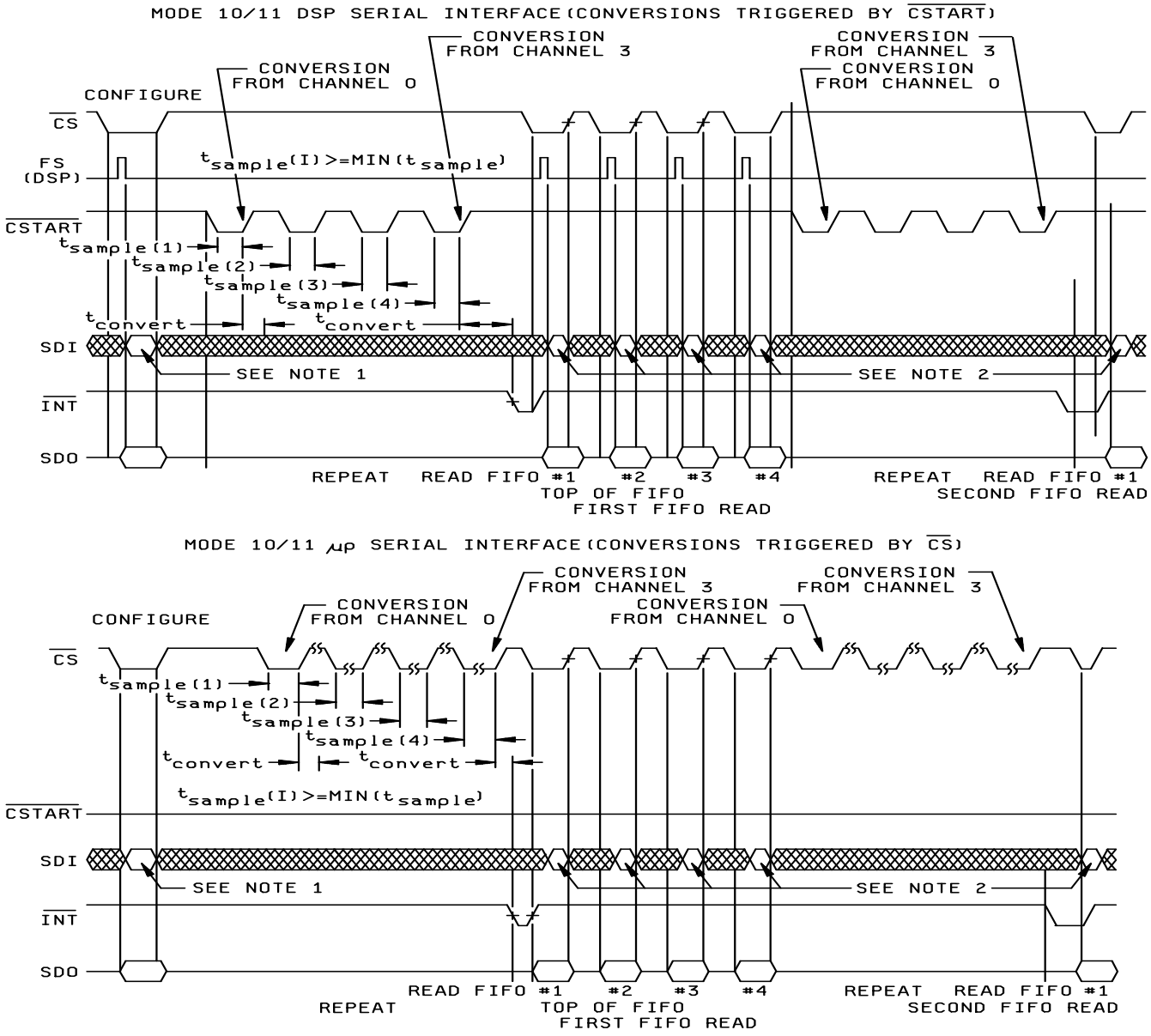
FIGURE 3. Timing waveforms - continued.




Mode 10/11 DSP Serial Interface (Conversions Triggered by FS)

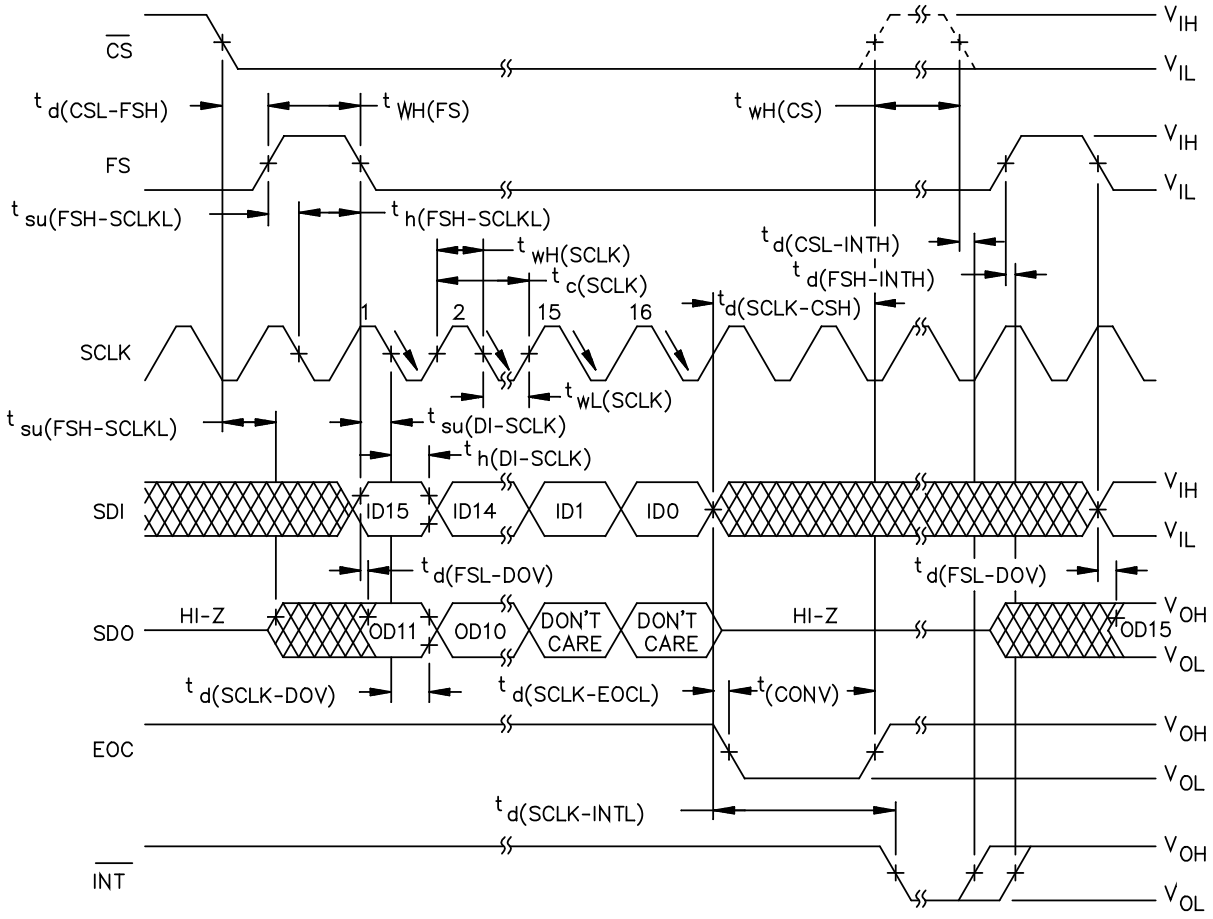
NOTE 1: Command = Configure write for mode 10 or 11, FIFO threshold = ½, sweep sequence = 0-1-2-3.
NOTE 2: Command = Read FIFO.
NOTE 3: Use any channel select command to trigger SDI input.

FIGURE 3. Timing waveforms - continued.




NOTE 1: Command = Configure write for mode 10 or 11, FIFO threshold = ½, sweep sequence = 0-1-2-3.
NOTE 2: Command = Read FIFO.

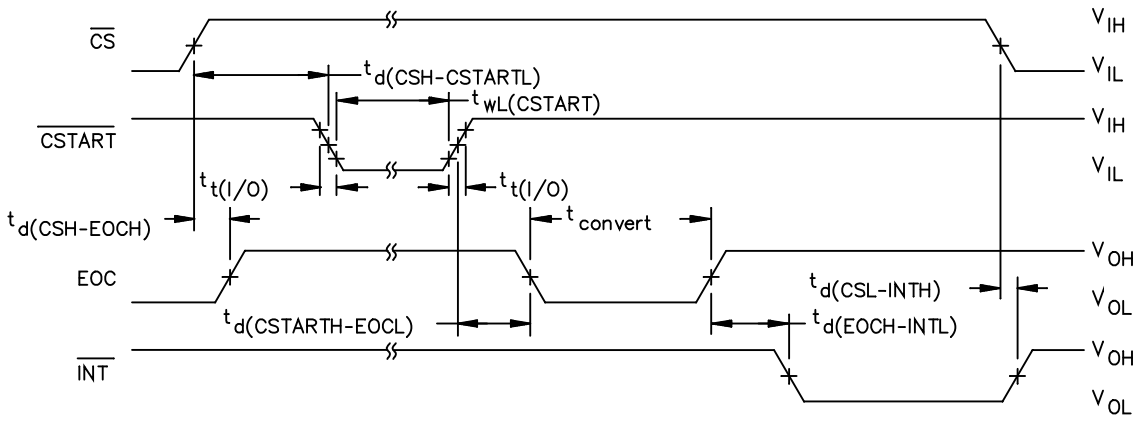
FIGURE 3. Timing waveforms - continued.




CRITICAL TIMING(NORM-L SAMPLING, FS IS ACTIVE)

FIGURE 3. Timing waveforms – continued.

CRITIC-L TIMING(EXTENDED SAMPLING,SINGLE SHOT)




CRITICAL TIMING(EXTENDED SAMPLING,REPEAT/SWEEP/REPEATSWEEP)

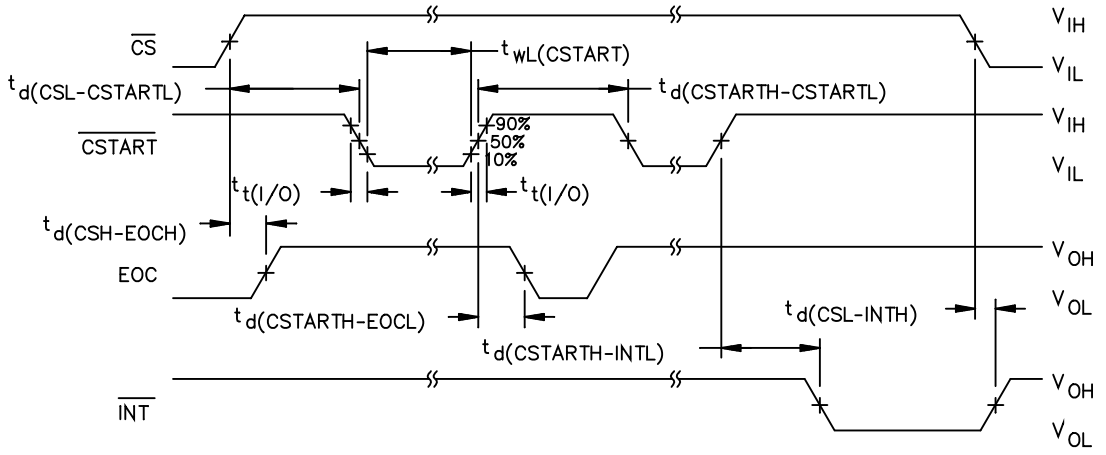



FIGURE 3. Timing waveforms – continued.

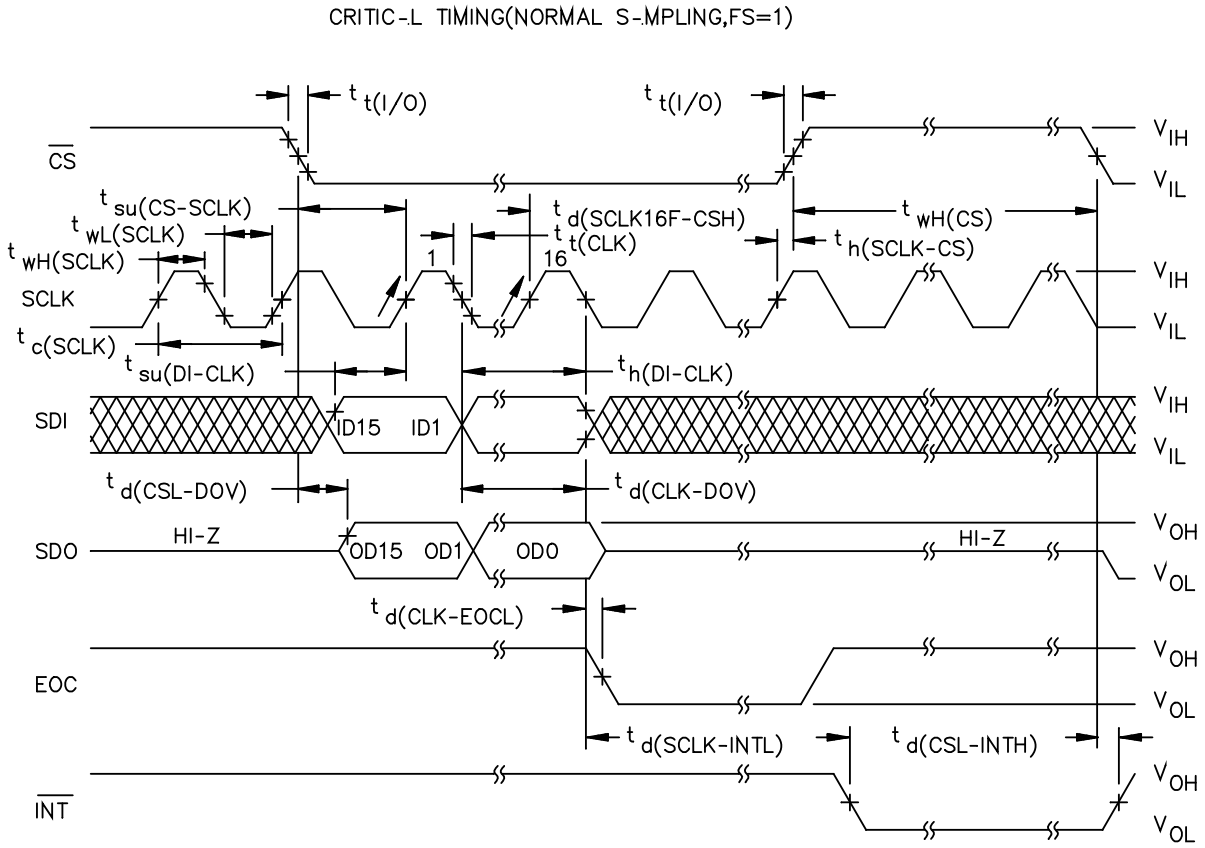



FIGURE 3. Timing waveforms – continued.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|
| | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | - - - |
| Final electrical parameters (see 4.2) | 1, 2, 3, 4, 5, 6, 9, 10, 11 1/ | 1, 2, 3, 4, 5, 6, 9, 10, 11 1/ |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 5, 6, 9, 10, 11 | 1, 2, 3, 4, 5, 6, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1 | 1 |
| Group D end-point electrical parameters (see 4.4) | 1 | 1 |
| Group E end-point electrical parameters (see 4.4) | - - - | - - - |

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-09-03

Approved sources of supply for SMD 5962-99570 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9957001QRA | 3/ | TLV2548MJB |
| 5962-9957001Q2A | 01295 | TLV2548MFKB |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Ln.<br>PO Box 660199<br>Dallas, TX 75243 |