| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Drawing updated to reflect current requirements. - gt | 02-05-22 | Raymond Monnin |
| B | Redrawn. Update paragraphs to MIL-PRF-38535 requirements. Remove class M requirements throughout. - drw | 14-06-12 | Charles F. Saffle |
| C | Make change to recommended operating conditions for high ($V_{IH}$) and low ($V_{IL}$) level digital input voltage levels in 1.4 herein. -rrp | 15-05-18 | Charles F. Saffle |
| D | Update paragraphs to current MIL-PRF-38535 requirements. - drw | 20-11-20 | James R. Eschmeyer |

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
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| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV STATUS | | | | REV | | | D | D | D | D | D | D | D | D | D | D | D | D | D | |
| OF SHEETS | | | | SHEET | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |

PMIC N/A

PREPARED BY
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CHECKED BY
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DRAWING APPROVAL DATE
99-10-20

REVISION LEVEL
D

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**https://www.dla.mil/LandandMaritime**

# STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL-LINEAR, DUAL, 12-BIT, PROGRAMMABLE, DIGITAL-TO-ANALOG CONVERTER, MONOLITHIC SILICON

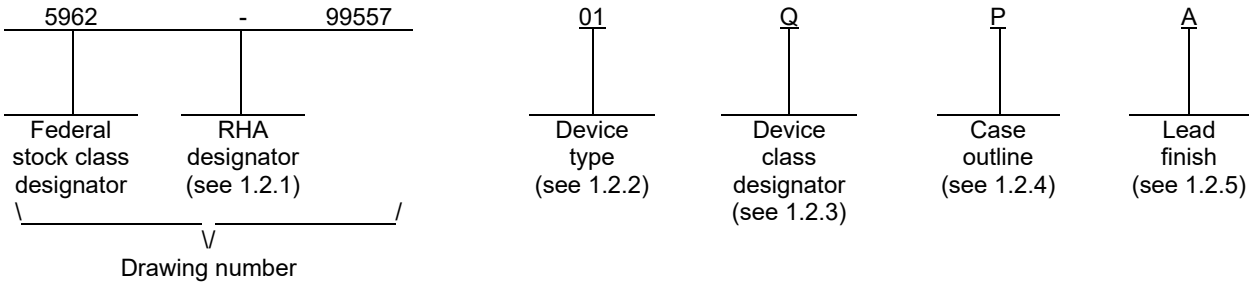
| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-99557** |

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | TLV5618AM | Dual, 12-bit, programmable digital-to-analog converter with power down |
| 02 | TLC5618AM | Dual, 12-bit, programmable digital-to-analog converter |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| P | GDIP1-T8 or CDIP2-T8 | 8 | Dual-in-line |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage ($V_{DD}$ to AGND) ..... 7 V
Digital input voltage range to AGND ..... -0.3 V $V_{DD}$ +0.3 V
Reference input voltage range to AGND ..... -0.3 V $V_{DD}$ +0.3 V
Output voltage at OUTPUT pin from external source (device type 02 only) ..... $V_{DD}$ +0.3 V
Continuous current at any terminal (device type 02 only) ..... ±20 mA
Power dissipation ($P_D$): ($T_A \leq 25°C$)
  Case P ..... 1050 mW 2/
  Case 2 ..... 1375 mW 3/
Junction temperature ($T_J$) ..... +150°C
Storage temperature range ..... -65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Thermal resistance, junction-to-case ($\theta_{JC}$) ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage ($V_{DD}$):
  Device type 01:
    With $V_{DD}$ = 5 V ..... 4.5 V to 5.5 V
    With $V_{DD}$ = 3 V ..... 2.7 V to 3.3 V
  Device type 02 ..... 4.5 V to 5.5 V
High level digital input voltage ($V_{IH}$):
  Device type 01:
    With $V_{DD}$ = 2.7 V ..... 2.0 V minimum
    With $V_{DD}$ = 5.5 V ..... 2.4 V minimum
  Device type 02 (with $V_{DD}$ = 5 V) ..... 0.7 $V_{DD}$ minimum 4/
Low level digital input voltage ($V_{IL}$):
  Device type 01:
    With $V_{DD}$ = 2.7 V ..... 0.6 V maximum
    With $V_{DD}$ = 5.5 V ..... 1.0 V maximum
  Device type 02 (with $V_{DD}$ = 5 V) ..... 0.3 $V_{DD}$ maximum 4/
Load resistance ($R_L$) ..... 2 kΩ
Load capacitance ($C_L$) (device type 01 only) ..... 100 pF maximum
Clock frequency ($f_{CLK}$) (device type 01 only) ..... 20 MHz
Ambient operating temperature range ($T_A$) ..... -55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ For case P, the derating factor above $T_A$ = +25°C is 8.4 mW/°C.
3/ For case 2, the derating factor above $T_A$ = +25°C is 11.0 mW/°C.
4/ This parameter is not production tested.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.4 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Power supply section | | | | | | | | |
| Power supply current | $I_{DD}$ | DAC latch = 0X800, no load, all inputs = AGND or $V_{DD}$ | fast | 1, 2, 3 | 01 | | 2.3 | mA |
| | | | slow | | | | 1 | |
| | | $V_{DD}$ = 5.5 V, no load, all inputs = 0 V or $V_{DD}$ | fast | | 02 | | 2.5 | |
| | | | slow | | | | 1 | |
| Reference input section | | | | | | | | |
| Input voltage range | $V_{IN}$ | REFIN = 2.048 V | | 1, 2, 3 | 01 | 0 | $V_{DD}$ -1.5 | V |
| | | | | | 02 | 0 | $V_{DD}$ -2 | |
| Digital inputs section | | | | | | | | |
| High level digital input current | $I_{IH}$ | $V_{IN} = V_{DD}$ | | 1, 2, 3 | 01 | | 1 | µA |
| | | ( DIN, SCLK, $\overline{CS}$ pins ), $V_{IN} = V_{DD}$ | | | 02 | | 1 | |
| Low level digital input current | $I_{IL}$ | $V_{IN}$ = 0 V | | 1, 2, 3 | 01 | -1 | | µA |
| | | ( DIN, SCLK, $\overline{CS}$ pins ), $V_{IN}$ = 0 V | | | 02 | -1 | | |
| Output sections | | | | | | | | |
| Output voltage range | $V_{OUT}$ | $R_L$ = 10 kΩ | | 1, 2, 3 | 01 | 0 | $V_{DD}$ -0.4 | V |
| | | ( OUTPUT A, OUTPUT B pins ), $R_L$ = 10 kΩ | | | 02 | | $V_{DD}$ -0.4 | |
| Output load regulation accuracy | $V_{OLR}$ | $V_O$ = 4.096 V, 2.048 V, $R_L$ = 2 kΩ | | 1, 2, 3 | 01 | | ±0.29 | % of FS voltage |
| | | ( OUTPUT A, OUTPUT B pins ), $V_{O(OUT)}$ = 4.096 V, $R_L$ = 2 kΩ | | | 02 | | ±0.29 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Static DAC section | | | | | | | | |
| Resolution | RES | | | 1, 2, 3 | All | 12 | | bits |
| Integral nonlinearity 2/ | INL | | | 1, 2, 3 | 01 | | ±4 | LSB |
| | | End point adjusted | | | 02 | | ±4 | |
| Differential nonlinearity 3/ | DNL | | | 1, 2, 3 | All | | ±1 | LSB |
| Zero scale error, offset error at zero scale 4/ | EZS | | | 1, 2, 3 | All | | ±12 | mV |
| Gain error | EG | 5/ | | 1, 2, 3 | All | | ±0.6 | % of FS voltage |
| Analog output dynamic section | | | | | | | | |
| Positive output slew rate | +SR | $C_L$ = 100 pF, $R_L$ = 10 kΩ, code 32 to code 4096, $T_A$ = +25°C, $V_{OUT}$ from 10 % to 90 % | Slow | 4 | 02 | 0.3 | | V/µs |
| | | | Fast | | | 2.4 | | |
| Negative output slew rate | -SR | $C_L$ = 100 pF, $R_L$ = 10 kΩ, code 4096 to code 32, $T_A$ = +25°C, $V_{OUT}$ from 10 % to 90 % | Slow | 4 | 02 | 0.15 | | V/µs |
| | | | Fast | | | 1.2 | | |
| Signal to noise ratio | SNR | $f_S$ = 102 kSPS, $f_{OUT}$ = 1 kHz, $C_L$ = 100 pF, $R_L$ = 10 kΩ | | 4, 5, 6 | 01 | 72 | | dB |
| Signal to noise + distortion | SINAD | $f_S$ = 102 kSPS, $f_{OUT}$ = 1 kHz, $C_L$ = 100 pF, $R_L$ = 10 kΩ | | 4, 5, 6 | 01 | 58 | | dB |
| Total harmonic distortion | THD | $f_S$ = 102 kSPS, $f_{OUT}$ = 1 kHz, $C_L$ = 100 pF, $R_L$ = 10 kΩ | | 4, 5, 6 | 01 | | -57 | dB |
| Spurious free dynamic range | SFDR | $f_S$ = 102 kSPS, $f_{OUT}$ = 1 kHz, $C_L$ = 100 pF, $R_L$ = 10 kΩ | | 4, 5, 6 | 01 | 57 | | dB |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Digital input timing section | | | | | | | |
| Setup time, $\overline{CS}$ low before first negative SCLK edge | $t_{su}$ (CS-CK) | See figure 3 | 9, 10, 11 | All | 5 | | ns |
| Setup time, 16th negative SCLK edge before $\overline{CS}$ rising edge | $t_{su}$ (C16-CS) | See figure 3 | 9, 10, 11 | All | 10 | | ns |
| SCLK pulse width high | $t_{WH}$ | See figure 3 | 9, 10, 11 | All | 25 | | ns |
| SCLK pulse width low | $t_{WL}$ | See figure 3 | 9, 10, 11 | All | 25 | | ns |
| Setup time, data ready before SCLK falling edge | $t_{su(D)}$ | See figure 3 | 9, 10, 11 | All | 8 | | ns |
| Hold time, data held valid after SCLK falling edge | $t_{h(D)}$ | See figure 3 | 9, 10, 11 | All | 5 | | ns |

1/ Unless otherwise specified, $V_{DD}$ = 2.7 V to 5.5 V for device type 01. $V_{DD}$ = 5 V ±5 %, $V_{ref(REFIN)}$ = 2.048 V for device type 02.

2/ The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full scale errors.

3/ The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measure and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

4/ Zero scale error is the deviation from zero voltage output when the digital input code is zero.

5/ Gain error is the deviation from the ideal output ($2 V_{ref}$ – 1 LSB) with an output load of 10 kΩ.

| Device types | 01 and 02 | |
|---|---|---|
| Case outlines | P | 2 |
| Terminal number | Terminal symbol | |
| 1 | DIN | NC |
| 2 | SCLK | DIN |
| 3 | $\overline{CS}$ | NC |
| 4 | OUTPUT A | NC |
| 5 | AGND | SCLK |
| 6 | REFIN | NC |
| 7 | OUTPUT B | $\overline{CS}$ |
| 8 | $V_{DD}$ | NC |
| 9 | --- | NC |
| 10 | --- | OIUTPUT A |
| 11 | --- | NC |
| 12 | --- | AGND |
| 13 | --- | NC |
| 14 | --- | NC |
| 15 | --- | REFIN |
| 16 | --- | NC |
| 17 | --- | OUTPUT B |
| 18 | --- | NC |
| 19 | --- | NC |
| 20 | --- | $V_{DD}$ |

NC = No connection

FIGURE 1. Terminal connections.

Device type 01

| Terminal symbol | I / O / P | Description |
|---|---|---|
| AGND | P | Ground |
| $\overline{CS}$ | I | Chip select. Digital input active low, used to enable/disable inputs. |
| DIN | I | Digital serial data input |
| OUTPUT A | O | DAC A analog output |
| OUTPUT B | O | DAC B analog output |
| REFIN | I | Analog reference voltage input |
| SCLK | I | Digital serial clock input |
| $V_{DD}$ | P | Positive power supply |

Device type 02

| Terminal symbol | I / O | Description |
|---|---|---|
| AGND | | Analog ground |
| $\overline{CS}$ | I | Chip select, active low |
| DIN | I | Serial data input |
| OUTPUT A | O | DAC A analog output |
| OUTPUT B | O | DAC B analog output |
| REFIN | I | Reference voltage input |
| SCLK | I | Serial clock input |
| $V_{DD}$ | | Positive power supply |

FIGURE 1. Terminal connections - continued.

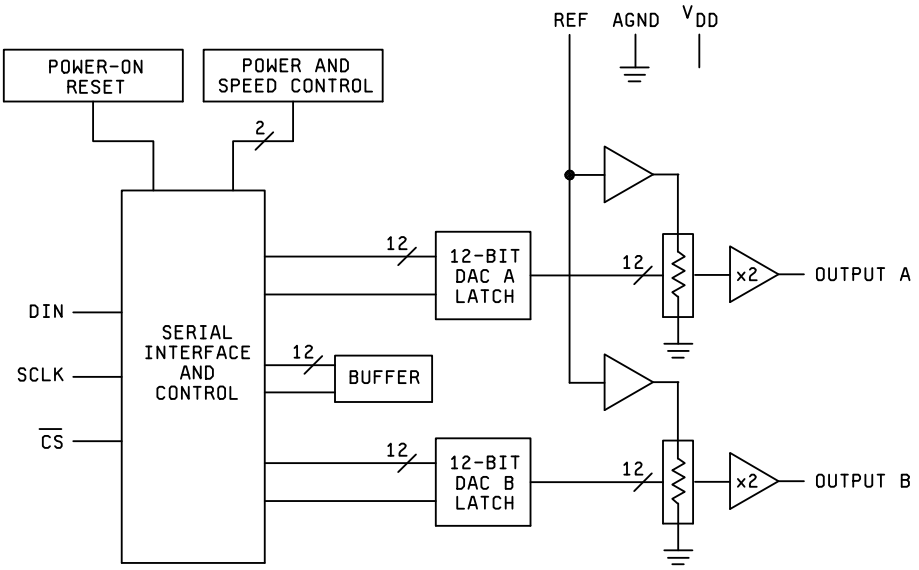



FIGURE 2. Block diagram.

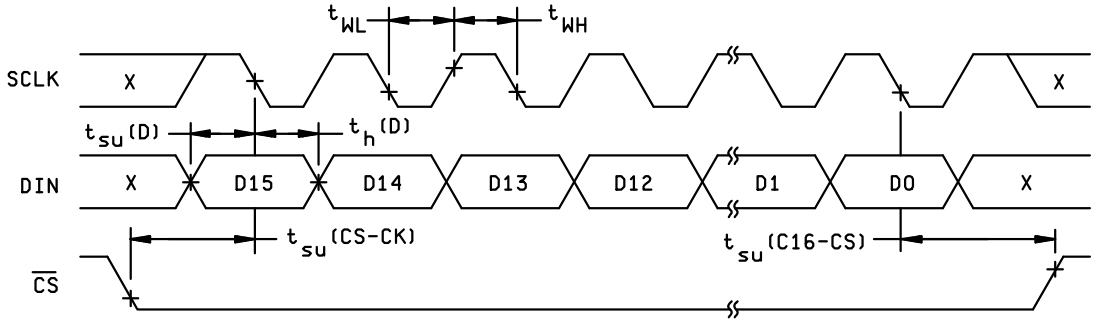



FIGURE 3. Timing waveforms.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|
| | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | - - - |
| Final electrical parameters (see 4.2) | 1, 2, 3, 4, 5, 6, 9, 10, 11 1/ | 1, 2, 3, 4, 5, 6, 9, 10, 11 1/ |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 5, 6, 9, 10, 11 | 1, 2, 3, 4, 5, 6, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1 | 1 |
| Group D end-point electrical parameters (see 4.4) | 1 | 1 |
| Group E end-point electrical parameters (see 4.4) | - - - | - - - |

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-11-20

Approved sources of supply for SMD 5962-99557 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9955701Q2A | 01295 | TLV5618AMFKB |
| 5962-9955701QPA | 01295 | TLV5618AMJGB |
| 5962-9955702Q2A | 01295 | TLC5618AMFKB |
| 5962-9955702QPA | 01295 | TLC5618AMJGB |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Lane<br>P.O. Box 660199<br>Dallas, TX 75243 |