

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I parameter changes: C_{IN} , t_{HPT} , t_{SPT} , t_{IHPT} , t_{ISPT} and t_{SLEW} for device 01, editorial changes Table I and Terminal connections. ksr	01-08-27	Raymond Monnin
B	Boilerplate update and part of five year review. tcr	05-12-30	Raymond Monnin
C	Updated boilerplate for five year review. lhl	12-03-21	Charles F. Saffle
D	Updated boilerplate to current MIL-PRF-38535 requirements and removed all Class M references; Updated 1.3 and 3.10 to include $T_{use} = +55$ degrees C; Updated 3.9 and 3.10 to include sampling 20(0). lhl	13-11-12	Charles F. Saffle

REV																				
SHEET																				
REV	D	D	D	D	D	D	D													
SHEET	15	16	17	18	19	20	21													
REV STATUS OF SHEETS	REV			D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			
PMIC N/A	PREPARED BY Kenneth Rice							DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil												
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Jeff Bowling																			
	APPROVED BY Raymond Monnin																			
	DRAWING APPROVAL DATE 00-05-12																			
	REVISION LEVEL D							SIZE A	CAGE CODE 67268	5962-99522										
							SHEET 1 OF 21													

1.4 Recommended operating conditions. 4/

Case operating temperature Range (T _C)-----	-55°C to +125°C
Supply voltage relative to ground (V _{CC})-----	+3.0V dc minimum to +3.6 V dc maximum
Ground voltage (GND) -----	0 V dc
Input high voltage (V _{IH})-----	2.0 V dc minimum
Input low voltage (V _{IL})-----	0.8 V dc maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JESD78 - IC Latch-Up Test.

(Copies of this document are available online at www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4/ All voltage values in this drawing are with respect to V_{SS}.

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3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Processing CPLDs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.8.1 Erasure of CPLDs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6 herein.

3.8.2 Programmability of CPLDs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7 herein.

3.8.3 Verification of erasure or programmed CPLDs. When specified, devices shall be verified as either programmed (see 4.7 herein) to the specified pattern or erased (see 4.6 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.9 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device using 20(0) sampling. The methods and procedures may be vendor specific, but shall be under document control and shall be made available upon request.

3.10 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention using 20(0) sampling. The methods and procedures may be vendor specific, but shall guarantee 10 years minimum at Tuse = +55°C. The vendor's procedure shall be kept under document control and shall be made available upon request by the preparing or acquiring activity, along with the test data.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 3.0 V ≤ V _{CC} ≤ 3.6 V -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit		
					Min	Max			
High Level output voltage	V _{OH}	V _{CC} = 3.0 V, V _{IL} = 0.8V I _{OH} = -3.0 mA, V _{IH} = 2.0 V <u>1/</u>	1, 2, 3	01	2.4		V		
Low level output voltage	V _{OL}	V _{CC} = 3.0 V, I _{OL} = 6.0 mA V _{IL} = 0.8 V, V _{IH} = 2.0 V <u>1/</u>					0.5	V	
High level input voltage <u>2/</u>	V _{IH}						2	5.5	V
Low level input voltage <u>2/</u>	V _{IL}						-0.5	0.8	V
Input load current	I _{IX}	V _{IN} = 0 V or V _{CC} , with Busshold off					-10	+10	μA
Output leakage current	I _{OZ}	V _{CC} = 3.6 V, V _O = GND or V _{CC} , Output disabled, Busshold off					-50	+50	μA
Output short circuit current <u>3/ 4/</u>	I _{OS}	V _{CC} = 3.6 V, V _{OUT} = 0.5 V					-30	-160	mA
Power supply current <u>5/</u>	I _{CC}	V _{CC} = 3.6 V, I _{OUT} = 0 mA, V _{IN} = 0 V and 3.6 V f = 1.0 MHz						200	mA
Input bus hold low sustained current <u>3/</u>	I _{BHL}	V _{CC} = 3.0 V, V _{IL} = 0.8 V					+75		μA
Input bus hold high sustained current <u>3/</u>	I _{BHH}	V _{CC} = 3.0 V, V _{IH} = 2.0 V					-75		μA
Input bus hold low sustained overdrive current <u>3/</u>	I _{BHLO}	V _{CC} = 3.6 V						+500	μA
Input bus hold high sustained overdrive current <u>3/</u>	I _{BHHO}	V _{CC} = 3.6 V						-500	μA
Input capacitance <u>3/</u>	C _{IN}	See 4.4.1e, V _{IN} = 3.3 V, f = 1 MHz, T _A = 25°C	4	01		10	pF		
Output capacitance <u>3/</u>	C _{OUT}	See 4.4.1e, V _{IN} = 3.3 V, f = 1 MHz, T _A = 25°C	4	01		12	pF		
Dual functional pin capacitance <u>3/</u>	C _{DP}	See 4.4.1e, V _{IN} = 3.3 V, f = 1 MHz, T _A = 25°C	4	01		16	pF		
Functional test		See 4.4.1c	7,8A,8B	01					

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3.0 V ≤ V _{CC} ≤ 3.6 V -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Input to combinatorial output <u>6/ 7/ 8/</u>	t _{PD}	See figures 2 and 3 (circuit A)	9, 10, 11	01		15	ns
Input to output through transparent input or output latch <u>3/ 6/ 7/ 8/</u>	t _{PDL}			01		19	ns
Input to output through transparent input and output latch <u>3/ 6/ 7/ 8/</u>	t _{PDLL}			01		20	ns
Input to output enable see figure 3 test waveforms <u>3/ 6/ 7/ 8/</u>	t _{EA}	See figures 2 and 3 (circuit B)		01		19	ns
Input to output disable see figure 3 test waveforms <u>3/ 6/ 7/</u>	t _{ER}			01		19	ns
Clock or Latch enable input High time <u>3/ 6/</u>	t _{WH}	See figures 2 and 3 (circuit A)		01	4		ns
Clock or latch enable input low time <u>3/ 6/</u>	t _{WL}			01	4		ns
Input register or latch set-up time <u>3/ 6/</u>	t _{IS}			01	3.0		ns
Input register or latch hold time <u>3/ 6/</u>	t _{IH}			01	3.0		ns
Input register clock or latch enable to combinatorial output <u>3/ 6/ 7/ 8/</u>	t _{ICO}			01		19	ns
Input register clock or latch enable to output through transparent output latch <u>3/ 6/ 7/ 8/</u>	t _{ICOL}			01		21	ns
Synchronous clock or latch enable to output <u>3/ 6/ 8/</u>	t _{CO}			01		8	ns
Register or latch data hold time <u>6/</u>	t _H			01	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3.0 V ≤ V _{CC} ≤ 3.6 V -55°C ≤ T _C ≤ +125°C	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Set-up time from input to synchronous clock or latch enable <u>6/ 7/</u>	t _S		9, 10, 11	01	8		ns
Set-up time from input through transparent latch to output register Synchronous clock or latch enable <u>3/ 6/ 7/</u>	t _{SL}			01	15		ns
Output Synchronous clock or latch enable to combinatorial output delay (through memory array) <u>3/ 6/ 7/ 8/</u>	t _{CO2}			01		19	ns
Output Synchronous clock or latch enable to output synchronous clock or latch enable (through logic array) <u>6/ 7/</u>	t _{SCS}			01	12		ns
Hold time for input through transparent latch from output register Synchronous clock or latch enable <u>3/ 6/</u>	t _{HL}			01	0		ns
Maximum frequency with internal feedback (lesser of 1/t _{SCS} , 1/(t _S + t _H), or 1/t _{CO}) <u>3/ 6/</u>	f _{MAX1}			01	83		MHz

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3.0 V ≤ V _{CC} ≤ 3.6 V -55°C ≤ T _C ≤ +125°C	Group A Subgroups	Device type	Limits		Unit	
					Min	Max		
Maximum frequency data path in output register/latched mode (lesser of 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{CO}) <u>3/ 6/</u>	f _{MAX2}	See figures 2 and 3 (circuit A)	9, 10, 11	01	125		MHz	
Maximum frequency with external feedback (lesser of 1/(t _{CO} + t _S), or 1/(t _{WL} + t _{WH}) <u>3/ 6/</u>	f _{MAX3}			01	62.5			
Maximum frequency in pipelined mode (lesser of 1/(t _{CO} + t _S), 1/t _{CS} , 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{SCS}) <u>3/ 6/</u>	f _{MAX4}			01	83.0			
Input register Synchronous clock to output register clock <u>3/ 6/ 7/</u>	t _{CS}			01	12			Ns
Asynchronous preset width <u>3/ 6/</u>	t _{PW}			01	15			
Asynchronous preset recovery time <u>3/ 6/ 7/</u>	t _{PR}			01	17			
Asynchronous preset to output <u>3/ 6/ 7/ 8/</u>	t _{PO}			01		21		
Asynchronous reset width <u>3/ 6/</u>	t _{RW}			01	15			
Asynchronous reset recovery time <u>3/ 6/ 7/</u>	t _{RR}			01	17			
Asynchronous reset to output <u>3/ 6/ 7/ 8/</u>	t _{RO}			01		21		
Product term clock or latch enable (PTCLK) to output <u>3/ 6/ 7/ 8/</u>	t _{COPT}			01		15		
Register or latch data hold time <u>3/ 6/</u>	t _{HPT}			01	6.0			
Set-up time from input to product term clock or latch enable (PTCLK) <u>3/ 6/</u>	t _{SPT}			01	6.0			

See footnotes at the end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3.0 V ≤ V _{CC} ≤ 3.6 V -55°C ≤ T _C ≤ +125°C	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Set-up time for buried register used as an input register from input to product term clock or latch enable (PTCLK) <u>3/ 6/ 7/</u>	t _{ISPT}	See figures 2 and 3 (circuit A)	9, 10, 11	01	0		ns
Buried register used as an input register or latch data hold time <u>3/ 6/</u>	t _{IHPT}			01	14		
Product term clock or latch enable (PTCLK) to output delay (through logic array) <u>3/ 6/ 7/8/</u>	t _{CO2PT}			01		24	
Low power adder <u>3/ 6/</u>	t _{LP}			01		2.5	
Slow output slew rate adder <u>3/ 6/</u>	t _{SLEW}			01		3.0	
Set-up time from TDI and TMS to TCK <u>3/ 6/</u>	t _{S JTAG}			01	0		
Hold time on TDI and TMS <u>3/ 6/</u>	t _{H JTAG}			01	20		
Falling edge of TCK to TDO <u>3/ 6/</u>	t _{CO JTAG}			01		20	
Maximum JTAG tap controller frequency <u>3/ 6/</u>	f _{JTAG}			01		20	MHz

1/ I_{OH} = -2 mA, I_{OL} = +2 mA for TDO.

2/ These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

3/ Tested initially and after any design or process changes that affect this parameter.

4/ Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

5/ Measured under AC conditions. Program pattern using 16-bit counter per logic block or equivalent.

6/ All AC parameters are measured with 2 outputs switching, and 35 pF AC test load, unless otherwise specified.

7/ Logic blocks operating in low power mode, add t_{LP} to this spec.

8/ Outputs using slow output slew rate, add t_{SLEW} to this spec.

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SHEET

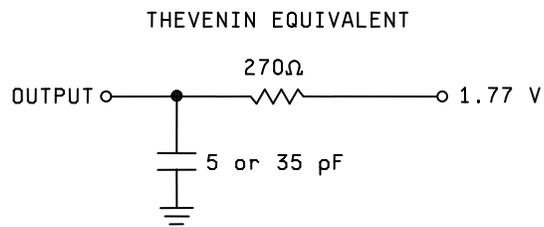
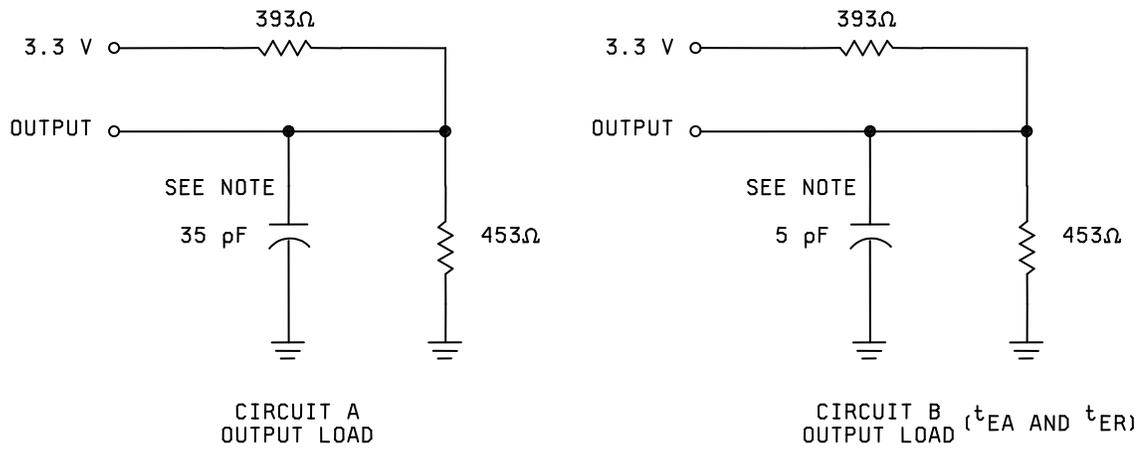
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Case outline Y

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	GND		29	I/O		57	I/O
2	V _{CC}		30	I/O		58	I/O
3	I/O		31	I/O		59	I/O
4	I/O		32	GND		60	I/O
5	I/O		33	I/O		61	I/O
6	I/O		34	I/O		62	CLK/I
7	I/O		35	I/O/TMS		63	V _{CC}
8	I/O		36	I/O		64	GND
9	I/O		37	I/O		65	CLK/I
10	I/O		38	I/O		66	I/O
11	GND		39	I/O		67	I/O
12	I/O		40	I/O		68	I/O
13	I/O		41	I		69	I/O
14	I/O/TCK		42	V _{CC}		70	I/O
15	I/O		43	GND		71	I/O
16	I/O		44	V _{CC}		72	I/O/TDI
17	I/O		45	I/O		73	I/O
18	I/O		46	I/O		74	GND
19	I/O		47	I/O		75	I/O
20	CLK/I		48	I/O		76	I/O
21	V _{CC}		49	I/O		77	I/O
22	GND		50	I/O		78	I/O
23	CLK/I		51	I/O/TDO		79	I/O
24	I/O		52	I/O		80	I/O
25	I/O		53	GND		81	I/O
26	I/O		54	I/O		82	I/O
27	I/O		55	I/O		83	JTAG _{EN}
28	I/O		56	I/O		84	V _{CC}

FIGURE 1. Terminal connections.

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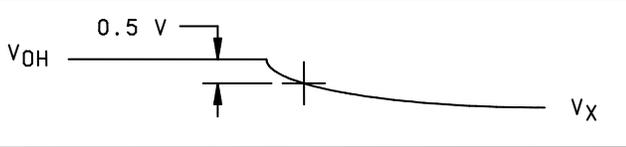
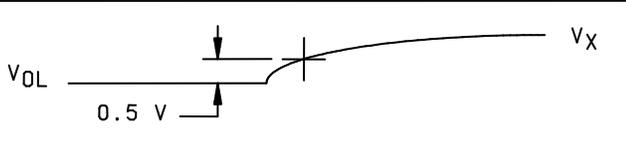
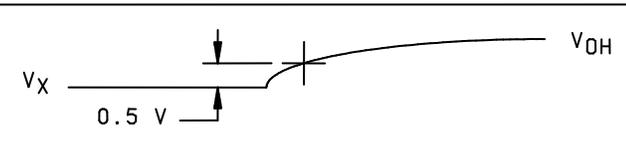
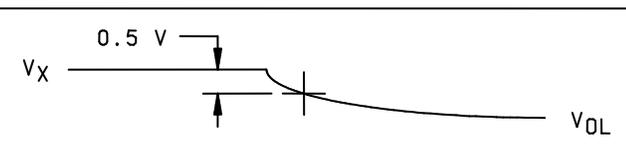


NOTE: INCLUDING SCOPE AND JIG (MINIMUM VALUES) .

FIGURE 2. Output load circuits and test conditions.

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TEST WAVEFORMS

PARAMETER	V_X	OUTPUT WAVEFORM - MEASUREMENT LEVEL
$t_{ER(-)}$	1.5 V	
$t_{ER(+)}$	2.6 V	
$t_{EA(+)}$	1.5 V	
$t_{EA(-)}$	V_{thc}	

INPUT PULSES

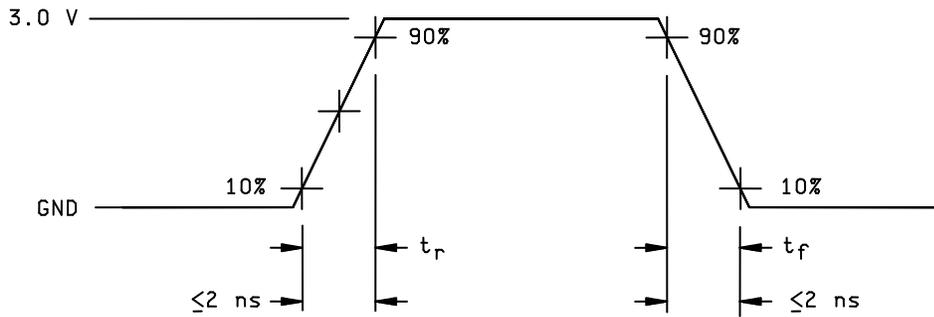


FIGURE 2. Output load circuits and test conditions - Continued.

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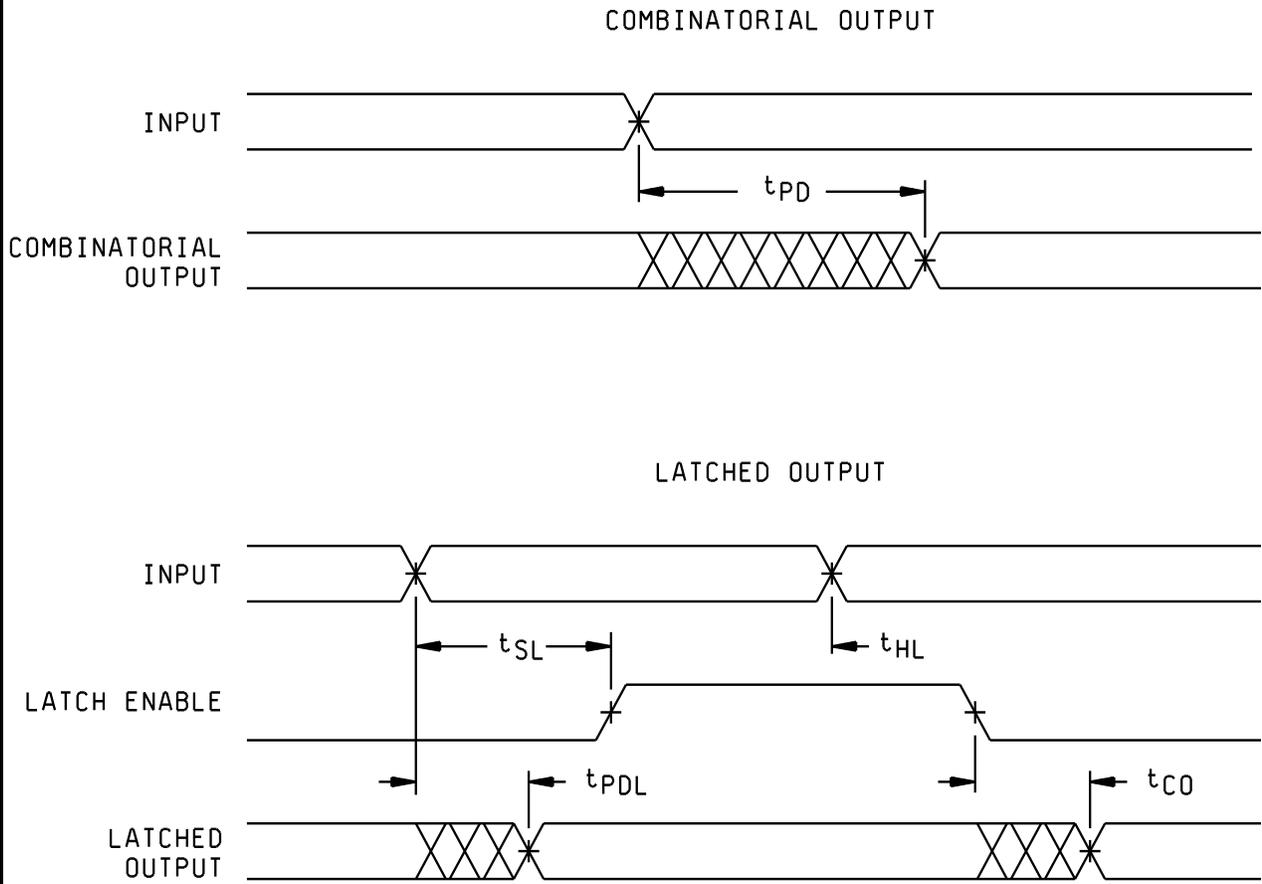


FIGURE 3. Switching waveforms.

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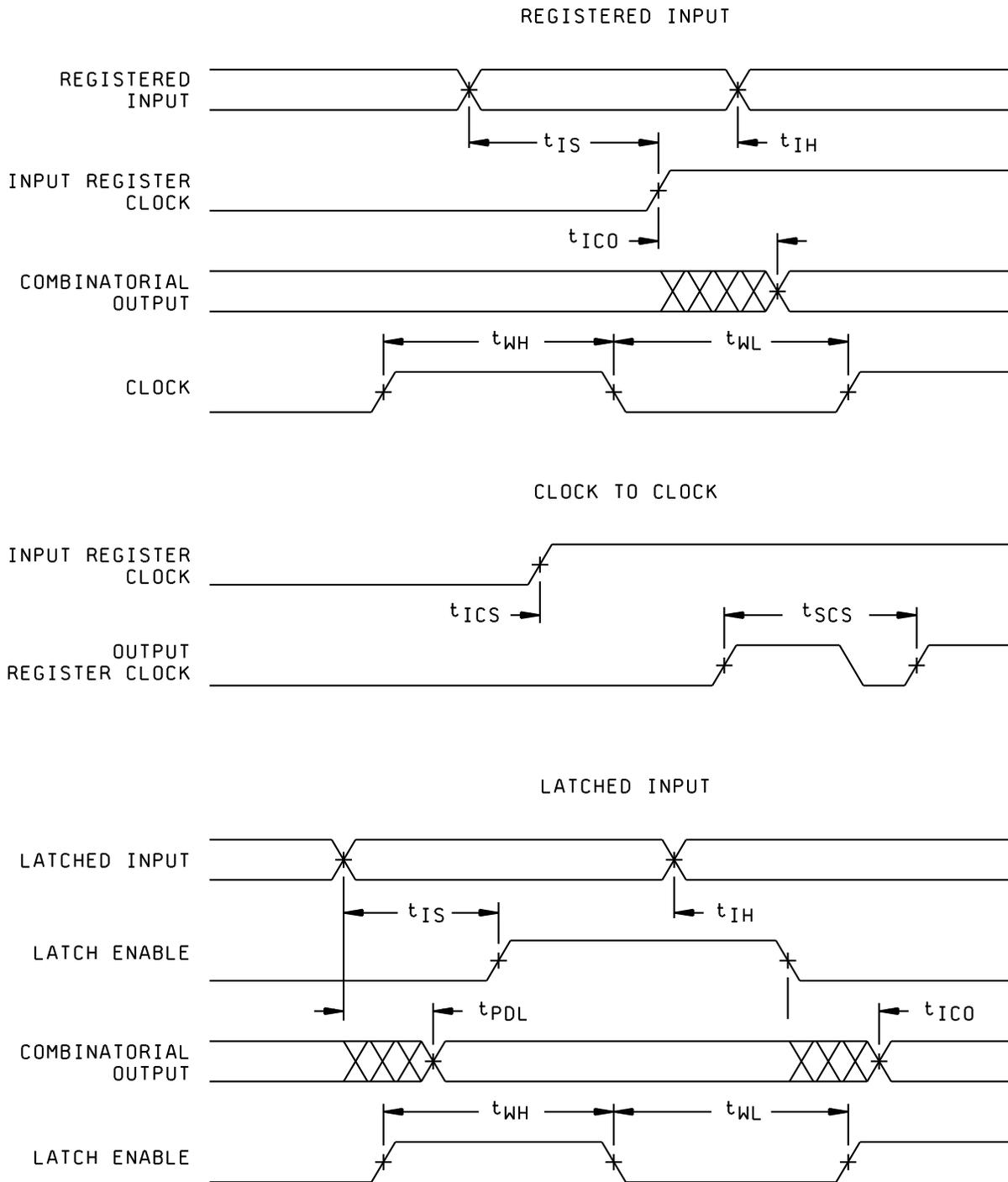
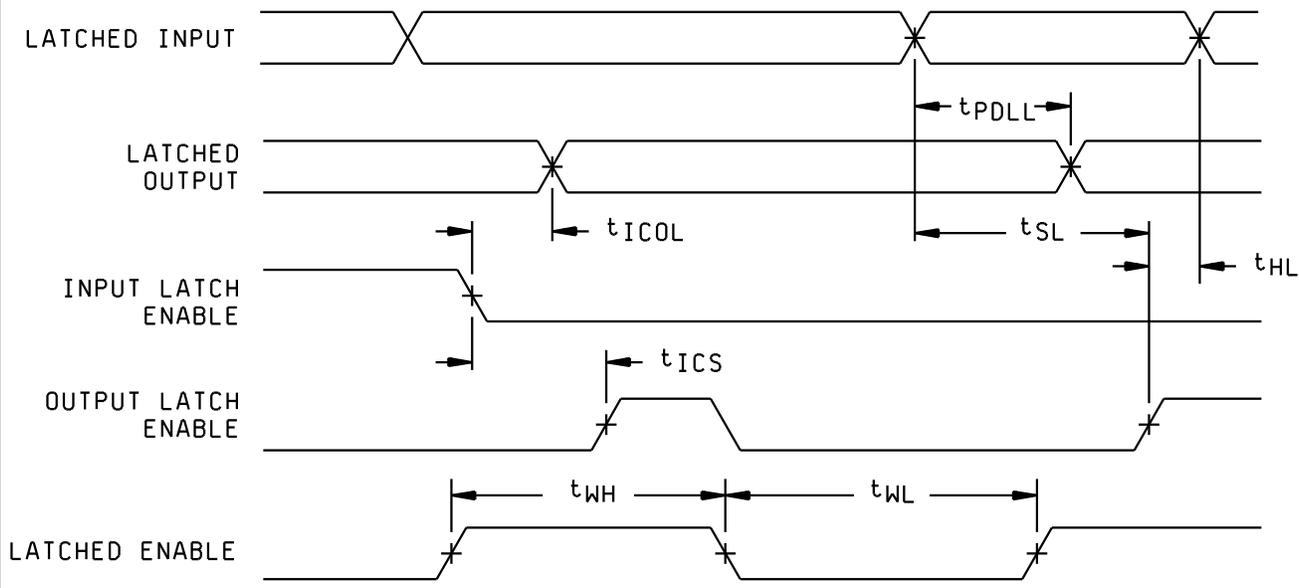


FIGURE 3. Switching waveforms - Continued.

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LATCHED INPUT AND OUTPUT



ASYNCHRONOUS RESET

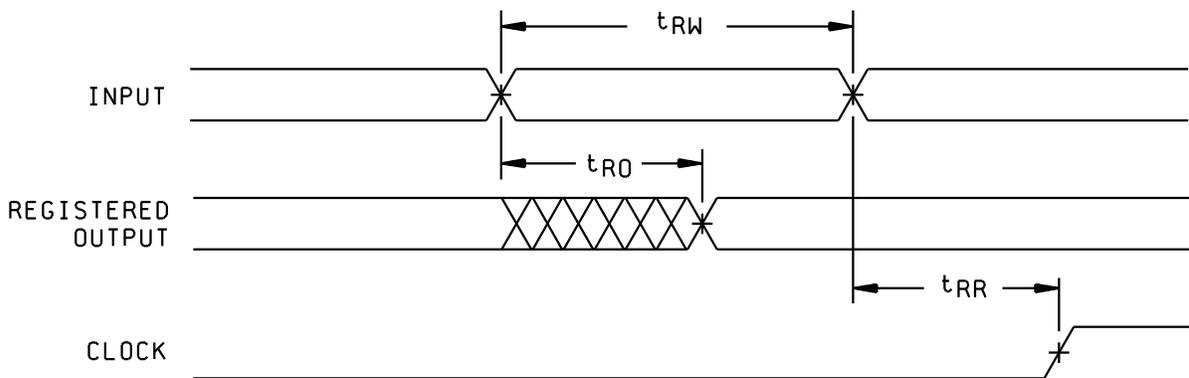


FIGURE 3. Switching waveforms - Continued.

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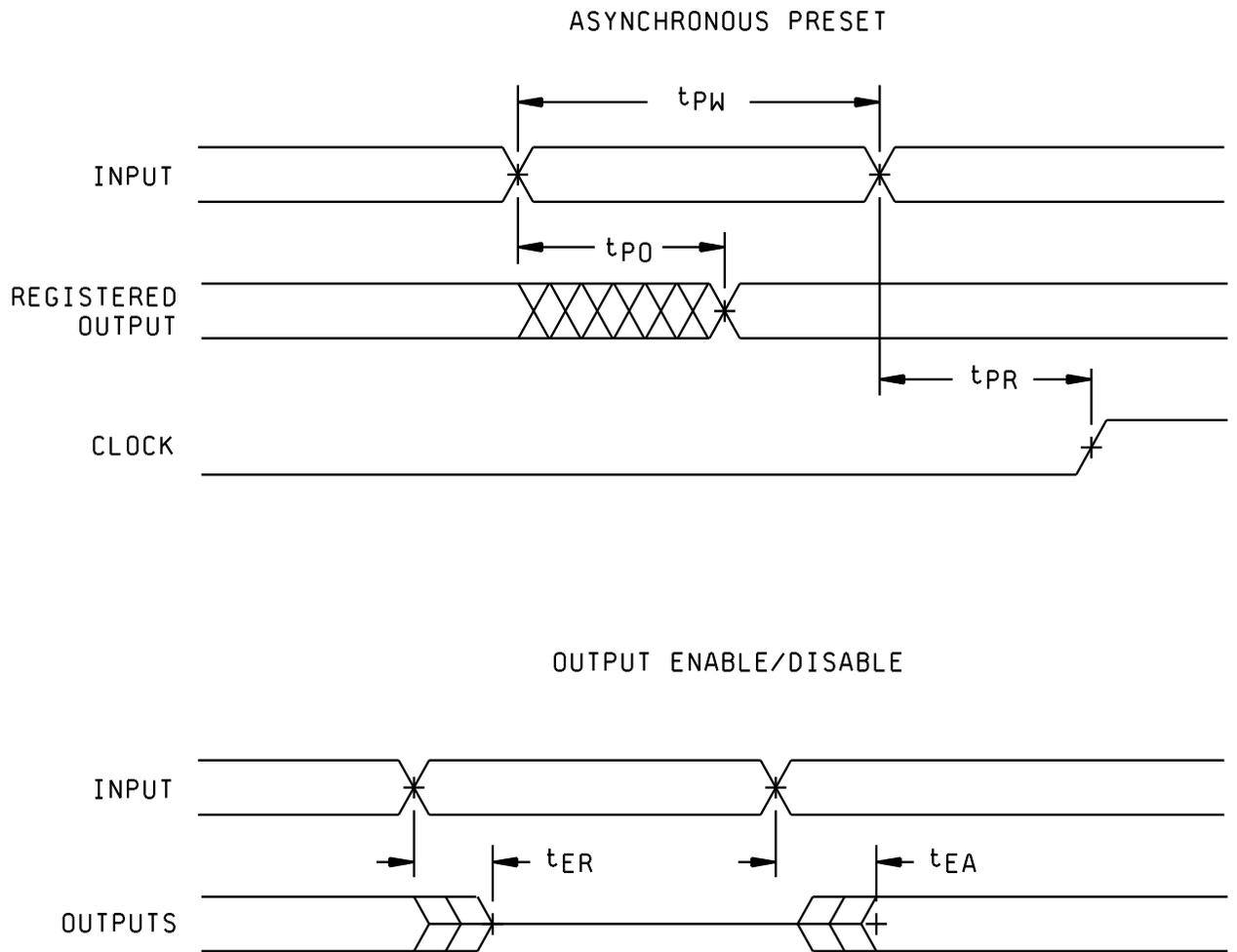
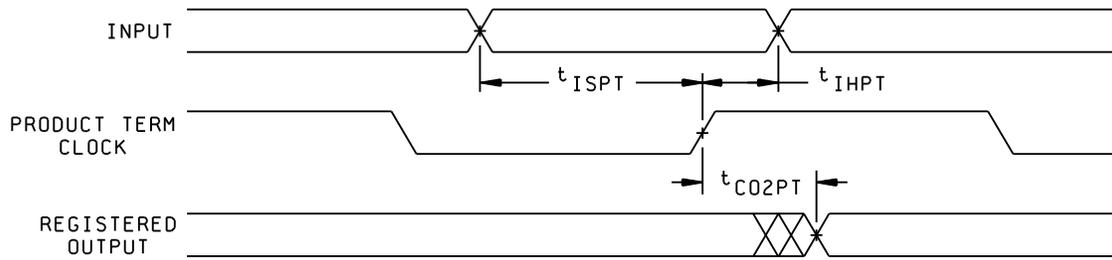


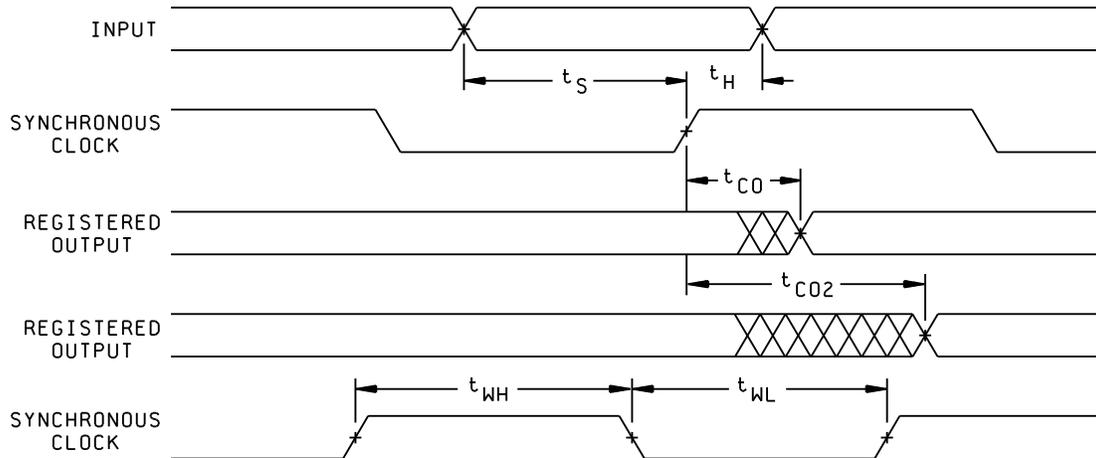
FIGURE 3. Switching waveforms - Continued.

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REGISTERED OUTPUT WITH PRODUCT TERM CLOCKING
INPUT COMING FROM ADJACENT BURIED REGISTER



REGISTERED OUTPUT WITH SYNCHRONOUS CLOCKING



REGISTERED OUTPUT WITH PRODUCT TERM CLOCKING
INPUT GOING THROUGH THE ARRAY

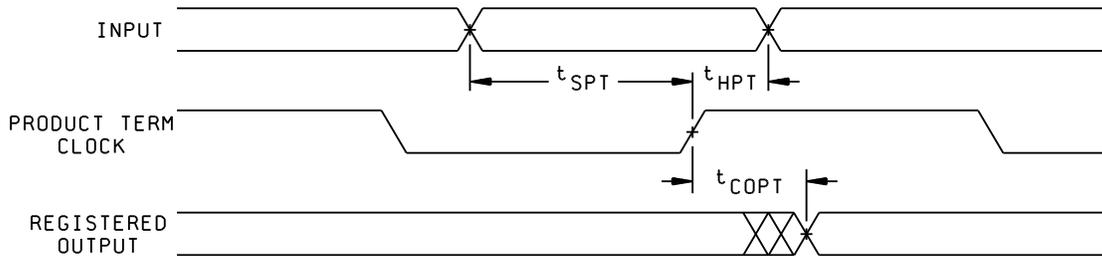


FIGURE 3. Switching waveforms - Continued.

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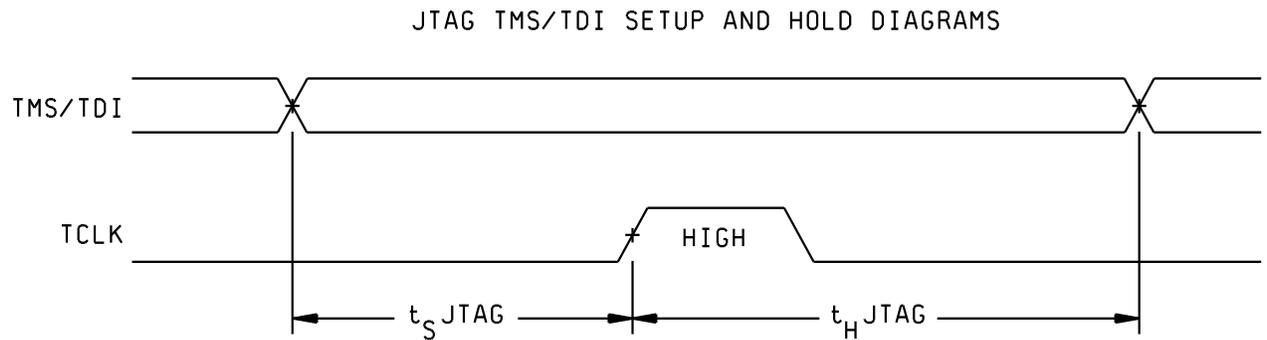
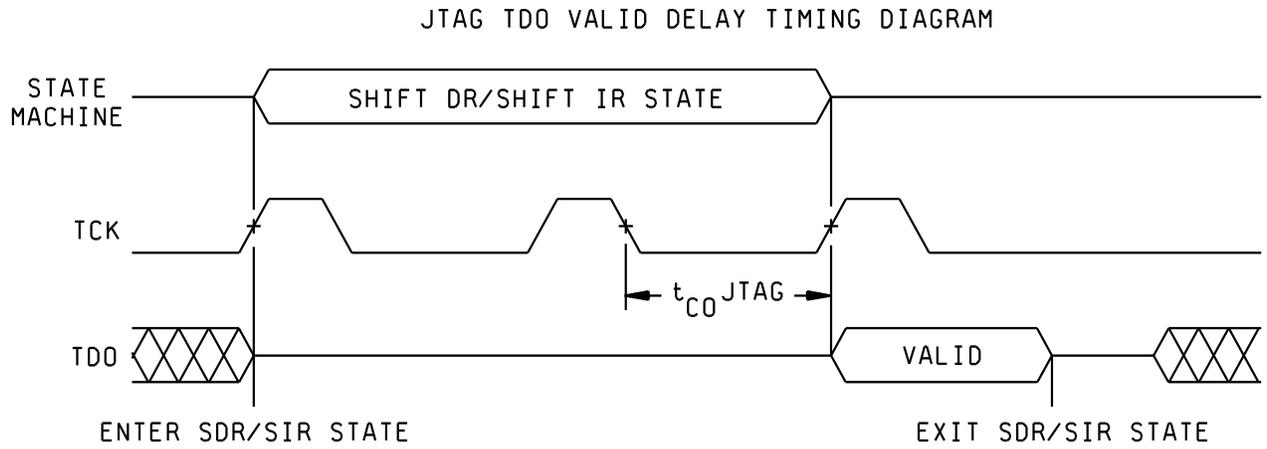


FIGURE 3. Switching waveforms - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device classes Q and V subgroups 7, 8A and 8B shall include verifying the functionality of the device.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC JESD78 may be used for reference.
- e. Subgroup 4 (C_{IN} , C_{OUT} , and C_{DP} measurements) shall be measured only for initial qualification and after any process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is three devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical Parameters (see 4.2)			1,7,9 or 2,8A,10
2	Static burn-in (method 1015)	Not Required	Not Required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
6	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
7	Group C end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
8	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
9	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I _{oz}	±10% of the specified value in table I
I _{ix}	±10% of the specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

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4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Erasure procedures. Erasure procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-11-12

Approved sources of supply for SMD 5962-99522 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9952201QYA	<u>3/</u>	CY37128VP84-83YMB

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply. The last known source is listed below.

Vendor CAGE number

65786

Vendor name and address

Cypress Semiconductor
 198 Champion Court
 San Jose, CA 95134-1709

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.