REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make change to 3.2.3 and add 1.5. Delete the radiation exposure circuit as specified under figure 2. - ro	00-12-20	R. MONNIN
B	Make change to the subgroups 8A and 8B limits on the Overshoot test as specified under table I. - ro	02-07-18	R. MONNIN
C	Delete 4.4.4.1.1, Accelerated aging test. - ro	08-06-03	R. HEBER
D	To make the title generic, delete the words “Radiation hardened” from the title block and paragraph 1.2.2. Delete footnote 2/ from Table IIA final electricals row. Add one footnote to Table IIB. Add CAGE code 60264. - ro	11-06-09	C. SAFFLE
E	Update drawing to current MIL-PRF-38535 requirements. Removed class M references. -rrp	16-08-09	C. SAFFLE

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
RAYMOND MONNIN

DRAWING APPROVAL DATE
00-05-09

MICROCIRCUIT, LINEAR, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
E	A	**67268**	**5962-99515**

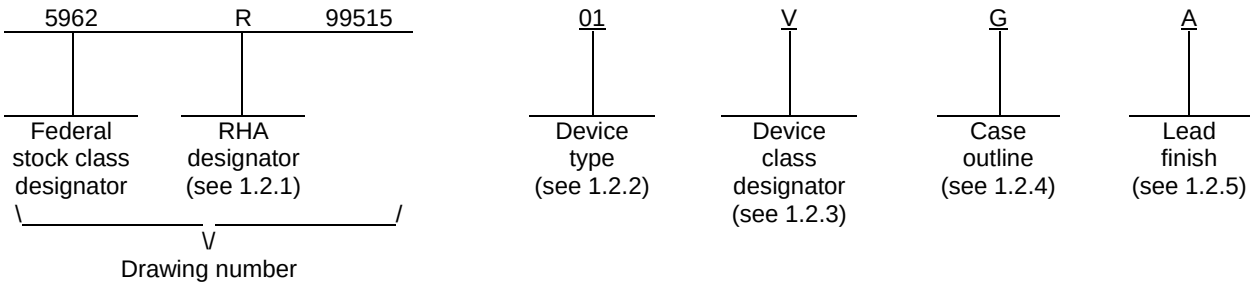
SHEET 1 OF 12

DSCC FORM 2233
APR 97

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LM101A	Operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
G	MACY1-X8	8	Can
H	GDFP1-F10 or CDFP2-F10	10	Flat pack
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	±22 V
Differential input voltage	±30 V
Input voltage (V_{IN})	±15 V 2/
Output short circuit duration	Continuous 3/
Power dissipation (P_D):	
Case G	750 mW (still air)
	1200 mW (500 linear feet per minute air flow)
Case H	500 mW (still air)
	800 mW (500 linear feet per minute air flow)
Case P	1000 mW (still air)
	1500 mW (500 linear feet per minute air flow)
Junction temperature (T_J)	+150°C
Storage temperature range	$-65°C \le T_A \le +150°C$
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case G	39°C/W
Cases H and P	26°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case G	165°C/W (still air)
	89°C/W (500 linear feet per minute air flow)
Case H	233°C/W (still air)
	155°C/W (500 linear feet per minute air flow)
Case P	128°C/W (still air)
	75°C/W (500 linear feet per minute air flow)

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	±20 V
Ambient operating temperature range (T_A)	$-55°C \le T_A \le +125°C$

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	100 krads (Si) 4/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

3/ The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J maximum, θ_{JA} maximum, and T_A. The maximum allowable power dissipation at any temperature is P_D max = (T_J max – T_A) / θ_{JA} or the number given in the absolute maximum ratings, whichever is lower.

4/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input offset voltage	V_{IO}	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V,		1	01	-2	+2	mV
		V_{CM} = -15 V		2,3		-3	+3	
			M,D,P,L,R	1		-2	+2	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V,		1		-2	+2	
		V_{CM} = +15 V		2,3		-3	+3	
			M,D,P,L,R	1		-2	+2	
		V_{CM} = 0 V		1		-2	+2	
				2,3		-3	+3	
			M,D,P,L,R	1		-2	+2	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V,		1		-2	+2	
		V_{CM} = 0 V		2,3		-3	+3	
			M,D,P,L,R	1		-2	+2	
Input offset current	I_{IO}	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V,		1,2	01	-10	+10	nA
		V_{CM} = -15 V, R_S = 100 kΩ		3		-20	+20	
			M,D,P,L,R	1		-10	+10	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V,		1,2		-10	+10	
		V_{CM} = +15 V, R_S = 100 kΩ		3		-20	+20	
			M,D,P,L,R	1		-10	+10	
		V_{CM} = 0 V, R_S = 100 kΩ		1,2		-10	+10	
				3		-20	+20	
			M,D,P,L,R	1		-10	+10	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V,		1,2		-10	+10	
		V_{CM} = 0 V, R_S = 100 kΩ		3		-20	+20	
			M,D,P,L,R	1		-10	+10	
Input bias current	$+I_{IB}$	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V,		1,2	01	-0.1	75	nA
		V_{CM} = -15 V, R_S = 100 kΩ		3		-0.1	100	
			M,D,P,L,R	1		-0.1	75	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V,		1,2		-0.1	75	
		V_{CM} = +15 V, R_S = 100 kΩ		3		-0.1	100	
			M,D,P,L,R	1		-0.1	75	
		V_{CM} = 0 V, R_S = 100 kΩ		1,2		-0.1	75	
				3		-0.1	100	
			M,D,P,L,R	1		-0.1	75	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input bias current	$+I_{IB}$	$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V,	1,2	01	-0.1	75	nA
		V_{CM} = 0 V, R_S = 100 kΩ	3		-0.1	100	
		M,D,P,L,R	1		-0.1	75	
Input bias current	$-I_{IB}$	$+V_{CC}$ = 35 V, $-V_{CC}$ = -5 V,	1,2	01	-0.1	75	nA
		V_{CM} = -15 V, R_S = 100 kΩ	3		-0.1	100	
		M,D,P,L,R	1		-0.1	75	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -35 V,	1,2		-0.1	75	
		V_{CM} = +15 V, R_S = 100 kΩ	3		-0.1	100	
		M,D,P,L,R	1		-0.1	75	
		V_{CM} = 0 V, R_S = 100 kΩ	1,2		-0.1	75	
			3		-0.1	100	
		M,D,P,L,R	1		-0.1	75	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = -5 V,	1,2		-0.1	75	
		V_{CM} = 0 V, R_S = 100 kΩ	3		-0.1	100	
		M,D,P,L,R	1		-0.1	75	
Power supply rejection ratio	+PSRR	$+V_{CC}$ = 10 V, $-V_{CC}$ = -20 V	1	01	-50	+50	μV/V
			2,3		-100	+100	
		M,D,P,L,R	1		-50	+50	
	-PSRR	$+V_{CC}$ = 20 V, $-V_{CC}$ = -10 V	1		-50	+50	
			2,3		-100	+100	
		M,D,P,L,R	1		-50	+50	
Common mode rejection ratio	CMRR	$\pm V_{CC}$ = ±35 V to ±5 V,	1,2,3	01	80		dB
		V_{CM} = ±15 V M,D,P,L,R	1		80		
Adjustment for input offset voltage	$+V_{IOADJ}$		1,2,3	01	4		mV
		M,D,P,L,R	1		4		
	$-V_{IOADJ}$		1,2,3			-4	
		M,D,P,L,R	1			-4	
Output short circuit current	$+I_{OS}$	$+V_{CC}$ = 15 V, $-V_{CC}$ = -15 V, $t \le 25$ ms, V_{CM} = -15 V	1,2,3	01	-60		mV
		M,D,P,L,R	1		-60		
	$-I_{OS}$	$+V_{CC}$ = 15 V, $-V_{CC}$ = -15 V, $t \le 25$ ms, V_{CM} = +15 V	1,2,3			+60	
		M,D,P,L,R	1			+60	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply current	I_{CC}	$+V_{CC}$ = 15 V, $-V_{CC}$ = -15 V	1	01		3	mA
			2			2.32	
			3			3.5	
		M,D,P,L,R	1			3	
Temperature 4/ coefficient of input offset voltage	ΔV_{IO} / ΔT	$+25°C \le T_A \le +125°C$	2	01	-15	+15	µV/°C
		$+25°C \le T_A \le -55°C$	3		-18	+18	
Temperature 4/ coefficient of input offset current	ΔI_{IO} / ΔT	$+25°C \le T_A \le +125°C$	2	01	-100	+100	pA/°C
		$+25°C \le T_A \le -55°C$	3		-200	+200	
Large signal (open 5/ loop) voltage gain	$-A_{VS}$	V_{OUT} = -15 V, R_1 = 2 kΩ	4	01	50		V/mV
			5,6		25		
		V_{OUT} = -15 V, R_1 = 10 kΩ	4		50		
			5,6		25		
	$+A_{VS}$	V_{OUT} = +15 V, R_1 = 2 kΩ	4		50		
			5,6		25		
		V_{OUT} = +15 V, R_1 = 10 kΩ	4		50		
			5,6		25		
Large signal (open 5/ loop) voltage gain	AVS	V_{CC} = ±5 V, R_1 = 2 kΩ, V_{OUT} = ±2 V	4,5,6	01	10		V/mV
		V_{CC} = ±5 V, R_1 = 10 kΩ, V_{OUT} = ±2 V			10		
Output voltage swing	$+V_{OP}$	V_{CM} = -20 V, R_1 = 10 kΩ	4,5,6	01	+16		V
		V_{CM} = -20 V, R_1 = 2 kΩ			+15		
	$-V_{OP}$	V_{CM} = 20 V, R_1 = 10 kΩ				-16	
		V_{CM} = 20 V, R_1 = 2 kΩ				-15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Slew rate	+SR	V_{IN} = -5 V to +5 V,	7,8A	01	0.3		V/μs
		A_V = 1	8B		0.2		
	-SR	V_{IN} = +5 V to –5 V,	7,8A		0.3		
		A_V = 1	8B		0.2		
Overshoot	OS	V_{IN} = 50 mV, A_V = 1	7	01		25	%
			8A,8B			35	
Rise time	TR	V_{IN} = 50 mV, A_V = 1	7,8A,8B	01		800	ns
Noise broadband	BB	BW = 10 Hz to 5 kHz, R_S = 0 Ω	7	01		15	μVrms
Noise popcorn	PC	BW = 10 Hz to 5 kHz, R_S = 100 kΩ	7	01		80	μV_{PK}

1/ Unless otherwise specified, $\pm V_{CC} = \pm 20$ V, V_{CM} = 0 V, R_S = 50 Ω.

2/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, R of irradiation. However, this device is only tested at the “R” level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.

4/ Calculated parameter.

5/ Datalog reading of K = V/mV.

Device type	01		
Case outlines	G	H	P
Terminal number	Terminal symbol		
1	BALANCE	NC	BALANCE / COMPENSATION
2	-INPUT	BALANCE	-INPUT
3	+INPUT	-INPUT	+INPUT
4	$-V_{CC}$	+INPUT	$-V_{CC}$
5	BALANCE	$-V_{CC}$	BALANCE
6	OUTPUT	BALANCE	OUTPUT
7	$+V_{CC}$	OUTPUT	$+V_{CC}$
8	NC	$+V_{CC}$	COMPENSATION
9	---	COMPENSATION	---
10	---	NC	---

NC = No connection

FIGURE 1. Terminal connections.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---
Final electrical parameters (see 4.2)	1,2,3,4,5, 1/ 6,7	1,2,3,4, 1/ 5,6,7,8A,8B
Group A test requirements (see 4.4)	1,2,3,4,5,6,7	1,2,3,4,5,6, 7,8A,8B
Group C end-point electrical parameters (see 4.4)	1	1,2,3 2/
Group D end-point electrical parameters (see 4.4)	1	1,2,3
Group E end-point electrical parameters (see 4.4)	1	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and delta limits shall be computed with reference to the previous endpoint electrical parameters.

TABLE IIB. Delta parameters. 1/

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
Input offset voltage	V_{IO}	V_{CM} = 0 V	-0.5	0.5	mV
Input bias current	$+I_{IB}$	V_{CM} = 0 V, R_S = 100 kΩ	-7.5	7.5	nA
Input bias current	$-I_{IB}$	V_{CM} = 0 V, R_S = 100 kΩ	-7.5	7.5	nA

1/ Deltas are performed at room temperature, T_A = +25°C, at life test.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.2 Dose rate burnout. When required by the customer, test shall be performed on devices, SEC, or approved test structures at technology qualifications and after any design or process changes which may effect the RHA capability of the process. Dose rate burnout shall be performed in accordance with test method 1023 of MIL-STD-883 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-08-09

Approved sources of supply for SMD 5962-99515 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9951501QGA	57300	MTLM101AQH
5962-9951501QPA	57300	MTLM101AQD8
5962-9951501VGA	3/	LM101AH-QMLV
5962-9951501VHA	3/	LM101AW-QMLV
5962-9951501VPA	3/	LM101AJ-QMLV
5962L9951501VGA	27014	LM101AHLQMLV
5962L9951501VHA	27014	LM101AWLQMLV
5962L9951501VPA	27014	LM101AJLQMLV
5962R9951501QGA	3/	LM101AHRQML
5962R9951501VGA	3/	LM101AHRQMLV
5962R9951501QHA	3/	LM101AWRQML
5962R9951501VHA	3/	LM101AWRQMLV
5962R9951501QPA	3/	LM101AJRQML
5962R9951501VPA	3/	LM101AJRQMLV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243
57300	Micross Components 7725 N. Orange Blossom Trail Orlando, FL 32810-2696