REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to TR(tr), TR(os), SR+, SR-, NI(BB), NI(PC), CS tests as specified in table I , 1.5, 4.4.1b, and table II. - ro	99-10-20	R. Monnin
B	Add test conditions to the input offset voltage temperature sensitivity test and the input offset current temperature sensitivity test in table I. Make changes to the title in table IIB. Editorial changes throughout. - rrp	99-11-17	R. Monnin
C	Add radiation hardened level "L" devices and delete figures 1 and 3. - ro	02-06-13	R. Monnin
D	Make change to input offset voltage post irradiation limits as specified under table I. - ro	03-10-15	R. Monnin
E	Add device type 02 tested at low dose rate. Make changes to 1.2.2, 1.5, Table I, Table IIB, Figure I, and 4.4.4.1. - ro	06-06-09	R. Monnin
F	Delete the 50 krads reference for device type 01 under paragraph 1.5. Change the dose rate from "12 mrads(Si) / s" to "10 mrads (Si) / s" for device type 02 under paragraph 1.5. Also under paragraph 1.5, third line of the paragraph, after method 1019, add the words, "condition D". Make changes to footnote 1/ as specified under Table I. - ro	08-03-11	R. Heber
G	Add paragraph 3.1.1 and appendix A. -rrp	08-11-03	R. Heber
H	Under Table I conditions column, V_{IO}, I_{IO}, $+I_{IB}$, $-I_{IB}$, $\Delta V_{IO} / \Delta T$, $\Delta I_{IO} / \Delta T$, and +PSRR tests, make polarity changes to V_{CM} limits. Under Table IIB, footnote 1/, delete "V_{CM} = -15 V" and substitute "V_{CM} = +15 V". Delete paragraphs 4.4.4.1.1 and 4.4.4.2. - ro	10-10-18	C. Saffle
J	Add device type 03. - drw	11-01-04	C Saffle
K	Sheet 13, table IIA, add subgroups 4, 5, 6, 7, 8A and 8B for group C and D end-point electrical parameters for device type 03. - drw	11-03-25	C Saffle
L	Update paragraphs to MIL-PRF-38535 requirements. - drw	19-08-02	Charles F. Saffle

REV																				
SHEET																				
REV	L	L	L	L	L	L	L	L	L											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	L	L	L	L	L	L	L	L	L	L	L	L	L	L
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
98-11-06

REVISION LEVEL
L

MICROCIRCUIT, LINEAR, RADIATION HARDENED, QUAD OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

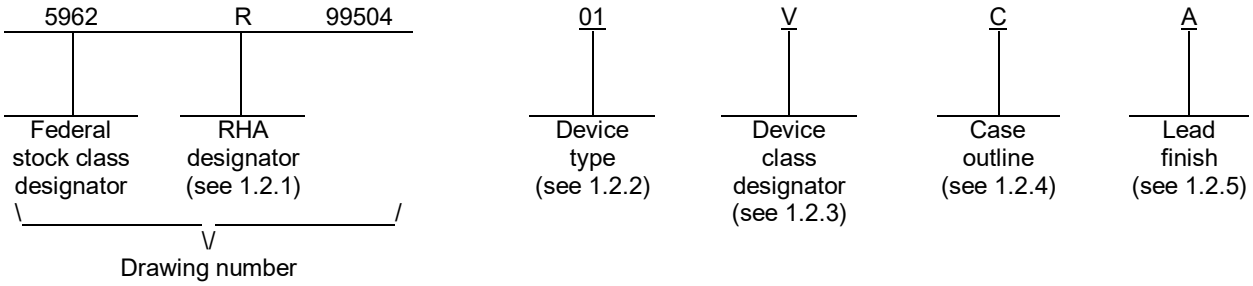
SIZE	CAGE CODE	
A	**67268**	**5962-99504**

SHEET 1 OF 23

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LM124A	Quad, operational amplifier
02	LM124A	Quad, operational amplifier
03	LM124A	Quad, operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
Z	GDFP1-G14	14	Flat pack with gull wing leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (+V_{CC})	32 V dc or ±16 V dc
Input voltage range	-0.3 V dc to +32 V dc
Differential input voltage	32 V dc
Input current (V_{IN} < -0.3 V dc)	50 mA 2/
Power dissipation: 3/	
Case C	1260 mW
Cases D and Z	700 mW
Storage temperature range	-65°C to +150°C
Output short-circuit to GND: 4/	
(One amplifier, +V_{CC} ≤ 15 V dc and T_A = 25°C)	Continuous
Lead temperature (soldering, 10 seconds)	260°C
Maximum junction temperature (T_J)	150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case C	19°C/W
Cases D and Z	18°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case C	103°C/W (still air) 51°C/W (500 LF/min air flow)
Cases D and Z	176°C/W (still air) 116°C/W (500 LF/min air flow)

1.4 Recommended operating conditions.

Supply voltage range	±5 V to ±15 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the operational amplifiers to go to the +V_{CC} voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than –0.3 V dc at 25°C.

3/ The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J, θ_{JA}, and T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J - T_A) / \theta_{JA}$ or the number given in 1.3 herein, whichever is lower.

4/ Short circuits from the output to +V_{CC} can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of +V_{CC}. At values of supply voltage in excess of +15 V dc, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

1.5 Radiation features.

Device type 01:
Maximum total dose available (dose rate = 50 – 300 rads(Si) / s)
RHA designator R ..... 100 krads (Si) 5/
Device type 02:
Maximum total dose available (dose rate = 10 mrads(Si) / s)
RHA designator R ..... 100 krads (Si) 6/

The manufacturer supplying RHA parts on this drawing has completed Lot Acceptance testing at Low Dose Rate (10 mrad/s) on these RHA marked parts. The Low Does Rate (LDR) testing that was performed demonstrates that these parts from the lot tested do not have an Enhanced Low Dose rate Sensitivity as defined by Method 1019, condition D. Lot Acceptance Testing at LDR will continue to be performed on each wafer or wafer lot until characterization testing has been performed in accordance with Method 1019 of MIL-STD-883. Since the redesigned part did not demonstrate ELDRS per Method 1019 and the previously tested device was ELDRS, the part number will be changed to an 02 device to distinguish the two parts.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

5/ For device type 01, these parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, test method 1019, condition A.
6/ For device type 02, these parts have been tested and do not demonstrate low dose rate sensitivity. Radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, test method 1019, condition D.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V_{IO}	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, V_{CM} = +15 V	1	01, 02	-2	2	mV
				03	-3	3	
			2, 3	01, 02	-4	4	
				03	-5	5	
		M, D, P, L, R	1	01, 02	-2.5	2.5	
		$+V_{CC}$ = 2 V, $-V_{CC}$ = -28, V_{CM} = -13 V	1	01, 02	-2	2	mV
				03	-3	3	
			2, 3	01, 02	-4	4	
				03	-5	5	
		M, D, P, L, R	1	01, 02	-2.5	2.5	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = GND, V_{CM} = +1.4 V	1	01, 02	-2	2	mV
				03	-3	3	
			2, 3	01, 02	-4	4	
				03	-5	5	
		M, D, P, L, R	1	01, 02	-2.5	2.5	
		$+V_{CC}$ = 2.5 V, $-V_{CC}$ = -2.5, V_{CM} = -1.1 V	1	01, 02	-2	2	mV
				03	-3	3	
			2, 3	01, 02	-4	4	
				03	-5	5	
		M, D, P, L, R	1	01, 02	-2.5	2.5	
Input offset current	I_{IO}	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, V_{CM} = +15 V	1, 2	01, 02	-10	10	nA
			3		-30	30	
		M, D, P, L, R	1		-15	15	
			1	03	-10	10	
			2, 3		-30	30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input offset current	I_{IO}	$+V_{CC}$ = 2 V, $-V_{CC}$ = -28, V_{CM} = -13 V		1, 2	01, 02	-10	10	nA
				3		-30	30	
			M, D, P, L, R	1		-15	15	
				1	03	-10	10	
				2, 3		-30	30	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = GND, V_{CM} = +1.4 V		1, 2	01, 02	-10	10	nA
				3		-30	30	
			M, D, P, L, R	1		-15	15	
				1	03	-10	10	
				2, 3		-30	30	
		$+V_{CC}$ = 2.5 V, $-V_{CC}$ = -2.5, V_{CM} = -1.1 V		1, 2	01, 02	-10	10	nA
				3		-30	30	
			M, D, P, L, R	1		-15	15	
				1	03	-10	10	
				2, 3		-30	30	
Input bias current	$+I_{IB}$	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, V_{CM} = +15 V		1, 2	01, 02	-50	+0.1	nA
				3		-100	+0.1	
			M, D, P, L, R	1		-75	+0.1	
				1	03	-85	+0.1	
				2, 3		-100	+01	
		$+V_{CC}$ = 2 V, $-V_{CC}$ = -28, V_{CM} = -13 V		1, 2	All	-50	+0.1	nA
				3		-100	+0.1	
			M, D, P, L, R	1	01, 02	-75	+0.1	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = GND, V_{CM} = +1.4 V		1, 2	All	-50	+0.1	nA
				3		-100	+0.1	
			M, D, P, L, R	1	01, 02	-75	+0.1	
		$+V_{CC}$ = 2.5 V, $-V_{CC}$ = -2.5 V, V_{CM} = -1.1 V		1, 2	All	-50	+0.1	nA
				3		-100	+0.1	
			M, D, P, L, R	1	01, 02	-75	+0.1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input bias current	$-I_{IB}$	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, V_{CM} = +15 V		1, 2	01, 02	-50	+0.1	nA
				3		-100	+0.1	
			M, D, P, L, R	1		-75	+0.1	
				1	03	-85	+0.1	
				2, 3		-100	+0.1	
		$+V_{CC}$ = 2 V, $-V_{CC}$ = -28 V, V_{CM} = -13 V		1, 2	All	-50	+0.1	nA
				3		-100	+0.1	
			M, D, P, L, R	1	01, 02	-75	+0.1	
		$+V_{CC}$ = 5 V, $-V_{CC}$ = GND, V_{CM} = +1.4 V		1, 2	All	-50	+0.1	nA
				3		-100	+0.1	
			M, D, P, L, R	1	01, 02	-75	+0.1	
		$+V_{CC}$ = 2.5 V, $-V_{CC}$ = -2.5 V, V_{CM} = -1.1 V		1, 2	All	-50	+0.1	nA
				3		-100	+0.1	
			M, D, P, L, R	1	01, 02	-75	+0.1	
Power supply rejection ratio	+PSRR	$-V_{CC}$ = GND, V_{CM} = +1.4 V, 5 V $\le V_{CC} \le$ 30 V		1, 2, 3	All	-100	100	µV/V
Common mode rejection ratio	CMRR			1, 2, 3	All	76		dB
Output short circuit current	I_{OS+}	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, V_{OUT} = 25 V		1, 2, 3	All	-70		mA
Power supply current	I_{CC}	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND		1, 2	All		3	mA
				3			4	
Input offset voltage temperature sensitivity	ΔV_{IO} / ΔT	$+V_{CC}$ = 5 V, $-V_{CC}$ = GND, V_{CM} = +1.4 V 3/, 4/		2, 3	All	-30	30	µV/°C
Input offset current temperature sensitivity	ΔI_{IO} / ΔT	$+V_{CC}$ = 5 V, $-V_{CC}$ = GND, V_{CM} = +1.4 V 3/, 4/		2	All	-400	400	pA/°C
				3		-700	700	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logical "0" output voltage	V_{OL}	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, R_L = 10 kΩ	4, 5, 6	All		35	mV
		$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, I_{OL} = 5 Ma	4, 5, 6	All		1.5	V
		$+V_{CC}$ = 4.5 V, $-V_{CC}$ = GND, I_{OL} = 2 μA	4, 5, 6	All		0.4	V
Logical "1" output voltage	V_{OH}	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, I_{OH} = -10 mA	4, 5, 6	All	27		V
		$+V_{CC}$ = 4.5 V, $-V_{CC}$ = GND, I_{OH} = -10 mA	4, 5, 6	All	2.4		V
Voltage gain	A_{VS+}	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, 1 V ≤ V_{OUT} ≤ 26 V, R_L = 10 kΩ	4	All	50		V/mV
			5, 6		25		
		M, D, P, L, R	1	01, 02	40		
		$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, 5 V ≤ V_{OUT} ≤ 20 V, R_L = 2 kΩ	4	All	50		V/mV
			5, 6		25		
		M, D, P, L, R	1	01, 02	40		
Voltage gain	A_{VS}	$+V_{CC}$ = 5 V, $-V_{CC}$ = GND, 1 V ≤ V_{OUT} ≤ 2.5 V, R_L = 10 kΩ	4, 5, 6	All	10		V/mV
		$+V_{CC}$ = 5 V, $-V_{CC}$ = GND, 1 V ≤ V_{OUT} ≤ 2.5 V, R_L = 2 kΩ	4, 5, 6	All	10		
Maximum output voltage swing	$+V_{OP}$	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, V_{OUT} = +30 V, R_L = 10 kΩ	4, 5, 6	All	27		V
		$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, V_{OUT} = +30 V, R_L = 2 kΩ	4, 5, 6	All	26		V
Transient response: rise time	TR(t_r)	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND 4/	7, 8A, 8B	All		1	μs
Transient response: overshoot	TR(os)	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND	7, 8A, 8B	01, 02		50	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Slew rate: rise	SR+	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND 4/	7, 8A, 8B	All	0.1		V/μs
Slew rate: fall	SR-	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND 4/	7, 8A, 8B	All	0.1		V/μs
Noise broadband	NI(BB)	$+V_{CC}$ = 15 V, $-V_{CC}$ = -15 V, BW = 10 Hz to 5 kHz 4/	7	All		15	μV/rms
Noise popcorn	NI(PC)	$+V_{CC}$ = 15 V, $-V_{CC}$ = -15 V, R_S = 20 kΩ, BW = 10 Hz to 5 kHz 4/	7	All		50	μV/peak
Channel separation	CS	$+V_{CC}$ = 30 V, $-V_{CC}$ = GND, R_L = 2 kΩ	7	All	80		dB
		V_{IN} = 1 V and 16 V, A to B R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, A to C R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, A to D R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, B to A R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, B to C R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, B to D R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, C to A R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, C to B R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, C to D R_L = 2 kΩ, 5/	7	All	80		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Channel separation	CS	V_{IN} = 1 V and 16 V, D to A R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, D to B R_L = 2 kΩ, 5/	7	All	80		dB
		V_{IN} = 1 V and 16 V, D to C R_L = 2 kΩ, 5/	7	All	80		dB

1/ RHA devices supplied to this drawing meet and are tested to all levels M, D, P, L, R of irradiation. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ The 01 device may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, test method 1019, condition A for device type 01. Device type 02, has been tested at low dose rate and does not demonstrate low dose rate sensitivity (see 1.5 herein).

3/ Calculated parameter.

4/ For device type 03, the parameter is guaranteed to the limit specified by characterization, but not production tested.

5/ $+V_{CC}$ = 30 V, $-V_{CC}$ = 0 V.

Device types	01, 02 and 03
Case outlines	C, D, and Z
Terminal number	Terminal symbol
1	OUTPUT 1
2	-INPUT 1
3	+INPUT 1
4	$+V_{CC}$
5	+INPUT 2
6	-INPUT 2
7	OUTPUT 2
8	OUTPUT 3
9	-INPUT 3
10	+INPUT 3
11	GND
12	+INPUT 4
13	-INPUT 4
14	OUTPUT 4

FIGURE 1. Terminal connections.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A for device type 01, condition D for device type 02 and as specified herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4 1/	1, 2, 3, 4, 1/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7, 8A, 8B
Group C end-point electrical parameters (see 4.4)	1	1, 2, 3, 4, 5, 6, 7, 8A, 8B 2/, 3/
Group D end-point electrical parameters (see 4.4)	1	1, 2, 3, 4, 5, 6, 7, 8A, 8B 3/
Group E end-point electrical parameters (see 4.4)	1	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters.
3/ Subgroups 4, 5, 6, 7, 8A and 8B applies for device type 03 only.

TABLE IIB. Operating life test delta parameters. T_A = +25°C. 1/

Parameter	Device types	Delta limit	
		Min	Max
V_{IO} 1/	01, 02	-0.5 mV	0.5 mV
$+I_{IB}$ 1/	01, 02	-10 nA	10 nA
	03	-16 nA	16 nA
$-I_{IB}$ 1/	01, 02	-10 nA	10 nA
	03	-16 nA	16 nA

1/ $+V_{CC}$ = 30 V, $-V_{CC}$ = GND, V_{CM} = +15 V.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

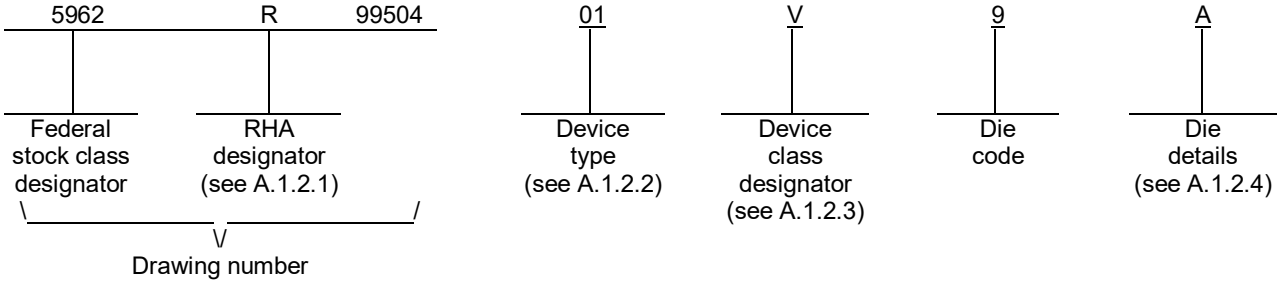
6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99504

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LM124A	Quad, operational amplifier
02	LM124A	Quad, operational amplifier
03	LM124A	Quad, operational amplifier

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02	A-1
03	B-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02	A-1
03	B-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02	A-1
03	B-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02	A-1
03	B-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1 and B-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1 and B-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1 and B-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 and 4.4.4.1 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

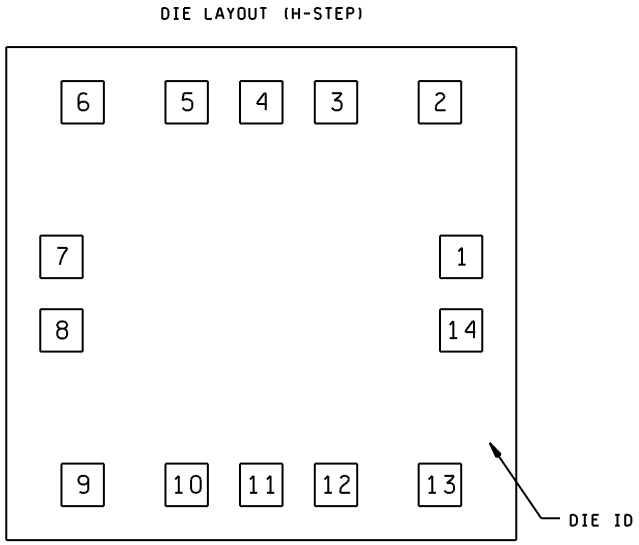
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



Die bonding pad locations and electrical functions

Die physical dimensions.
- Die size: 1346.2 μm x 1422.4 μm (53.0 mils x 56.0 mils)
- Die thickness: 330 μm nominal
- Pad size: 92 μm x 92 μm
- Minimum pitch: 127 μm

Interface materials.
- Top metallization: Al 0.5%Cu
- Backside metallization: Si (bare)

Glassivation.
- Type: Vapox over metal (VOM) only
- Thickness: 8 kÅ – 12 kÅ

Substrate: Silicon

Assembly related information.
- Substrate potential: Floating or GND
- Special assembly instructions: None

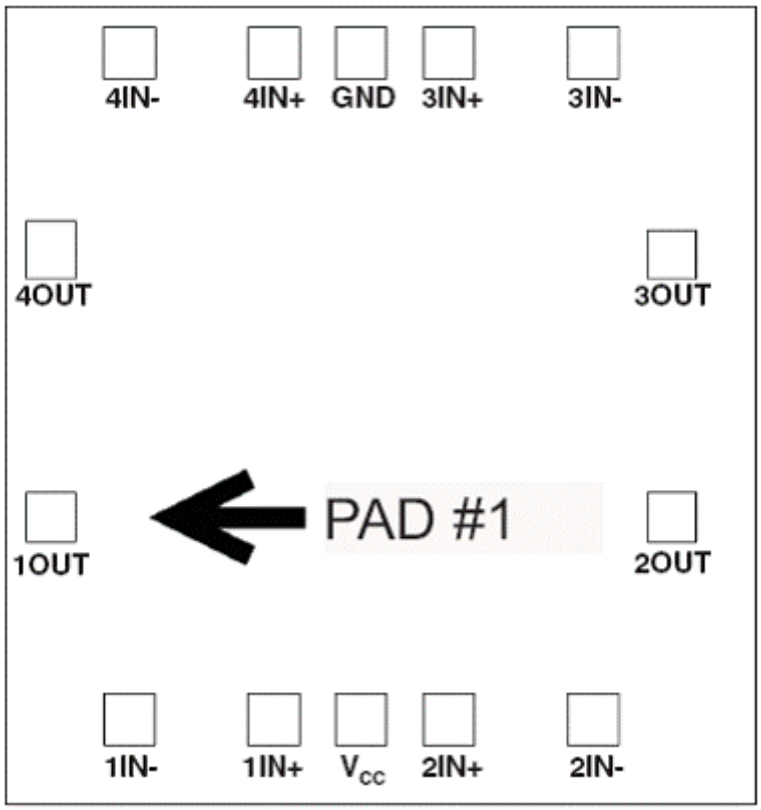
FIGURE A-1. Die bonding pad locations and electrical functions.

Die bonding pad locations measured in μm.

Pad number	Signal name	X	Y
1	Output 1	559	81
2	-Input 1	461	597
3	+Input 1	160	597
4	$+V_{CC}$	-29	597
5	+Input 2	-160	597
6	-Input 2	-461	597
7	Output 2	-559	81
8	Output 3	-559	-81
9	-Input 3	-461	-597
10	+Input 3	-160	-597
11	GND	7	-597
12	+Input 4	160	-597
13	-Input 4	461	-597
14	Output 4	559	-81

NOTE:
1. Die bonding pad locations are referenced to die center.

FIGURE A-1. Die bonding pad locations and electrical functions – continued.



Die bonding pad locations and electrical functions

Die physical dimensions.	
Die size:	1574.8 μm x 1447.8 μm (62.0 mils x 57.0 mils)
Die thickness:	15 mils
Interface materials.	
Top metallization:	AlCu 0.5%
Backside metallization:	Silicon with backgrind
Glassivation.	
Type:	Teos
Thickness:	7 kA
Substrate:	Silicon
Assembly related information.	
Backside potential:	Floating
Special assembly instructions:	None

FIGURE B-1. Die bonding pad locations and electrical functions.

BOND PAD COORDINATES (microns)

DESCRIPTION	PAD NUMBER	Xmin	Ymin	Xmax	Ymax
1OUT	1	426.72	1249.68	523.24	1346.20
1IN-	2	25.40	1093.47	127	1192.53
1IN+	3	25.40	808.99	127	910.59
Vcc	4	25.40	635	127	734.06
2IN+	5	25.40	462.28	127	563.88
2IN-	6	25.40	177.80	127	279.40
2OUT	7	426.72	25.40	523.24	121.92
3OUT	8	949.96	25.40	1046.48	121.92
3IN-	9	1346.20	177.80	1447.80	279.40
3IN+	10	1346.20	462.28	1447.80	563.88
GND	11	1346.20	635	1447.80	736.60
4IN+	12	1346.20	807.72	1447.80	909.32
4IN-	13	1346.20	1092.20	1447.80	1193.80
4OUT	14	949.96	1249.68	1046.48	1346.20

NOTE:
1. Die bonding pad locations are referenced to die center.

FIGURE B-1. Die bonding pad locations and electrical functions – continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-08-02

Approved sources of supply for SMD 5962-99504 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962L9950401VCA	3/	LM124AJLQMLV
5962L9950401VDA	3/	LM124AWLQMLV
5962L9950401VZA	3/	LM124AWGLQMLV
5962R9950401QCA	3/	LM124AJRQML
5962R9950401QDA	3/	LM124AWRQML
5962R9950401QZA	3/	LM124AWGRQML
5962R9950401VCA	01295	LM124AJRQMLV
5962R9950401VDA	01295	LM124AWRQMLV
5962R9950401VZA	01295	LM124AWGRQMLV
5962R9950401V9A	01295	LM124 MDR
5962R9950402VCA	01295	LM124AJRLQMLV
5962R9950402VDA	01295	LM124AWRLQMLV
5962R9950402VZA	01295	LM124AWGRLQMLV
5962R9950402V9A	01295	LM124 MDE
5962-9950403VCA	01295	LM124AJQMLV
5962-9950403V9B	01295	LM124AKGD-SP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243