REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update the boilerplate to the current requirements of MIL-PRF-38535. - jak	07-10-24	Thomas M. Hess
B	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. Delete class M requirement throughout. - LTG	14-03-20	Thomas M. Hess

REV																				
SHEET																				
REV	B																			
SHEET	15																			

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
98-09-18

REVISION LEVEL
B

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, HIGH SPEED CMOS, 4-TO-16 LINE DECODER/DEMULTIPLEXER, WITH INPUT LATCHES, MONOLITHIC SILICON

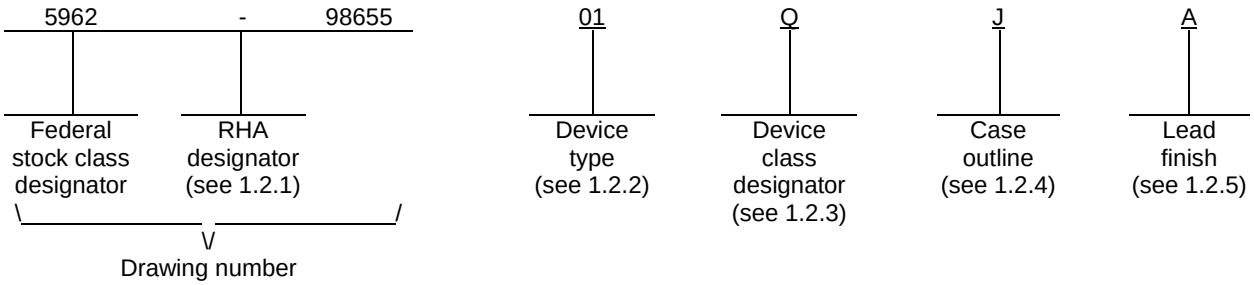
SIZE	CAGE CODE	
A	**67268**	**5962-98655**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC4514	4-to-16 line decoder/demultiplexer with input latches

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to VCC +0.5 V dc
DC input diode current (I_{IK}) ($V_{IN} < -0.5$ V or $V_{IN} > V_{CC} + 0.5$ V)	±20 mA
DC output diode current (I_{OK}) ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±20 mA
DC drain current, per output (I_{OUT}) (-0.5 V $< V_O < V_{CC} + 0.5$ V)	±25 mA
DC output source or sink current per output pin (I_{OUT}), ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} or ground current (I_{CC})	±50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+265°C
Thermal resistance, junction-to-case (Θ_{JC})	20°C/W
Thermal resistance, junction-to-ambient (Θ_{JA})	60°C/W
Junction temperature (T_J)	+175°C
Maximum package power dissipation at T_A = +125°C (P_D)	0.83 W 4/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Input voltage range, high (V_{IH}):	
V_{CC} = 2.0 V	1.5 V
V_{CC} = 4.5 V	3.15 V
V_{CC} = 6.0 V	4.2 V
Input voltage range, low (V_{IL}):	
V_{CC} = 2.0 V	0.5 V
V_{CC} = 4.5 V	1.35 V
V_{CC} = 6.0 V	1.8 V
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise or fall time (t_r, t_f):	
V_{CC} = 2.0 V	1000 ns
V_{CC} = 4.5 V	500 ns
V_{CC} = 6.0 V	400 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C unless otherwise noted.
4/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the following rate:

Case outline J	16.7 mW/°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD7 - Standard for Description of 54/74HCXXXXX and 54/74HCTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S Arlington, VA 22201-2107).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+2.0\ V \le V_{CC} \le +6.0\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 2/		Unit
					Min	Max	
High level output voltage	V_{OH}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OUT} = -20.0\ \mu A$	2.0 V 3/	1, 2, 3	1.9		V
			4.5 V		4.4		
			6.0 V 3/		5.9		
High level output voltage, TTL loads		For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OUT} = -4.0$ mA	4.5 V	1	3.98		
				2, 3	3.7		
		For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OUT} = -5.2$ mA	6.0 V 3/	1	5.48		
				2, 3	5.2		
Low level output voltage	V_{OL}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OUT} = +20.0\ \mu A$	2.0 V 3/	1, 2, 3		0.1	V
			4.5 V			0.1	
			6.0 V 3/			0.1	
Low level output voltage, TTL loads		For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OUT} = +4.0$ mA	4.5 V	1		0.26	
				2, 3		0.4	
		For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OUT} = +5.2$ mA	6.0 V 3/	1		0.26	
				2, 3		0.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+2.0\ V \le V_{CC} \le +6.0\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 2/		Unit
					Min	Max	
Input current high	I_{IH}	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND	6.0 V	1		+0.1	µA
				2, 3		+1.0	
Input current low	I_{IL}	For input under test, V_{IN} = GND For all other inputs, $V_{IN} = V_{CC}$ or GND	6.0 V	1		-0.1	µA
				2, 3		-1.0	
Quiescent supply current	I_{CC}	For all inputs, $V_{IN} = V_{CC}$ or GND I_{OUT} = 0.0 A	6.0 V	1		8.0	µA
				2, 3		160.0	
Input capacitance	C_{IN}	See 4.4.1c	0.0 V	4		10.0	pF
Functional test	4/	$V_{IN} = V_{IH}$ or V_{IL} Verify output V_{OUT} See 4.4.1b	2.0 V	7, 8	L	H	
			4.5 V				
			6.0 V				
$\overline{LE}$ pulse width	t_w 3/	See figure 4	2.0 V	9	75		ns
				10, 11	110		
			4.5 V	9	15		
				10, 11	22		
			6.0 V	9	13		
				10, 11	19		
Select to $\overline{LE}$ setup time, high or low	t_s 3/	See figure 4	2.0 V	9	100		ns
				10, 11	150		
			4.5 V	9	20		
				10, 11	30		
			6.0 V	9	17		
				10, 11	26		
Select to $\overline{LE}$ hold time, high or low	t_h 3/	See figure 4	2.0 V	9, 10, 11	0.0		ns
			4.5 V		0.0		
			6.0 V		0.0		
Propagation delay time, select to output	t_{PHL1} t_{PLH1} 5/	C_L = 50 pF minimum See figure 4	2.0 V 3/	9		275	ns
				10, 11		415	
			4.5 V	9		55	
				10, 11		83	
			6.0 V 3/	9		47	
				10, 11		71	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+2.0\ V \le V_{CC} \le +6.0\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 2/		Unit
					Min	Max	
Propagation delay time, $\overline{LE}$ to output	t_{PHL2} t_{PLH2} 5/	C_L = 50 pF minimum See figure 4	2.0 V 3/	9		225	ns
				10, 11		340	
			4.5 V	9		45	
				10, 11		68	
			6.0 V 3/	9		38	
				10, 11		58	
Propagation delay time, $\overline{E}$ to output	t_{PHL3} t_{PLH3} 5/	C_L = 50 pF minimum See figure 4	2.0 V 3/	9		175	ns
				10, 11		265	
			4.5 V	9		35	
				10, 11		53	
			6.0 V 3/	9		30	
				10, 11		45	
Output transition time	t_{THL} t_{TLH} 3/	C_L = 50 pF minimum See figure 4	2.0 V	9		75	ns
				10, 11		110	
			4.5 V	9		15	
				10, 11		22	
			6.0 V	9		13	
				10, 11		19	

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} test, where the output terminals shall be open. When performing the I_{CC} test, the current meter shall be placed in the circuit such that all current flows through the meter. The values to be used for V_{IH} and V_{IL} shall be the V_{IH} minimum and V_{IL} maximum values listed in section 1.4 herein.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ This parameter is guaranteed, if not tested. This parameter is characterized upon initial design or process changes which affect this characteristic.

4/ The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein.

5/ For propagation delay tests, the worst case paths must be tested.

Device type	All
Case outline	J
Terminal number	Terminal symbol
1	$\overline{LE}$
2	A0
3	A1
4	Y7
5	Y6
6	Y5
7	Y4
8	Y3
9	Y1
10	Y2
11	Y0
12	GND
13	Y13
14	Y12
15	Y15
16	Y14
17	Y9
18	Y8
19	Y11
20	Y10
21	A2
22	A3
23	$\overline{E}$
24	V_{CC}

FIGURE 1. Terminal connections.

Decode truth table (LE = 1)

$\overline{E}$	Decoder inputs				Addressed output
	A3	A2	A1	A0	
0	0	0	0	0	Y0
0	0	0	0	1	Y1
0	0	0	1	0	Y2
0	0	0	1	1	Y3
0	0	1	0	0	Y4
0	0	1	0	1	Y5
0	0	1	1	0	Y6
0	0	1	1	1	Y7
0	1	0	0	0	Y8
0	1	0	0	1	Y9
0	1	0	1	0	Y10
0	1	0	1	1	Y11
0	1	1	0	0	Y12
0	1	1	0	1	Y13
0	1	1	1	0	Y14
0	1	1	1	1	Y15
1	X	X	X	X	All outputs = 0

1 = High logic level
0 = Low logic level
X = Don't care

FIGURE 2. Truth table.

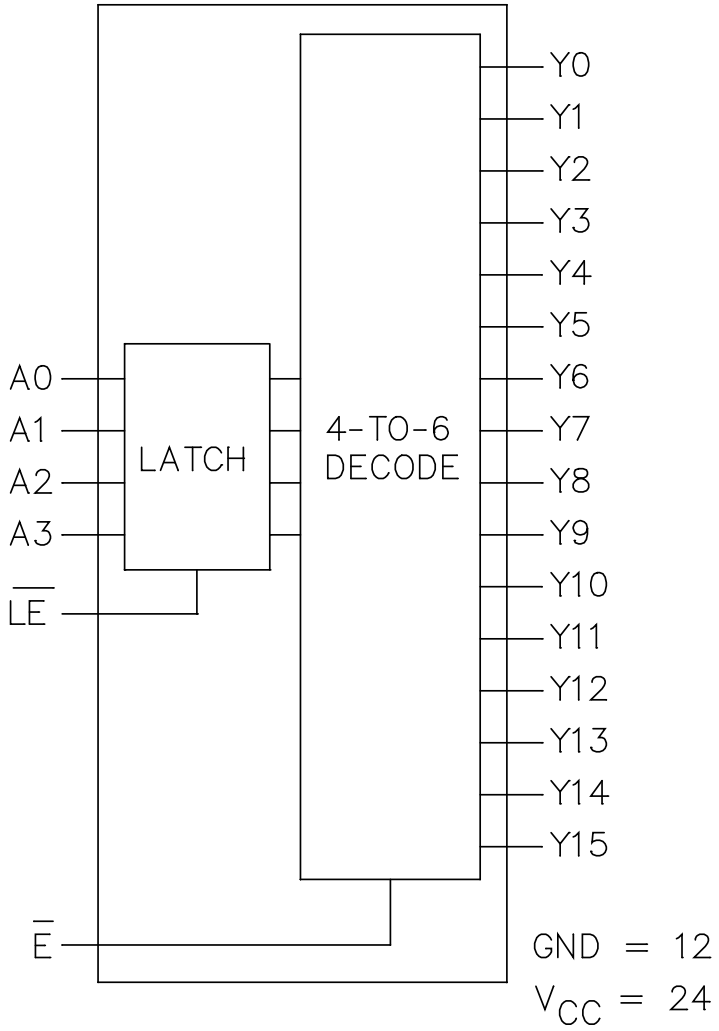
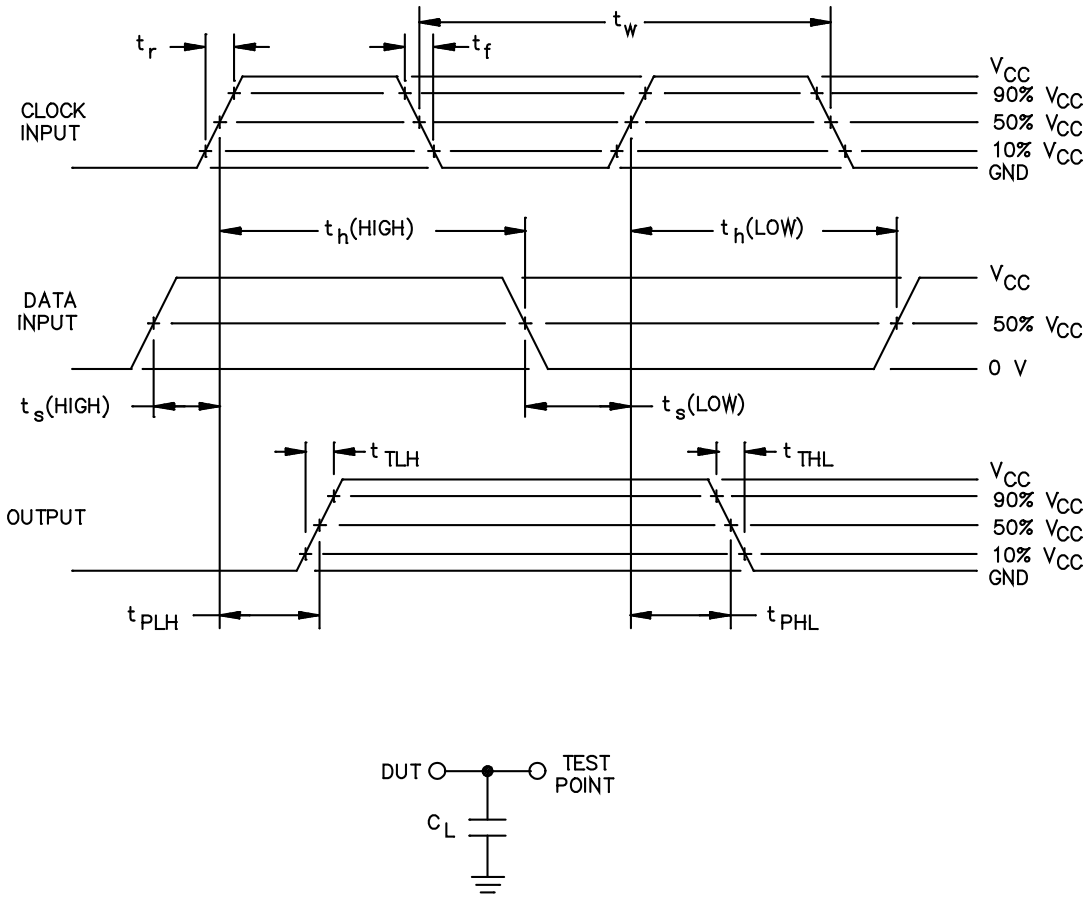


FIGURE 3. Block diagram.



NOTES:
1. C_L = 50 pF (includes test jig and probe capacitance).
2. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 1 MHz; t_r = 6.0 ns; t_f = 6.0 ns; t_r and t_f shall be measured from 0.1 V_{CC} to 0.9 V_{CC} and from 0.9 V_{CC} to 0.1 V_{CC}, respectively; duty cycle = 50 percent.
3. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. The C_{IN} test shall be sufficient to validate the limits defined in table I herein.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroups 1 and 7.
2/ PDA applies to subgroups 1, 7 and 9.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-03-20

Approved sources of supply for SMD 5962-98655 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9865501QJA	01295	CD54HC4514F3A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493