

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes IAW NOR 5962-R065-99. - TVN	99-06-03	Monica L. Poelking
B	Update boilerplate to MIL-PRF-38535 requirements. Incorporate Revision A changes from NOR 5962-R065-99. - CFS	03-03-18	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	07-12-12	Thomas M. Hess
D	Add device type 02. - PHN	10-08-11	Thomas M. Hess
E	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-09-11	Thomas M. Hess
F	Update device type 02 availability to bulletin page. Update boilerplate to MIL-PRF-38535 requirements. - DRH	24-05-08	Muhammad A. Akbar



REV	F	F	F	F	F	F	F	F	F	F	F	F								
SHEET	35	36	37	38	39	40	41	42	43	44	45	46								
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

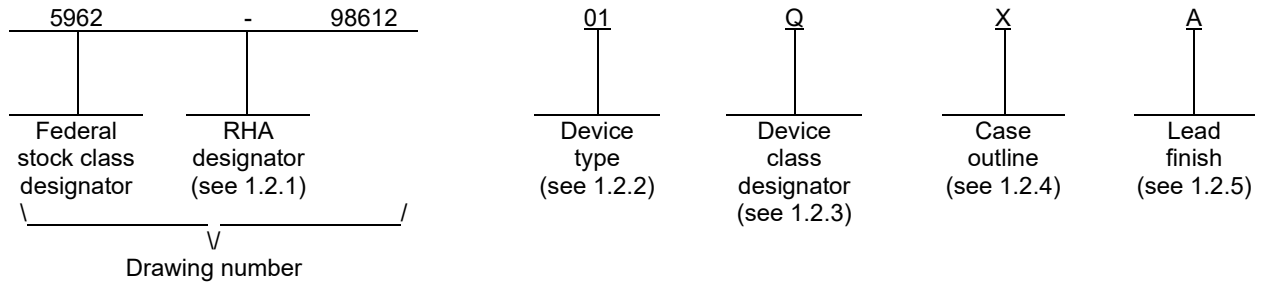
REV STATUS OF SHEETS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	PREPARED BY Thanh V. Nguyen	<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="https://www.dia.mil/LandandMaritime">https://www.dia.mil/LandandMaritime</a></p>																	
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Thanh V. Nguyen																		
	APPROVED BY Monica L. Poelking	<p align="center">MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR CONTROLLER, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 99-04-30																		
	REVISION LEVEL <b>F</b>	SIZE <b>A</b>	CAGE CODE <b>67268</b>	<b>5962-98612</b>															
		SHEET	1	OF	46														

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Operating temperature range</u>	<u>Circuit function</u>
01	320F240	-55°C to +125°C	Digital signal processor controller
02	320F240	-55°C to +115°C	Digital signal processor controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	132	Ceramic quad flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{DD}$ ) .....	-0.3 V dc to +7.0 V dc 2/
Input voltage range ( $V_{IN}$ ) .....	-0.3 V dc to +7.0 V dc
Output voltage range ( $V_{OUT}$ ) .....	-0.3 V dc to +7.0 V dc
Storage temperature range ( $T_{STG}$ ).....	-65°C to +150°C
Analog supply reference source ( $V_{REFHI}$ , $V_{REFLO}$ ).....	-0.3 V dc to +7.0 V dc
Analog input voltage range ( $V_{AI}$ ) .....	-0.3 V dc to +7.0 V dc
Resolution .....	10-bit (1024 values)
Monotonic .....	Assured
Output conversion mode .....	000h to 3FFh (000h for $V_I \leq V_{SSA}$ ; 3FFh for $V_I \geq V_{CCA}$ )
Thermal resistance, junction-to-ambient ( $\theta_{JA}$ ) .....	55.71°C/W
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	2.57°C/W

1.4 Recommended operating conditions.

Digital supply voltage range ( $DV_{DD}$ ) .....	+4.5 V to +5.5 V
Supply voltage return .....	0.0 V
High level input voltage range ( $V_{IH}$ ):	
XTAL1/CLKIN .....	+3.0 V to $V_{DD} + 0.3$ V
$\overline{PORESET}$ , $\overline{NMI}$ , $\overline{RS}$ , and $\overline{TRST}$ .....	+2.2 V to $V_{DD} + 0.3$ V
All other inputs.....	+2.0 V to $V_{DD} + 0.3$ V
Low level input voltage range ( $V_{IL}$ ):	
XTAL1/CLKIN .....	-0.3 V to 0.7 V
All other inputs.....	-0.3 V to 0.8 V
High level output current ( $I_{OH}$ ):	
$\overline{RS}$ .....	-19 mA 3/
IOPA[0:3], SCIRXD/IO, SCITXD/IO, XINT2/IO, XINT3/IO, ADCSOC/IOPC0, TMRDIR/IOPB6, TMRCLK/IOPB7, EMU0, EMU1/ $\overline{OFF}$ .....	-16 mA 3/
All other outputs.....	-23 mA 3/
Low level output current ( $I_{OL}$ ):	
$\overline{RS}$ .....	8 mA 3/
IOPA[0:3], SCIRXD/IO, SCITXD/IO, XINT2/IO, XINT3/IO, ADCSOC/IOPC0, TMRDIR/IOPB6, TMRCLK/IOPB7, EMU0, EMU1/ $\overline{OFF}$ .....	7.5 mA 3/
All other outputs.....	14.5 mA 3/
Case operating temperature range ( $T_C$ ):	
Device type 01 .....	-55°C to +125°C
Device type 02 .....	-55°C to +115°C
Flash programming operating temperature range ( $T_{FP}$ ) .....	-40°C to +85°C
Recommended operating conditions for 10-bit dual analog-to-digital converter (ADC):	
Analog supply voltage range ( $V_{CCA}$ ).....	4.5 V to +5.5 V
Analog ground ( $V_{SSA}$ ).....	0 V
Analog supply reference source range ( $V_{REFHI}$ ) .....	$V_{REFLO}$ to $V_{CCA}$ 4/
Analog ground reference source range ( $V_{REFLO}$ ).....	$V_{SSA}$ to $V_{REFHI}$ 4/
Analog input voltage range – ADCIN0-ADCIN15 ( $V_{AI}$ ).....	$V_{SSA}$ to $V_{CCA}$

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/  $V_{DD}$  refers to supply voltage types  $CV_{DD}$  (digital core supply voltage),  $DV_{DD}$  (digital I/O supply voltage), and  $V_{DDP}$  (programming voltage supply). All voltages are measured with respect to  $V_{SS}$ .
- 3/ Typical readings derived from Spice simulations. Not production tested.
- 4/  $V_{REFHI}$  and  $V_{REFLO}$  must be stable, within  $\pm 1/2$  LSB of the required resolution, during the entire conversion time.

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following document(s) form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these document(s) are those cited in the solicitation or contract.

### INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at <https://www.ieee.org/>.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 4.

3.2.5 Test circuit and timing waveforms. The test circuit and timing waveforms are as specified on figure 5.

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3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 IEEE 1149.1 compliance. These devices shall be compliant to IEEE 1149.1.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
High-level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = MAX		All	1, 2, 3	2.4		V
Low-level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = MAX		All	1, 2, 3		0.6	V
Input current	I <sub>I</sub>	V <sub>I</sub> = V <sub>SS</sub> or V <sub>DD</sub>	$\overline{\text{TRST}}$ with internal pulldown	All	1, 2, 3	-10	500	μA
			EMU0, EMU1/ $\overline{\text{OFF}}$ , TMS, TCK, and TDI, with internal pullup			-500	10	
			All other input pins			-10	10	
Output current, high impedance state (off-state)	I <sub>OZ</sub>	V <sub>O</sub> = V <sub>DD</sub> or 0.0 V		All	1, 2, 3	-5	5	μA
Supply current, operating mode	I <sub>DD1</sub>	t <sub>c(CO)</sub> = 50 ns		All	1, 2, 3		100 <u>1</u> /	mA
Supply current, idle 1 low-power mode	I <sub>DD2</sub>	t <sub>c(CO)</sub> = 50 ns		All	1, 2, 3		50 <u>1</u> /	mA
Supply current, idle 2 low-power mode	I <sub>DD3</sub>	t <sub>c(CO)</sub> = 50 ns		All	1, 2, 3		7 <u>1</u> /	mA
Supply current, PLL power-down mode	I <sub>DD4</sub>	t <sub>c(CO)</sub> = 50 ns		All	1, 2, 3		5 <u>1</u> /	mA
Supply current, OSC power-down mode	I <sub>DD5</sub>	t <sub>c(CO)</sub> = 50 ns		All	1, 2, 3		400 <u>1</u> /	μA
Flash programming supply current	I <sub>DDP</sub>	t <sub>c(CO)</sub> = 50 ns		All	1, 2, 3		10 <u>1</u> /	mA
Input capacitance	C <sub>I</sub>	See 4.4.1c		All	4		15	pF
Output capacitance	C <sub>O</sub>	See 4.4.1c		All	4		15	pF
Functional testing		See 4.4.1b		All	7, 8			

See footnotes at end of table.

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DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

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SHEET  
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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit	
					Min	Max		
Clock options – Input clock frequency with the PLL circuit disabled								
Input clock frequency, divide-by-2 mode	f <sub>x1</sub>		All	9, 10, 11	0 <u>2</u> /	40	MHz	
Input clock frequency, divide-by-1 mode	f <sub>x2</sub>		All	9, 10, 11	0 <u>2</u> /	20		
Clock options – Switching characteristics, H = 0.5 t <sub>c(CO)</sub> <u>3</u> /								
Cycle time, CPUCLK	t <sub>c(CPU)</sub>	See figure 5	CLKIN divide by 2	All	9, 10, 11	2t <sub>c(CI)</sub> <u>1</u> /	<u>2</u> /	ns
			CLKIN divide by 1			t <sub>c(CI)</sub> <u>1</u> /		
Cycle time, SYSCLK	t <sub>c(SYS)</sub>	See figure 5	CPUCLK divide by 2	All	9, 10, 11	2t <sub>c(CPU)</sub> <u>1</u> /	<u>2</u> /	ns
			CPUCLK divide by 4 <u>4</u> /			4t <sub>c(CPU)</sub> <u>1</u> /		
Cycle time, CLKOUT	t <sub>c(CO)</sub>	See figure 5	CLKIN divide by 2	All	9, 10, 11	2t <sub>c(CI)</sub> <u>1</u> /	<u>2</u> /	ns
			CLKIN divide by 1			t <sub>c(CI)</sub> <u>1</u> /		
Delay time, XTAL1/CLKIN high to CLKOUT high/low	t <sub>d(CIH-CO)</sub>	See figure 5	All	9, 10, 11	3	22	ns	
Fall time, CLKOUT	t <sub>f(CO)</sub>		All	9, 10, 11		5 <u>1</u> /	ns	
Rise time, CLKOUT	t <sub>r(CO)</sub>		All	9, 10, 11		5 <u>1</u> /	ns	
Pulse duration, CLKOUT low	t <sub>w(COL)</sub>		All	9, 10, 11	H-10	H-1	ns	
Pulse duration, CLKOUT high	t <sub>w(COH)</sub>		All	9, 10, 11	H+0	H+8	ns	
Clock options – Timing requirements								
Cycle time, XTAL1/CLKIN	t <sub>c(CI)</sub>	See figure 5	Divide by 2	All	9, 10, 11	25	<u>2</u> /	ns
			Divide by 1			50		
Fall time, XTAL1/CLKIN	t <sub>f(CI)</sub>	See figure 5	All	9, 10, 11		5 <u>1</u> /	ns	
Rise time, XTAL1/CLKIN	t <sub>r(CI)</sub>		All	9, 10, 11		5 <u>1</u> /	ns	
Pulse duration, XTAL1/CLKIN low as a percentage of t <sub>c(CI)</sub>	t <sub>w(CIL)</sub>		All	9, 10, 11	45	55	%	
Pulse duration, XTAL1/CLKIN high as a percentage of t <sub>c(CI)</sub>	t <sub>w(CIH)</sub>		All	9, 10, 11	45	55	%	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Clock options – Input characteristics with the PLL circuit enabled								
Input clock frequency	f <sub>x</sub>	External reference crystal = 4 MHz		All	9, 10, 11		4 <u>1/</u>	MHz
		External reference crystal = 6 MHz					6 <u>1/</u>	
		External reference crystal = 8 MHz					8 <u>1/</u>	
Load capacitance	C1, C2			All	4		10 <u>1/</u>	pF
Clock options – Switching characteristics, H = 0.5 t <sub>c(CO)</sub>								
Cycle time, CPUCLK	t <sub>c(CPU)</sub>	See figure 5	Before PLL lock, CLKIN divide by 2	All	9, 10, 11	2t <sub>c(CI)</sub> <u>1/</u>	<u>2/</u>	ns
			Before PLL lock, CLKIN divide by 1			t <sub>c(CI)</sub> <u>1/</u>		
			After PLL lock			50 <u>1/</u>		
Cycle time, SYSCLK	t <sub>c(SYS)</sub>	See figure 5	CPUCLK divide by 2	All	9, 10, 11	2t <sub>c(CPU)</sub> <u>1/</u>	<u>2/</u>	ns
			CPUCLK divide by 4 <u>4/</u>			4t <sub>c(CPU)</sub> <u>1/</u>		
Cycle time, CLKOUT	t <sub>c(CO)</sub>	See figure 5		All	9, 10, 11	50	<u>2/</u>	ns
Fall time, CLKOUT	t <sub>f(CO)</sub>		All	9, 10, 11		5 <u>1/</u>	ns	
Rise time, CLKOUT	t <sub>r(CO)</sub>		All	9, 10, 11		5 <u>1/</u>	ns	
Pulse duration, CLKOUT low	t <sub>w(COL)</sub>		All	9, 10, 11	H-10	H-1	ns	
Pulse duration, CLKOUT high	t <sub>w(COH)</sub>		All	9, 10, 11	H+0	H+8	ns	
Transition time, PLL synchronized after PLL enabled	t <sub>p</sub>		See figure 5	Before PLL lock, CLKIN divide by 2	All	9, 10, 11		2000 t <sub>c(CI)</sub>
		Before PLL lock, CLKIN divide by 1					1000 t <sub>c(CI)</sub>	
Clock options – Timing requirements <u>3/</u>								
Cycle time, XTAL1/CLKIN	t <sub>c(CI)</sub>	See figure 5	External reference crystal = 4 MHz	All	9, 10, 11	250	<u>2/</u>	ns
			External reference crystal = 6 MHz				167	
			External reference crystal = 8 MHz				125	
Fall time, XTAL1/CLKIN	t <sub>f(CI)</sub>	See figure 5		All	9, 10, 11		5 <u>1/</u>	ns
Rise time, XTAL1/CLKIN	t <sub>r(CI)</sub>		All	9, 10, 11		5 <u>1/</u>	ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Clock options – Timing requirements – Continued 3/							
Pulse duration, XTAL1/CLKIN low as a percentage of t <sub>c(CI)</sub>	t <sub>w(CIL)</sub>	See figure 5	All	9, 10, 11	40	60	%
Pulse duration, XTAL1/CLKIN high as a percentage of t <sub>c(CI)</sub>	t <sub>w(CIH)</sub>		All	9, 10, 11	40	60	%
Low-power mode timings – Switching characteristics, H = 0.5 t <sub>c(CO)</sub>							
Delay time, CLKOUT switching to program execution resume 3/	t <sub>d(WAKE-A)</sub>	See figure 5	Idle 1 and idle 2			15xt <sub>c(CO)</sub>	ns
			PLL or OSC power down			15xt <sub>c(CI)</sub>	
Delay time, idle instruction executed to CLKOUT high 3/	t <sub>d(IDLE-COH)</sub>	See figure 5	Idle 2, PLL power down, OSC power down			500 1/	ns
Delay time, CLKOUT switching to PLL synchronized 3/	t <sub>d(WAKE-LOCK)</sub>	See figure 5	PLL or OSC power down			100 1/	μs
Delay time, wakeup interrupt asserted to oscillator running	t <sub>d(WAKE-OSC)</sub>	See figure 5	OSC power down			10 1/	ms
Delay time, idle instruction executed to oscillator power off	t <sub>d(IDLE-OSC)</sub>	See figure 5	OSC power down			60 1/	μs
Memory and parallel I/O interface read timings – Switching characteristics for a memory read, H = 0.5 t <sub>c(CO)</sub> 5/							
Delay time, CLKOUT/IOPC1 low to address valid	t <sub>d(CO-A)RD</sub>	See figure 5	All	9, 10, 11		17	ns
Delay time, CLKOUT/IOPC1 low to $\overline{\text{STRB}}$ low	t <sub>d(CO-SL)RD</sub>		All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 low to $\overline{\text{STRB}}$ high	t <sub>d(CO-SH)RD</sub>		All	9, 10, 11		6	ns
Delay time, CLKOUT/IOPC1 low to $\overline{\text{PS}}$ , $\overline{\text{DS}}$ , $\overline{\text{IS}}$ , and $\overline{\text{BR}}$ low	t <sub>d(CO-ACTL)RD</sub>		All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 low to $\overline{\text{PS}}$ , $\overline{\text{DS}}$ , $\overline{\text{IS}}$ , and $\overline{\text{BR}}$ high	t <sub>d(CO-ACTH)RD</sub>		All	9, 10, 11		10	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit	
					Min	Max		
Memory and parallel I/O interface read timings – Timing requirements for a memory read, H = 0.5 t <sub>c(CO)</sub> 5/								
Access time, from address valid to read data	t <sub>a(A)</sub> 1/	See figure 5	0 wait state	All	9, 10, 11		2H-32	ns
			1 wait state				4H-32	
Setup time, data read before CLKOUT/IOPC1 low	t <sub>su(D-COL)RD</sub>	See figure 5	All	9, 10, 11	13			ns
Hold time, data read after CLKOUT/IOPC1 low	t <sub>h(COL-D)RD</sub>		All	9, 10, 11	2			ns

Memory and parallel I/O interface write timings – Switching characteristic for a memory write, H = 0.5 t <sub>c(CO)</sub> 5/								
Delay time, CLKOUT/IOPC1 high to address valid	t <sub>d(CO-A)W</sub>	See figure 5	All	9, 10, 11		17		ns
Delay time, CLKOUT/IOPC1 low to data bus driven	t <sub>d(CO-D)</sub>		All	9, 10, 11		15		ns
Delay time, address valid after WE high	t <sub>d(D-WH)</sub>		All	9, 10, 11	H-8			ns
Pulse duration, WE high	t <sub>w(WH)</sub>		All	9, 10, 11	2H-11			ns
Pulse duration, WE low	t <sub>w(WL)</sub>		All	9, 10, 11	2H-11			ns
Delay time, CLKOUT/IOPC1 low to WE low	t <sub>d(CO-WL)</sub>		All	9, 10, 11		9		ns
Delay time, CLKOUT/IOPC1 low to WE high	t <sub>d(CO-WH)</sub>		All	9, 10, 11		9		ns
Delay time, write data valid before WE high	t <sub>d(WH-D)</sub>		All	9, 10, 11	2H-8			ns
Delay time, WE high to data bus high-Z	t <sub>d(D-WHZ)</sub>		All	9, 10, 11	0	5		ns
Delay time, CLKOUT/IOPC1 low to STRB low	t <sub>d(CO-SL)W</sub>		All	9, 10, 11			10	

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>10</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Memory and parallel I/O interface write timings – Switching characteristic for a memory write, H = 0.5 t <sub>c(CO)</sub> – Continued <u>5/</u>							
Delay time, CLKOUT/IOPC1 low to STRB high	t <sub>d(CO-SH)W</sub>	See figure 5	All	9, 10, 11		6	ns
Delay time, CLKOUT/IOPC1 high to PS, DS, IS, and BR low	t <sub>d(CO-ACTL)W</sub>		All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 high to PS, DS, IS, and BR high	t <sub>d(CO-ACTH)W</sub>		All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 high to R/W low	t <sub>d(CO-RWL)</sub>		All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 high to R/W high	t <sub>d(CO-RWH)</sub>		All	9, 10, 11		10	ns
READY timings – Timing requirements <u>6/</u>							
Setup time, READY low before CLKOUT/IOPC1 high	t <sub>su(R-CO)</sub>	See figure 5	All	9, 10, 11	14		ns
Hold time, READY low after CLKOUT/IOPC1 high	t <sub>h(CO-R)</sub>		All	9, 10, 11	0		ns
Valid time, READY after address valid on read	t <sub>v(R)ARD</sub> <u>1/</u>		All	9, 10, 11		3H-31	ns
Valid time, READY after address valid on write	t <sub>v(R)AW</sub> <u>1/</u>		All	9, 10, 11		4H-31	ns
<u>RS</u> and <u>PORESET</u> timings – Switching characteristics for a reset, H = 0.5 t <sub>c(CO)</sub>							
Pulse duration, <u>RS</u> low <u>7/</u>	t <sub>w(RSL1)</sub> <u>1/</u>	See figure 5	All	9, 10, 11	8t <sub>c(SYS)</sub>		ns
Delay time, <u>RS</u> low to program address at reset vector	t <sub>d(RS)</sub> <u>1/</u>		All	9, 10, 11	4H		ns
Delay time, <u>RS</u> high to reset vector executed	t <sub>d(EX)</sub> <u>1/</u>		All	9, 10, 11	32H		ns

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	<b>SIZE A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>11</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
<u>RS</u> and <u>PORESET</u> timings – Timing requirements for a reset, H = 0.5 t <sub>c(CO)</sub>							
Pulse duration, <u>RS</u> or <u>PORESET</u> low <u>8/</u>	t <sub>w(RSL)</sub> <u>1/</u>	See figure 5	All	9, 10, 11	5		ns
<u>XF</u> , <u>BIO</u> , and <u>MP/MC</u> timings – Switching characteristic, H = 0.5 t <sub>c(CO)</sub>							
Delay time, CLKOUT high to XF high/low	t <sub>d(XF)</sub>	See figure 5	All	9, 10, 11		11	ns
<u>XF</u> , <u>BIO</u> , and <u>MP/MC</u> timings – Timing requirements, H = 0.5 t <sub>c(CO)</sub>							
Pulse duration, <u>BIO</u> low	t <sub>w(BIOL)</sub>	See figure 5	All	9, 10, 11	2H+16		ns
Pulse duration, <u>MP/MC</u> valid <u>9/</u>	t <sub>w(MPMCV)</sub> <u>1/</u>		All	9, 10, 11	2H+24		ns
PWM/CMP timings – Switching characteristic for PWM timing, H = 0.5 t <sub>c(CO)</sub>							
Delay time, CLKOUT high to PWM output switching	t <sub>d(PWM)CO</sub> <u>1/</u>	See figure 5	All	9, 10, 11		12	ns
PWM/CMP timings – Timing requirements							
Pulse duration, TMRDIR low/high	t <sub>w(TMRDIR)</sub> <u>1/</u>	See figure 5	All	9, 10, 11	4H+12		ns
Pulse duration, TMRCLK low as a percentage of TMRCLK cycle time	t <sub>w(TMRCLKL)</sub> <u>1/</u>		All	9, 10, 11	40	60	%
Pulse duration, TMRCLK high as a percentage of TMRCLK cycle time	t <sub>w(TMRCLKH)</sub> <u>1/</u>		All	9, 10, 11	40	60	%
Cycle time, TMRCLK	t <sub>c(TMRCLK)</sub> <u>1/</u>		All	9, 10, 11	4xt <sub>c(CPU)</sub>		ns
Capture and QEP timings – Timing requirements							
Pulse duration, CAP input low/high	t <sub>w(CAP)</sub> <u>1/</u>	See figure 5	All	9, 10, 11	4H+12		ns
Interrupt timings – Switching characteristics for interrupt, H = 0.5 t <sub>c(CO)</sub>							
Delay time, <u>PDPINT</u> low to PWM to high-impedance state	t <sub>d(PWM)PDP</sub>	See figure 5	All	9, 10, 11	0	15	ns

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>12</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit		
					Min	Max			
Interrupt timings – Timing requirements									
Pulse duration, INT input low/high	t <sub>w(INT)</sub>	See figure 5	All	9, 10, 11	t <sub>c(SYS)</sub> +12		ns		
Pulse duration, $\overline{\text{PDPINT}}$ input low	t <sub>w(PDP)</sub>		All	9, 10, 11	2H+18		ns		
Delay time, INT low/high to interrupt-vector fetch	t <sub>d(INT)</sub> <u>1/</u>		All	9, 10, 11	2t <sub>c(SYS)</sub> +4t <sub>c(CPU)</sub>		ns		
General-purpose input/output timings – Switching characteristics for a GPI/O, H = 0.5 t <sub>c(CO)</sub>									
Delay time, CLKOUT low to GPO low/high	t <sub>d(GPO)CO</sub>	See figure 5	All 9, 10, 11		XINT2/IO, XINT3/IO, IOPB6, IOPB7, and IOPC0		33	ns	
					All other GPOs		25		
General-purpose input/output timings - Timing requirements									
Pulse duration, GPI high/low	t <sub>w(GPI)</sub>	See figure 5	All	9, 10, 11	t <sub>c(SYS)</sub> +12		ns		
Serial communications interface (SCI) I/O timings – Timing characteristics for SCI <u>10/</u>									
Cycle time, SCICLK	t <sub>c(SCC)</sub> <u>1/</u>	See figure 5	All 9, 10, 11		(BRR+1) is even and BRR = 0		16t <sub>c</sub>	65536t <sub>c</sub>	ns
					(BRR+1) is odd and BRR ≠ 0		24t <sub>c</sub>	65535t <sub>c</sub>	
Valid time, SCITXD data	t <sub>v(TXD)</sub>	See figure 5	All 9, 10, 11		(BRR+1) is even and BRR = 0		t <sub>c(SCC)</sub> -70	t <sub>c(SCC)</sub> +70	ns
					(BRR+1) is odd and BRR ≠ 0		t <sub>c(SCC)</sub> -70	t <sub>c(SCC)</sub> +70	
Valid time, SCIRXD data	t <sub>v(RXD)</sub>	See figure 5	All 9, 10, 11		(BRR+1) is even and BRR = 0		16t <sub>c</sub>		ns
					(BRR+1) is odd and BRR ≠ 0		24t <sub>c</sub>		

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	<b>SIZE A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>13</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit	
					Min	Max		
SPI master mode external timing parameters (clock phase = 0) 1/ 11/								
Cycle time, SPICLK	t <sub>c(SPC)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	4t <sub>c</sub> <u>10/</u>	128t <sub>c</sub> <u>10/</u>	ns
			(SPIBRR+1) is odd or SPIBRR > 3			5t <sub>c</sub> <u>10/</u>	127t <sub>c</sub> <u>10/</u>	
Pulse duration, SPICLK high (clock polarity = 0)	t <sub>w(SPCH)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)M</sub> -7 0	0.5t <sub>c(SPC)M</sub>	ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> -0 .5t <sub>c</sub> -70	0.5t <sub>c(SPC)M</sub> -0.5t <sub>c</sub>	
Pulse duration, SPICLK low (clock polarity = 1)	t <sub>w(SPCL)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)M</sub> -7 0	0.5t <sub>c(SPC)M</sub>	ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> -0 .5t <sub>c</sub> -70	0.5t <sub>c(SPC)M</sub> -0.5t <sub>c</sub>	
Pulse duration, SPICLK low (clock polarity = 0)	t <sub>w(SPCL)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)M</sub> -7 0	0.5t <sub>c(SPC)M</sub>	ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> +0.5t <sub>c</sub> -70	0.5t <sub>c(SPC)M</sub> +0.5t <sub>c</sub>	
Pulse duration, SPICLK high (clock polarity = 1)	t <sub>w(SPCH)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)M</sub> -7 0	0.5t <sub>c(SPC)M</sub>	ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> +0.5t <sub>c</sub> -70	0.5t <sub>c(SPC)M</sub> +0.5t <sub>c</sub>	
Delay time, SPICLK high (clock polarity = 0) to SPISIMO valid	t <sub>d(SPCH-SIMO)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	-10	10	ns
			(SPIBRR+1) is odd or SPIBRR > 3			-10	10	
Delay time, SPICLK low (clock polarity = 1) to SPISIMO valid	t <sub>d(SPCL-SIMO)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	-10	10	ns
			(SPIBRR+1) is odd or SPIBRR > 3			-10	10	
Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	t <sub>h(SPCL-SIMO)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)M</sub> -7 0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> +0.5t <sub>c</sub> -70		
Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1)	t <sub>h(SPCH-SIMO)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)M</sub> -7 0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> +0.5t <sub>c</sub> -70		

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>14</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit	
					Min	Max		
SPI master mode external timing parameters (clock phase = 0) – Continued <u>1/ 11/</u>								
Setup time, SPISOMI before SPICLK low (clock polarity = 0)	t <sub>su(SOMI-SPCL)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0		
Setup time, SPISOMI before SPICLK high (clock polarity = 1)	t <sub>su(SOMI-SPCH)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0		
Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	t <sub>h(SPCL-SOMI)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.25t <sub>c(SPC)M</sub> - 70		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> - 0.5t <sub>c-70</sub>		
Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	t <sub>h(SPCH-SOMI)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.25t <sub>c(SPC)M</sub> - 70		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> - 0.5t <sub>c-70</sub>		
SPI master mode external timing parameters (clock phase = 1) <u>1/ 13/</u>								
Cycle time, SPICLK	t <sub>c(SPC)M</sub>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	4t <sub>c</sub> <u>10/</u>	128t <sub>c</sub> <u>10/</u>	ns
			(SPIBRR+1) is odd or SPIBRR > 3			5t <sub>c</sub> <u>10/</u>	127t <sub>c</sub> <u>10/</u>	
Pulse duration, SPICLK high (clock polarity = 0)	t <sub>w(SPCH)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)M</sub> - 70	0.5t <sub>c(SPC)M</sub>	ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> - 0.5t <sub>c-70</sub>	0.5t <sub>c(SPC)M</sub> - 0.5t <sub>c</sub>	
Pulse duration, SPICLK low (clock polarity = 1)	t <sub>w(SPCL)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)M</sub> - 70	0.5t <sub>c(SPC)M</sub>	ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> - 0.5t <sub>c-70</sub>	0.5t <sub>c(SPC)M</sub> - 0.5t <sub>c</sub>	
Pulse duration, SPICLK low (clock polarity = 0)	t <sub>w(SPCL)M</sub> <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)M</sub> - 70	0.5t <sub>c(SPC)M</sub>	ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)M</sub> + 0.5t <sub>c-70</sub>	0.5t <sub>c(SPC)M</sub> + 0.5t <sub>c</sub>	

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	<b>SIZE A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>15</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>c</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>c</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit	
					Min	Max		
SPI master mode external timing parameters (clock phase = 1) – Continued <u>1/ 13/</u>								
Pulse duration, SPICLK high (clock polarity = 1)	t <sub>w(SPCH)</sub> M <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)</sub> M -7 0	0.5t <sub>c(SPC)</sub> M	ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)</sub> M +0.5t <sub>c</sub> -70	0.5t <sub>c(SPC)</sub> M +0.5t <sub>c</sub>	
Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0)	t <sub>su(SIMO-SPCH)</sub> M <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)</sub> M -7 0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)</sub> M -7 0		
Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1)	t <sub>su(SIMO-SPCL)</sub> M <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)</sub> M -7 0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)</sub> M -7 0		
Hold time, SPISIMO data valid after SPICLK high (clock polarity = 0)	t <sub>h(SPCH-SIMO)</sub> M <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)</sub> M -7 0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)</sub> M -7 0		
Hold time, SPISIMO data valid after SPICLK low (clock polarity = 1)	t <sub>h(SPCL-SIMO)</sub> M <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.5t <sub>c(SPC)</sub> M -7 0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)</sub> M -7 0		
Setup time, SPISOMI before SPICLK high (clock polarity = 0)	t <sub>su(SOMI-SPCH)</sub> M <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0		
Setup time, SPISOMI before SPICLK low (clock polarity = 1)	t <sub>su(SOMI-SPCL)</sub> M <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0		
Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	t <sub>h(SPCH-SOMI)</sub> M <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.25t <sub>c(SPC)</sub> M -70		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)</sub> M -7 0		
Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	t <sub>h(SPCL-SOMI)</sub> M <u>12/</u>	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0.25t <sub>c(SPC)</sub> M -70		ns
			(SPIBRR+1) is odd or SPIBRR > 3			0.5t <sub>c(SPC)</sub> M -7 0		

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>16</b>



TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>c</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>c</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
SPI slave mode external timing requirements (clock phase = 0) 1/ 14/							
Cycle time, SPICLK	t <sub>c(SPC)S</sub>	See figure 5	All	9, 10, 11	8t <sub>c</sub> 10/		ns
Pulse duration, SPICLK high (clock polarity = 0)	t <sub>w(SPCH)S</sub> 12/		All	9, 10, 11	0.5t <sub>c(SPC)S</sub> -7 0	0.5t <sub>c(SPC)S</sub>	ns
Pulse duration, SPICLK low (clock polarity = 1)	t <sub>w(SPCL)S</sub> 12/		All	9, 10, 11	0.5t <sub>c(SPC)S</sub> -7 0	0.5t <sub>c(SPC)S</sub>	ns
Pulse duration, SPICLK low (clock polarity = 0)	t <sub>w(SPCL)S</sub> 12/		All	9, 10, 11	0.5t <sub>c(SPC)S</sub> -7 0	0.5t <sub>c(SPC)S</sub>	ns
Pulse duration, SPICLK high (clock polarity = 1)	t <sub>w(SPCH)S</sub> 12/		All	9, 10, 11	0.5t <sub>c(SPC)S</sub> -7 0	0.5t <sub>c(SPC)S</sub>	ns
Delay time, SPICLK high (clock polarity = 0) to SPISOMI valid	t <sub>d(SPCH-SOMI)S</sub> 12/		All	9, 10, 11	0.375t <sub>c(SPC)S</sub> -70		ns
Delay time, SPICLK low (clock polarity = 1) to SPISOMI valid	t <sub>d(SPCL-SOMI)S</sub> 12/		All	9, 10, 11	0.375t <sub>c(SPC)S</sub> -70		ns
Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	t <sub>v(SPCL-SOMI)S</sub> 12/		All	9, 10, 11	0.75t <sub>c(SPC)S</sub>		ns
Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	t <sub>v(SPCH-SOMI)S</sub> 12/		All	9, 10, 11	0.75t <sub>c(SPC)S</sub>		ns
Setup time, SPISIMO before SPICLK low (clock polarity = 0)	t <sub>su(SIMO-SPCL)S</sub> 12/		All	9, 10, 11	0		ns
Setup time, SPISIMO before SPICLK high (clock polarity = 1)	t <sub>su(SIMO-SPCH)S</sub> 12/	All	9, 10, 11	0		ns	

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>17</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
SPI slave mode external timing requirements (clock phase = 0) – Continued 1/ 14/							
Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	t <sub>v(SPCL-SIMO)</sub> S <u>12/</u>	See figure 5	All	9, 10, 11	0.5t <sub>c(SPC)</sub> S		ns
Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	t <sub>v(SPCH-SIMO)</sub> S <u>12/</u>		All	9, 10, 11	0.5t <sub>c(SPC)</sub> S		ns
SPI slave mode external timing requirements (clock phase = 1) 1/ 15/							
Cycle time, SPICLK	t <sub>c(SPC)</sub> S	See figure 5	All	9, 10, 11	8t <sub>c</sub> <u>10/</u>		ns
Pulse duration, SPICLK high (clock polarity = 0)	t <sub>w(SPCH)</sub> S <u>12/</u>		All	9, 10, 11	0.5t <sub>c(SPC)</sub> S -7 0	0.5t <sub>c(SPC)</sub> S	ns
Pulse duration, SPICLK low (clock polarity = 1)	t <sub>w(SPCL)</sub> S <u>12/</u>		All	9, 10, 11	0.5t <sub>c(SPC)</sub> S -7 0	0.5t <sub>c(SPC)</sub> S	ns
Pulse duration, SPICLK low (clock polarity = 0)	t <sub>w(SPCL)</sub> S <u>12/</u>		All	9, 10, 11	0.5t <sub>c(SPC)</sub> S -7 0	0.5t <sub>c(SPC)</sub> S	ns
Pulse duration, SPICLK high (clock polarity = 1)	t <sub>w(SPCH)</sub> S <u>12/</u>		All	9, 10, 11	0.5t <sub>c(SPC)</sub> S -7 0	0.5t <sub>c(SPC)</sub> S	ns
Setup time, SPISOMI before SPICLK high (clock polarity = 0)	t <sub>su(SOMI-SPCH)</sub> S <u>12/</u>		All	9, 10, 11	0.125t <sub>c(SPC)</sub> S		ns
Setup time, SPISOMI before SPICLK low (clock polarity = 1)	t <sub>su(SOMI-SPCL)</sub> S <u>12/</u>		All	9, 10, 11	0.125t <sub>c(SPC)</sub> S		ns
Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	t <sub>v(SPCH-SOMI)</sub> S <u>12/</u>		All	9, 10, 11	0.75t <sub>c(SPC)</sub> S		ns
Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	t <sub>v(SPCL-SOMI)</sub> S <u>12/</u>		All	9, 10, 11	0.75t <sub>c(SPC)</sub> S		ns

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>18</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
SPI slave mode external timing requirements (clock phase = 1) – Continued 1/ 15/							
Setup time, SPISIMO before SPICLK high (clock polarity = 0)	t <sub>su(SIMO-SPCH)</sub> 12/	See figure 5	All	9, 10, 11	0		ns
Setup time, SPISIMO before SPICLK low (clock polarity = 1)	t <sub>su(SIMO-SPCL)</sub> 12/		All	9, 10, 11	0		ns
Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	t <sub>v(SPCH-SIMO)</sub> 12/		All	9, 10, 11	0.5t <sub>c(SPC)</sub> S		ns
Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	t <sub>v(SPCL-SIMO)</sub> 12/		All	9, 10, 11	0.5t <sub>c(SPC)</sub> S		ns

10-bit dual analog-to-digital converter (ADC) – Electrical characteristics 16/

Analog supply current	I <sub>CCA</sub>	V <sub>CCA</sub> = 5.5 V	Converting	All	1, 2, 3		5	mA
			Non-converting				2	
		V <sub>CCA</sub> = V <sub>REFHI</sub> = 5.5 V	PLL or OSC power down				1	
Input charge current, V <sub>REFHI</sub> or V <sub>REFLO</sub>	I <sub>ref</sub>	V <sub>CCA</sub> = V <sub>CCD</sub> = V <sub>REFHI</sub> = 5.5 V V <sub>REFLO</sub> = 0 V		All	1, 2, 3		5	mA
Analog input capacitance	C <sub>ai</sub>	Typical capacitive load on analog input pin	Non-sampling	All	4		6	pF
			Sampling				8	
Analog input source impedance	Z <sub>AI</sub>	Analog input source impedance for conversions to remain within specifications		All	1, 2, 3		9	kΩ
Differential non-linearity error	E <sub>DNL</sub>	Difference between the actual step width and the ideal value		All	1, 2, 3	-1	1.5	LSB
Integral non-linearity error	E <sub>INL</sub>	Maximum deviation from the best straight line through the ADC transfer characteristics, excluding the quantization error		All	1, 2, 3		±1.5	LSB
Delay time, power-up to ADC valid	t <sub>d(PU)</sub>	Time to stabilize analog stage after power-up		All	9, 10, 11		10	μs

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET 19

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
10-bit dual analog-to-digital converter (ADC) – Timing requirements <u>1/</u>							
Cycle time, ADC prescaled clock	t <sub>c(AD)</sub>	See figure 5	All	9, 10, 11	1		μs
Pulse duration, total sample/hold and conversion time <u>17/</u>	t <sub>w(SHC)</sub>		All	9, 10, 11	6.1		μs
Pulse duration, sample/hold time	t <sub>w(SH)</sub>		All	9, 10, 11	t <sub>c(AD)</sub>		μs
Setup time, analog input stable before sample/hold start	t <sub>su(SH)</sub>		All	9, 10, 11	0		ns
Hold time, analog input stable after sample/hold complete	t <sub>h(SH)</sub>		All	9, 10, 11	0		ns
Pulse duration, total conversion time	t <sub>w(C)</sub>		All	9, 10, 11	4.5t <sub>c(AD)</sub>		μs
Delay time, start of conversion to begin of sample and hold <u>18/</u>	t <sub>d(SOC-SH)</sub>		All	9, 10, 11	3t <sub>c(SYS)</sub>		ns
Delay time, end of conversion to data loaded into result FIFO	t <sub>d(EOC-FIFO)</sub>		All	9, 10, 11	3t <sub>c(SYS)</sub>		ns

Flash EEPROM – Switching characteristics

Program-erase endurance		All	9, 10, 11	10K		Cycles
Program pulse per word <u>19/</u>		All	9, 10, 11	1	150	Pulses
Erase pulses per array <u>19/</u>		All	9, 10, 11	1	1000	Pulses
Flash-write pulses per array <u>19/</u>		All	9, 10, 11	1	6000	Pulses

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>20</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions +4.5 V ≤ V <sub>DD</sub> ≤ +5.5 V -55°C ≤ T <sub>C</sub> ≤ +125°C for device type 01 -55°C ≤ T <sub>C</sub> ≤ +115°C for device type 02 unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
<b>Flash EEPROM – Timing requirements</b>							
Delay time, after mode deselect to stabilization <u>19/</u>	t <sub>d(BUSY)</sub>		All	9, 10, 11	10		μs
Delay time, verify read mode select to stabilization <u>19/</u>	t <sub>d(RD-VERIFY)</sub>		All	9, 10, 11	10		μs
<b>Flash EEPROM – Programming operation (maximum programming temperature 85°C for flash memory)</b>							
Pulse duration, programming algorithm <u>19/</u>	t <sub>w(PGM)</sub>		All	9, 10, 11	95	105	μs
Delay time, program mode select to stabilization <u>19/</u>	t <sub>d(PGM-MODE)</sub>		All	9, 10, 11	10		μs
<b>Flash EEPROM – Erase operation</b>							
Pulse duration, erase algorithm <u>19/</u>	t <sub>w(ERASE)</sub>		All	9, 10, 11	6.65	7.35	ms
Delay time, erase mode select to stabilization <u>19/</u>	t <sub>d(ERASE-MODE)</sub>		All	9, 10, 11	10		μs
<b>Flash EEPROM – Flash-write operation</b>							
Pulse duration, flash-write algorithm <u>19/ 20/</u>	t <sub>w(FLW)</sub>		All	9, 10, 11	13.3	14.7	ms
Delay time, flash-write mode select to stabilization <u>19/ 20/</u>	t <sub>d(FLW-MODE)</sub>		All	9, 10, 11	10		μs
<b>JTAG timings</b>							
TMS/TDI setup to TCK high	t <sub>su</sub>	See figure 5	All	9, 10, 11	20		ns
TMS/TDI hold from TCK high	t <sub>h</sub>		All	9, 10, 11	15		ns
TCK low to TDO valid	t <sub>d</sub>		All	9, 10, 11		30	ns

See footnotes on next sheet.

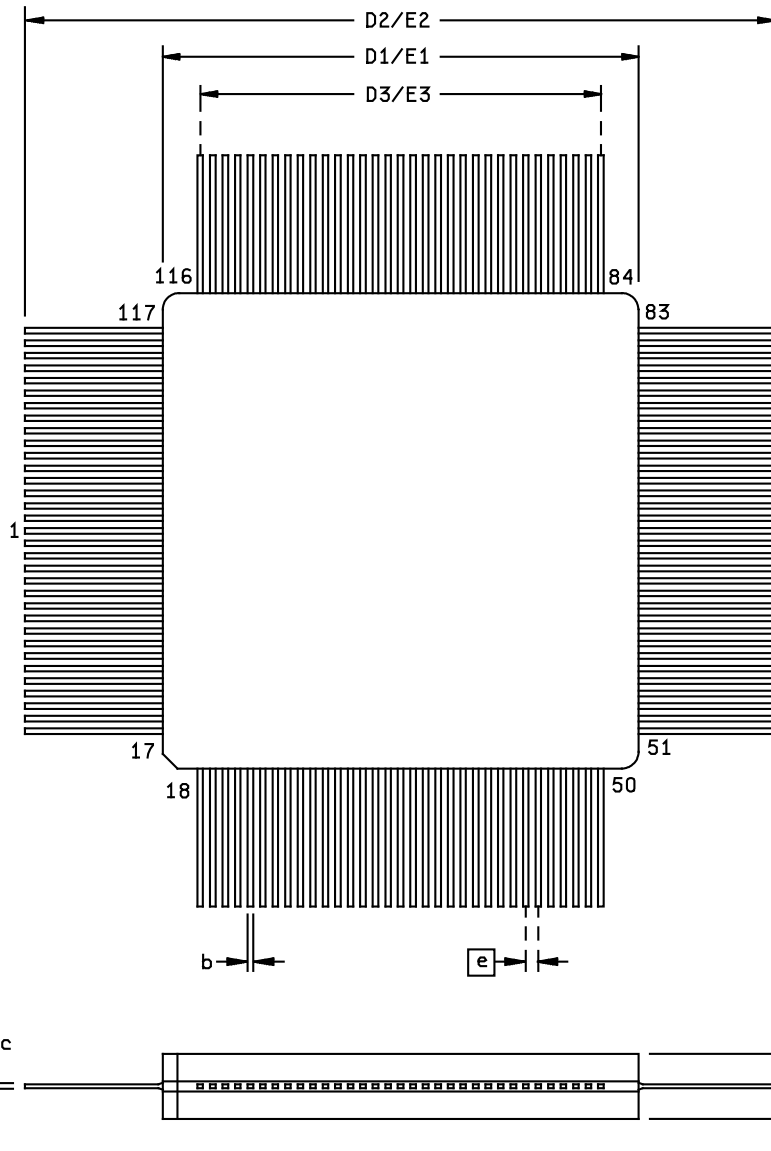
<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>21</b>

TABLE I. Electrical performance characteristics - Continued.

- 1/ Not production tested.
- 2/ This device utilizes a fully static design and, therefore, can operate with input clock cycle time  $[t_{c(CI)}]$  approaching infinity. The device is characterized at frequencies approaching 0 Hz.
- 3/ Timing assumes CLKOUT is set to output CPUCLK. CLKOUT is initialized to CPUCLK by power-on reset.
- 4/ SYSCLK is initialized to divide-by-4 mode by any device reset.
- 5/ All timings with respect to CLKOUT/IOPC1 assume CLKSRC[1:0] bits are set to select CPUCLK for output.
- 6/ The READY timings are based on one software wait state. At full speed operation, the device does not allow for single READY-based wait states.
- 7/ The parameter  $t_{w(RSL1)}$  refers to the time  $\overline{RS}$  is an output.
- 8/ The parameter  $t_{w(RSL)}$  refers to the time  $\overline{RS}$  is an input.
- 9/ This is the minimum time the MP/ $\overline{MC}$  pin needs to be stable in order to be recognized by internal logic; however, for proper operation, the user must maintain a valid level for the duration of the entire memory access (or accesses) on- or off-chip.
- 10/  $t_c$  = system clock cycle time =  $1/SYSCLK = t_{c(SYS)}$ .
- 11/ The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
- 12/ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).
- 13/ The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.
- 14/ The MASTER/SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
- 15/ The MASTER/SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is set.
- 16/ Absolute resolution = 4.89 mV. At  $V_{REFHI} = 5\text{ V}$  and  $V_{REFLO} = 0\text{ V}$ , this is one LSB. As  $V_{REFHI}$  decreases,  $V_{REFLO}$  increases, or both, the LSB sizes decrease. Therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.
- 17/ The total sample/hold and conversion time is determined by the summation of  $t_{d(SOC-SH)}$ ,  $t_{w(SH)}$ ,  $t_{w(C)}$ , and  $t_{d(EOC-FIFO)}$ .
- 18/ Start of conversion is signaled by the ADCIMSTART bit or the ADCSOC bit set in software, the external start signal active (ADCSOC), or internal EVSOC signal active.
- 19/ These parameters are used in the flash programming algorithms.
- 20/ Refer to the recommended operating conditions section for the flash programming operating temperature range when programming flash.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
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Case outline X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.79	3.81	.110	.150	D2/E2	37.08	39.12	1.460	1.540
b	0.20	0.36	.008	.014	D3/E3	20.32 TYP		.800 TYP	
c	0.10	0.20	.004	.008	e	0.635 BSC		.025 BSC	
D1/E1	23.75	24.51	.935	.965					

FIGURE 1. Case outline.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	<b>SIZE A</b>		<b>5962-98612</b>
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Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{WE}$	23	D10	45	SPISIMO/IO
2	DV <sub>DD</sub>	24	D11	46	V <sub>SS</sub>
3	V <sub>SS</sub>	25	D12	47	DV <sub>DD</sub>
4	R/ $\overline{W}$	26	D13	48	SPISOMI/IO
5	$\overline{BR}$	27	D14	49	SPICLK/IO
6	$\overline{STRB}$	28	D15	50	V <sub>CCP</sub> /WDDIS
7	CV <sub>DD</sub>	29	V <sub>SS</sub>	51	SPISTE/IO
8	CV <sub>SS</sub>	30	TCK	52	$\overline{PDPINT}$
9	D0	31	TDI	53	XINT1
10	D1	32	$\overline{TRST}$	54	XINT2/IO
11	D2	33	TMS	55	XINT3/IO
12	D3	34	TDO	56	$\overline{OSCBYP}$
13	DV <sub>DD</sub>	35	$\overline{RS}$	57	XTAL2
14	V <sub>SS</sub>	36	READY	58	XTAL1/CLKIN
15	D4	37	MP/ $\overline{MC}$	59	V <sub>SS</sub>
16	D5	38	EMU0	60	CV <sub>DD</sub>
17	D6	39	EMU1/ $\overline{OFF}$	61	V <sub>SS</sub>
18	D7	40	NMI	62	DV <sub>DD</sub>
19	D8	41	$\overline{PORESET}$	63	ADCSOC/IOPC0
20	V <sub>SS</sub>	42	RESERVED	64	CLKOUT/IOPC1
21	DV <sub>DD</sub>	43	SCIRXD/IO	65	XF/IOPC2
22	D9	44	SCITXD/IO	66	$\overline{BIO}$ /IOPC3

FIGURE 2. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>24</b>



Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
67	CAP1/QEP1/IOPC4	89	ADCIN10	111	A1
68	CAP2/QEP2/IOPC5	90	ADCIN9/IOPA2	112	A2
69	CAP3/IOPC6	91	ADCIN8/IOPA3	113	V <sub>SS</sub>
70	CAP4/IOPC7	92	V <sub>SS</sub>	114	A3
71	V <sub>SS</sub>	93	DV <sub>DD</sub>	115	A4
72	ADCIN0/IOPA0	94	PWM1/CMP1	116	A5
73	ADCIN1/IOPA1	95	PWM2/CMP2	117	A6
74	ADCIN2	96	PWM3/CMP3	118	A7
75	ADCIN3	97	PWM4/CMP4	119	A8
76	ADCIN4	98	PWM5/CMP5	120	V <sub>SS</sub>
77	ADCIN5	99	PWM6/CMP6	121	DV <sub>DD</sub>
78	ADCIN6	100	PWM7/CMP7/IOPB0	122	A9
79	ADCIN7	101	PWM8/CMP8/IOPB1	123	A10
80	ADCIN15	102	PWM9/CMP9/IOPB2	124	A11
81	ADCIN14	103	DV <sub>DD</sub>	125	A12
82	ADCIN13	104	V <sub>SS</sub>	126	A13
83	ADCIN12	105	T1PWM/T1CMP/IOPB3	127	A14
84	V <sub>CCA</sub>	106	T2PWM/T2CMP/IOPB4	128	A15
85	V <sub>REFHI</sub>	107	T3PWM/T3CMP/IOPB5	129	$\overline{DS}$
86	V <sub>REFLO</sub>	108	TMRDIR/IOPB6	130	$\overline{IS}$
87	V <sub>SSA</sub>	109	TMRCLK/IOPB7	131	$\overline{PS}$
88	ADCIN11	110	A0	132	W/ $\overline{R}$

FIGURE 2. Terminal connections - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>25</b>

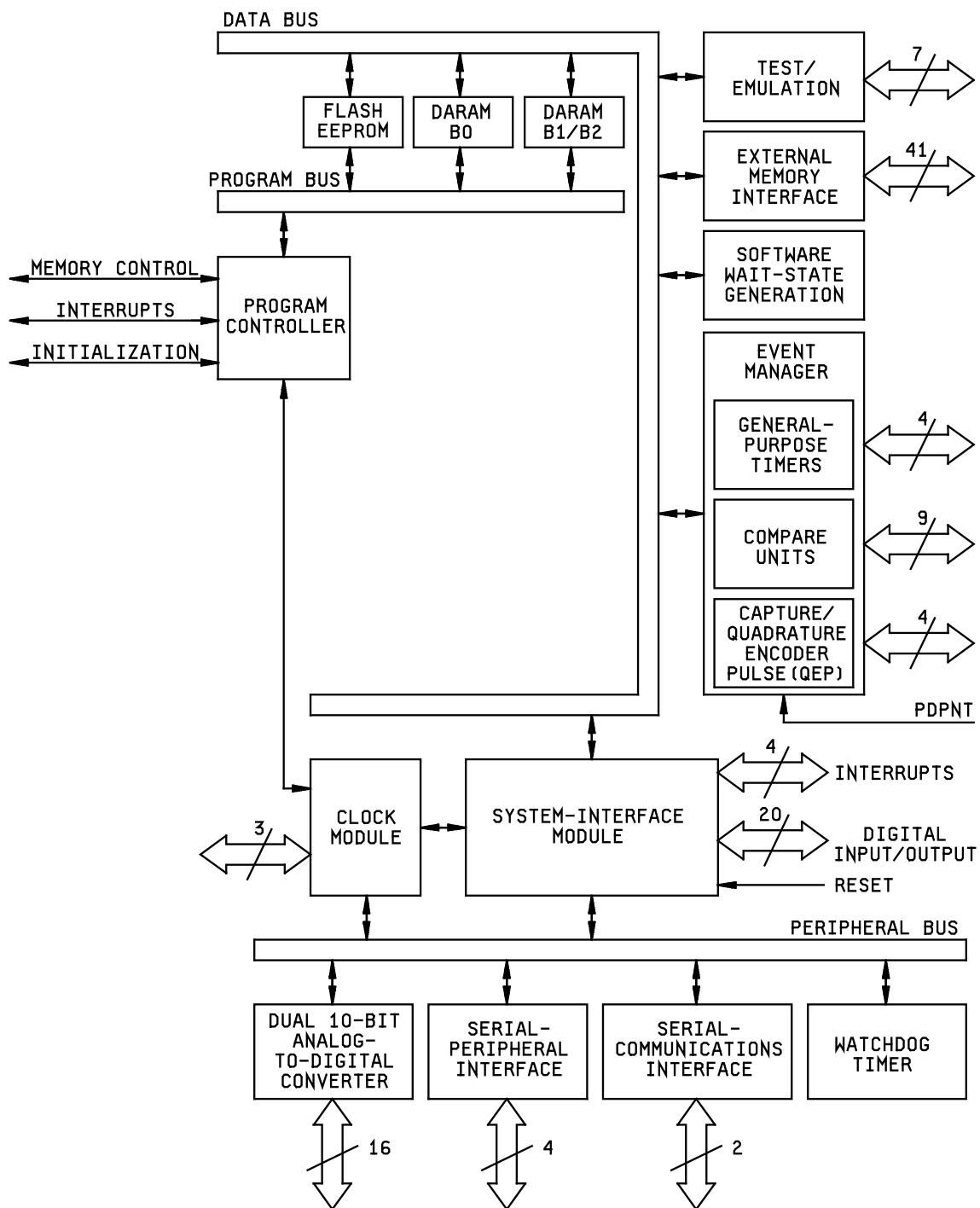


FIGURE 3. Block diagram.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

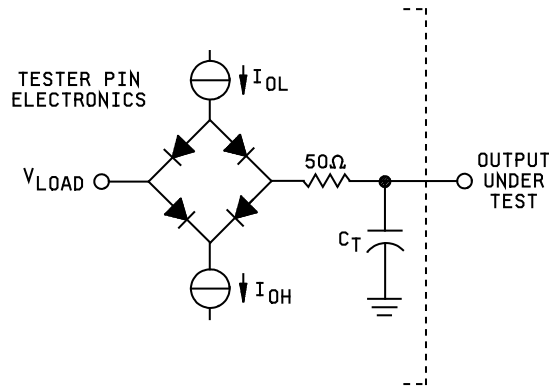
**5962-98612**

REVISION LEVEL  
**F**

SHEET  
**26**

Instruction code	Instruction name
00000000	EXTEST
11111111	BYPASS
00000010	SAMPLE
00000110	TRIBYP
00000011	INTEST

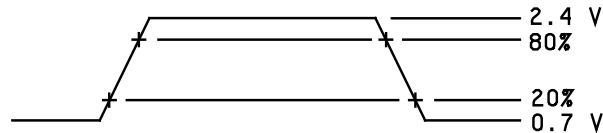
FIGURE 4. Boundary scan instruction codes.



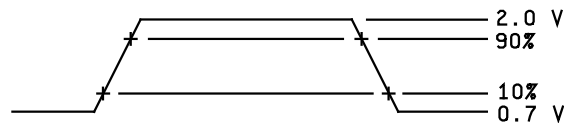
NOTES:

- $I_{OL}$  = 2 mA (all outputs)
- $I_{OH}$  = 300  $\mu$ A (all outputs)
- $V_{LOAD}$  = 1.5 V
- $C_T$  = 110-pF typical load-circuit capacitance

TEST LOAD CIRCUIT



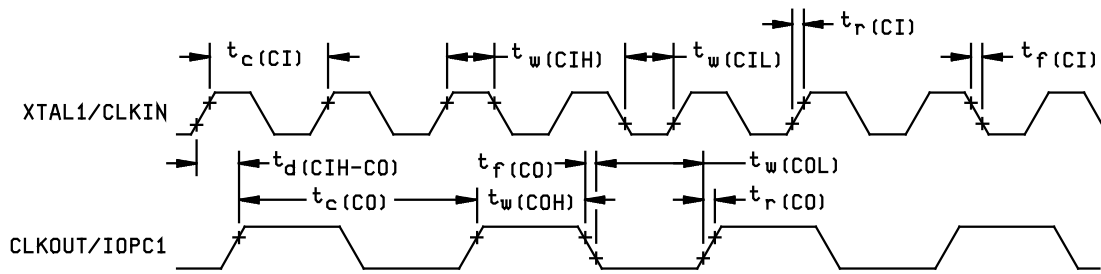
TTL-LEVEL OUTPUTS



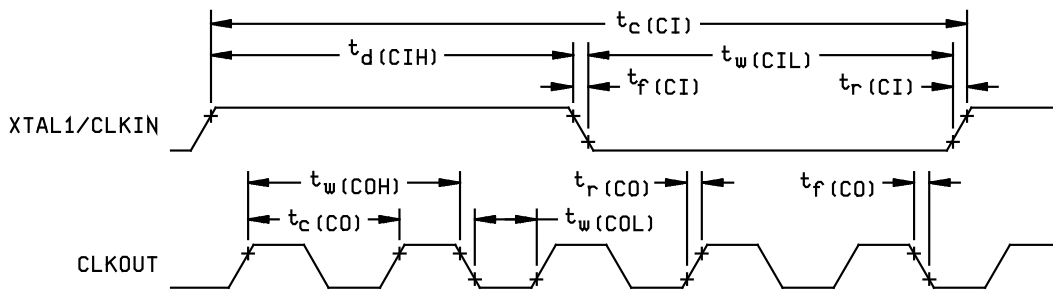
TTL-LEVEL INPUTS

FIGURE 5. Test circuit and timing waveforms.

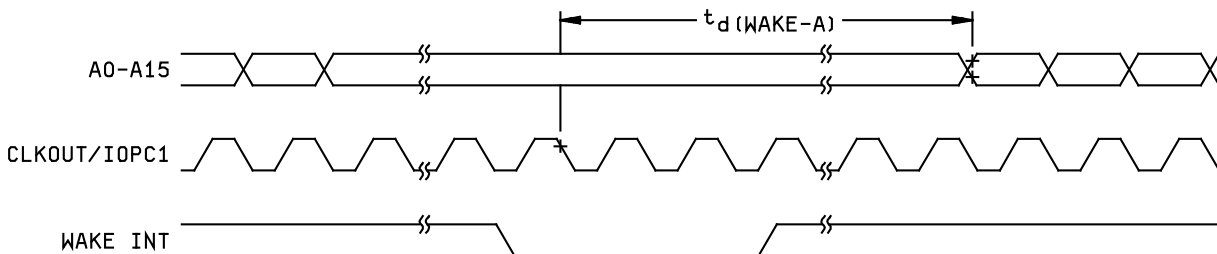
<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>27</b>



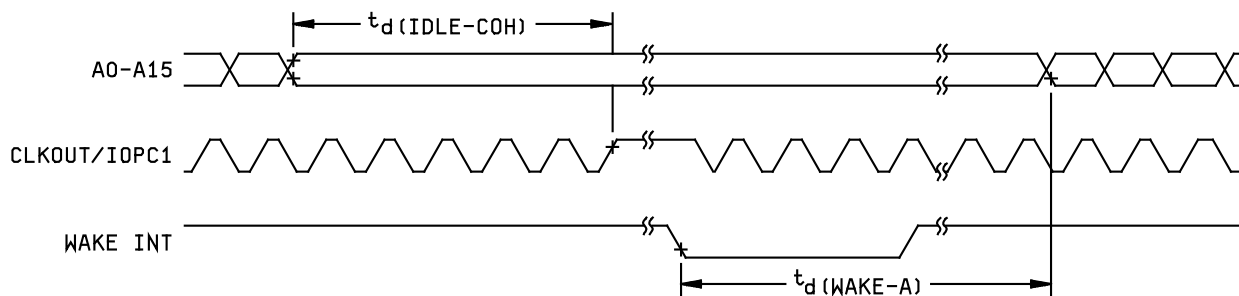
EXTERNAL DIVIDE-BY-TWO CLOCK TIMINGS



CLKIN-TO-CLKOUT TIMINGS FOR PLL OSCILLATOR MODE,  
MULTIPLY-BY-5 OPTION WITH 4-MHz CRYSTAL



IDLE1 ENTRY AND EXIT TIMINGS



IDLE2 ENTRY AND EXIT TIMINGS

FIGURE 5. Test circuit and timing waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>28</b>

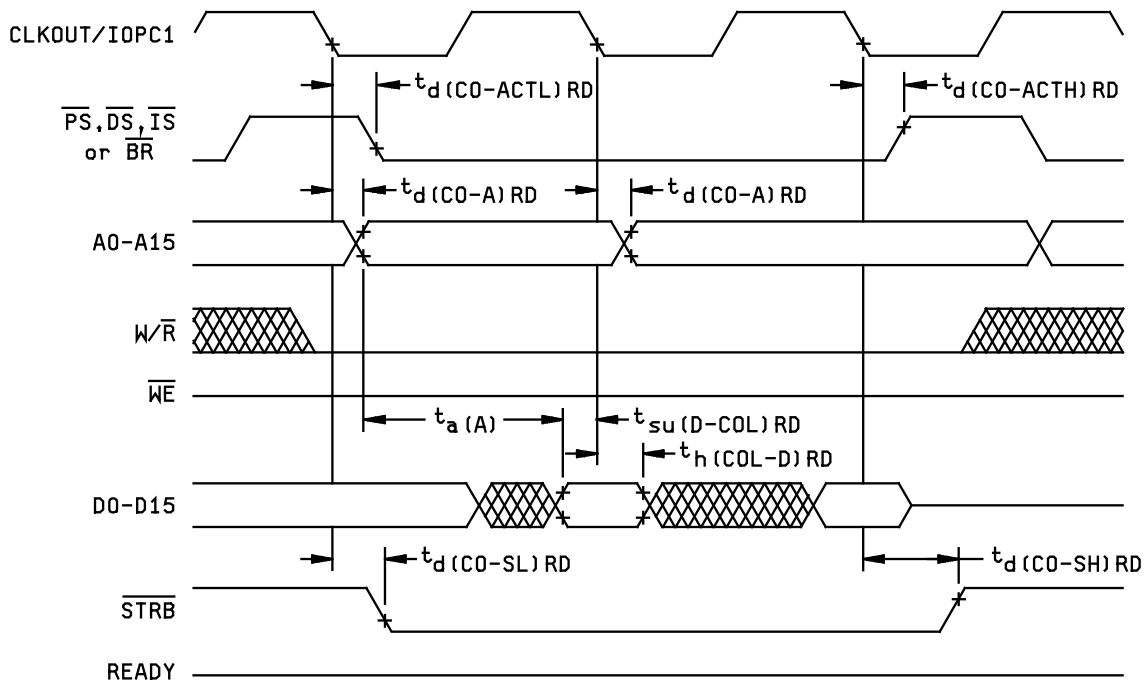
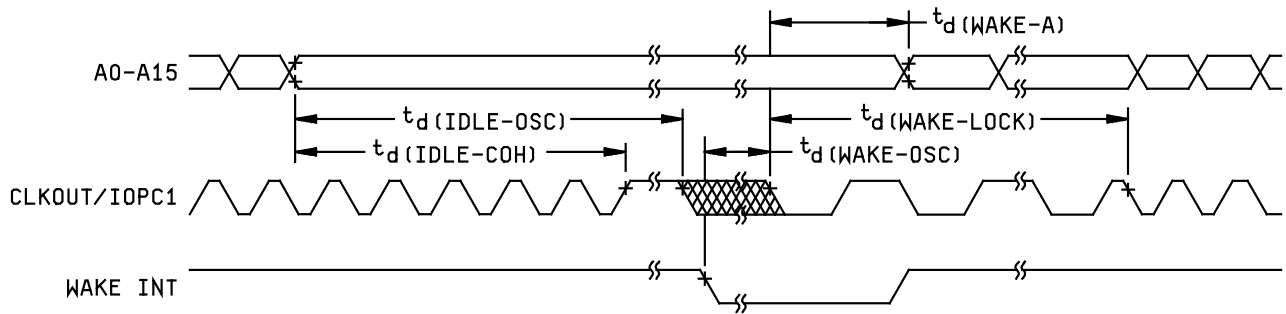
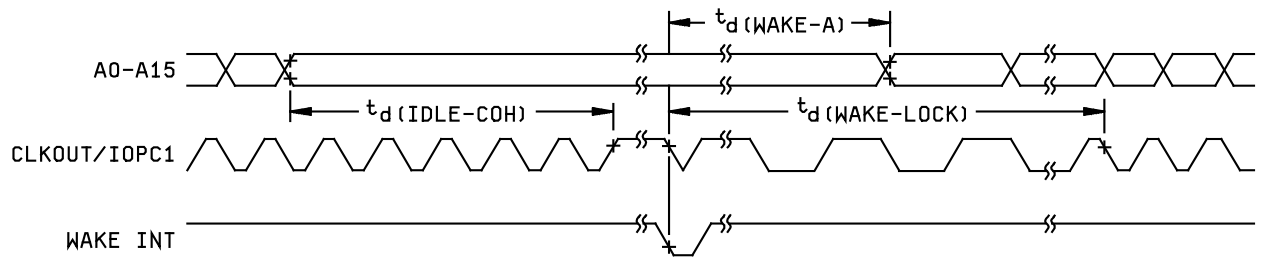


FIGURE 5. Test circuit and timing waveforms - Continued.

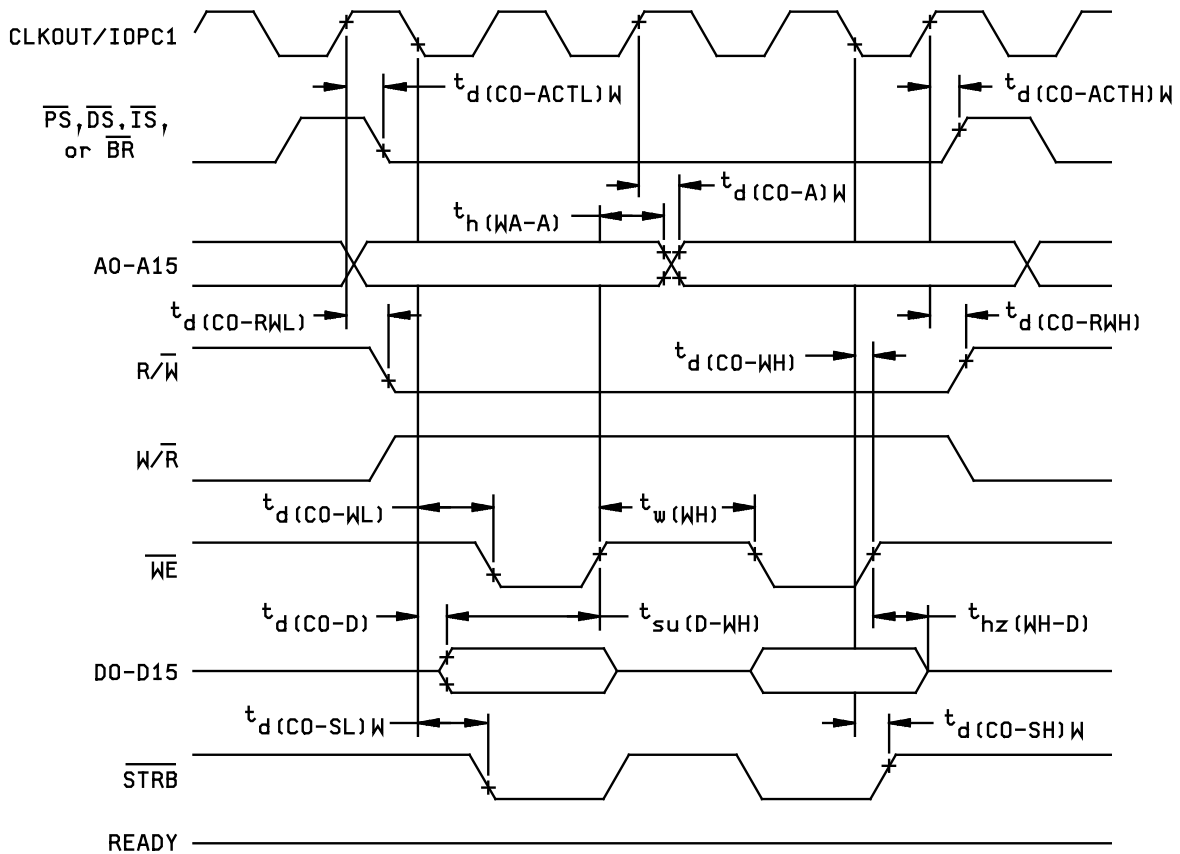
**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-98612**

REVISION LEVEL  
**F**

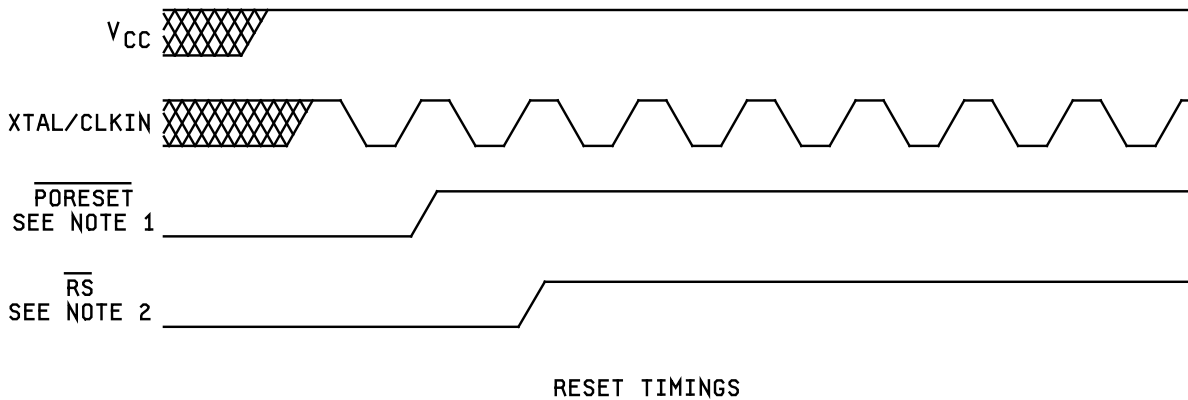
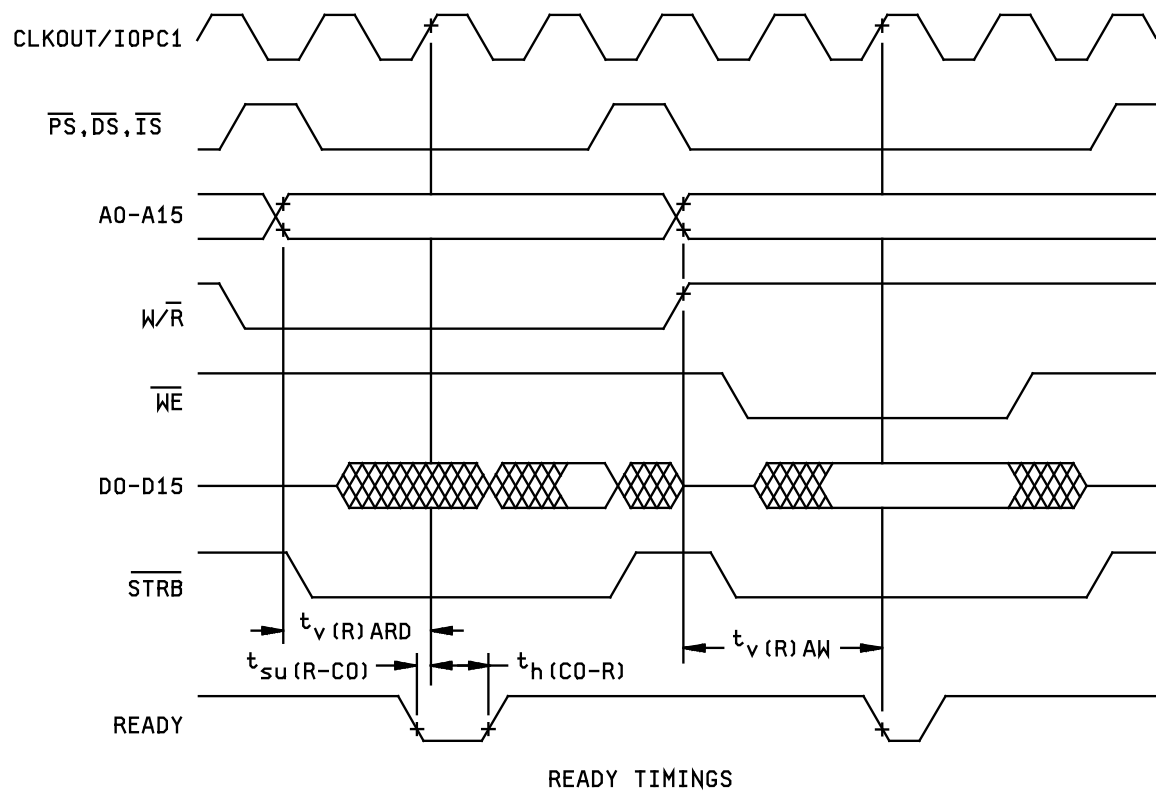
SHEET  
**29**



MEMORY INTERFACE WRITE TIMINGS

FIGURE 5. Test circuit and timing waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>30</b>

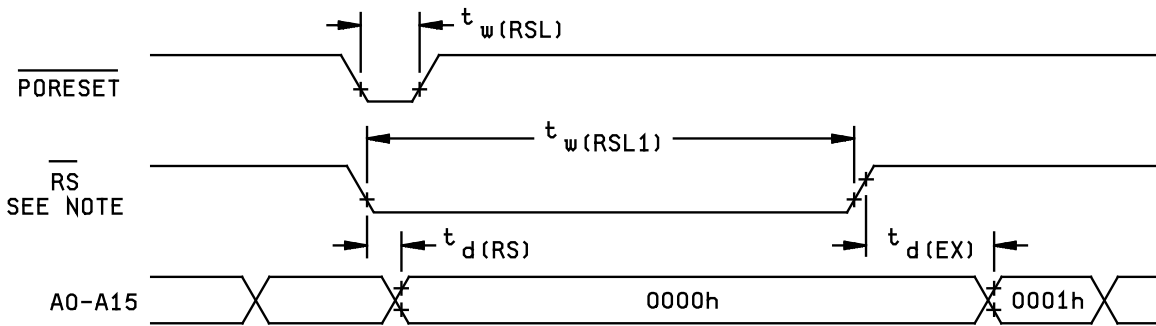


NOTES:

1.  $\overline{\text{PORESET}}$  is required to be driven low during power up to ensure all clock/PLL registers are reset to a known state.
2.  $\overline{\text{RS}}$  is a bidirectional (open-drain output) pin and can be optionally pulled low through an open-drain or open-collector drive circuit, or through a 2.7-k $\Omega$  resistor in series with a totem pole drive circuit. If  $\overline{\text{RS}}$  is left undriven, then a 20-k $\Omega$  pullup resistor should be used.

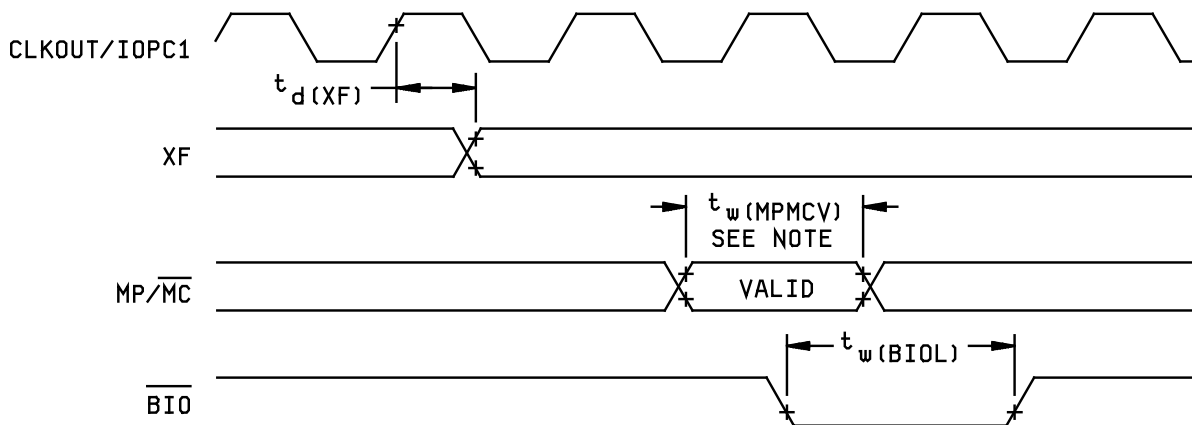
FIGURE 5. Test circuit and timing waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>31</b>



POWER-ON RESET TIMINGS

NOTE:  $\overline{\text{RS}}$  is driven low by any device reset, which includes asserting  $\overline{\text{PORESET}}$ ,  $\overline{\text{RS}}$ , access to an illegal address, execution of a software reset, or a watchdog timer reset.

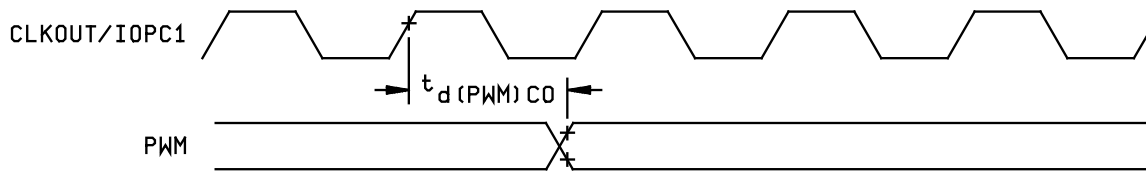


$\text{XF}$ ,  $\overline{\text{BIO}}$ , AND  $\text{MP}/\overline{\text{MC}}$  TIMINGS

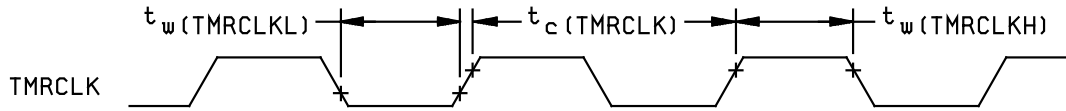
FIGURE 5. Test circuit and timing waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>32</b>

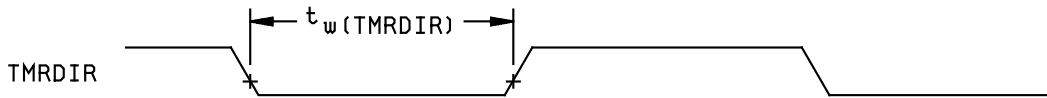




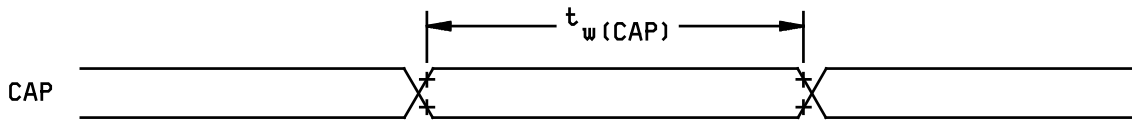
PWM AND COMPARE OUTPUT TIMINGS



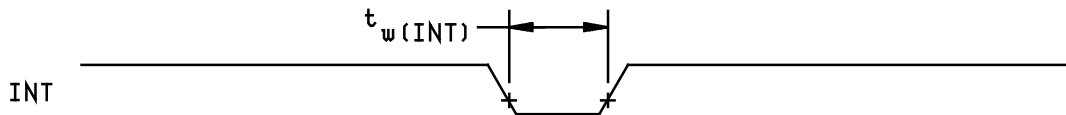
EXTERNAL TIMER CLOCK INPUT TIMINGS



EXTERNAL TIMER DIRECTION INPUT TIMINGS



CAPTURE AND QEP INPUT TIMINGS



EXTERNAL INTERRUPT TIMINGS

FIGURE 5. Test circuit and timing waveforms - Continued.

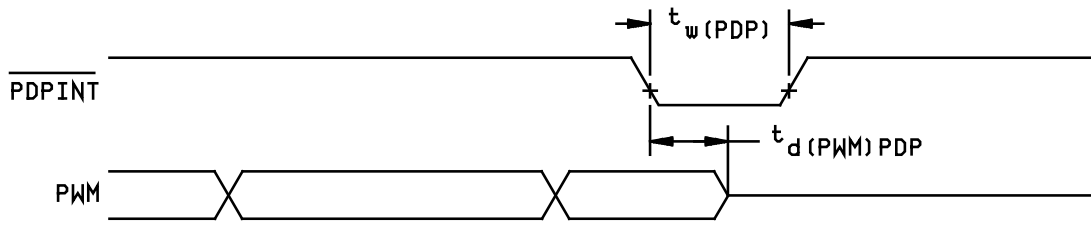
**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

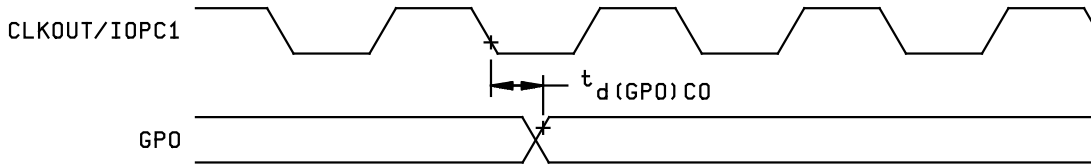
**5962-98612**

REVISION LEVEL  
**F**

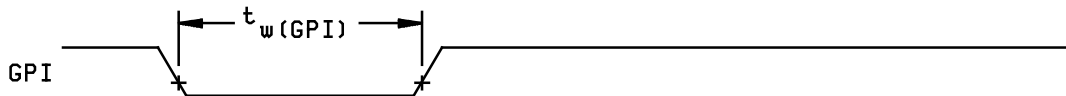
SHEET  
**33**



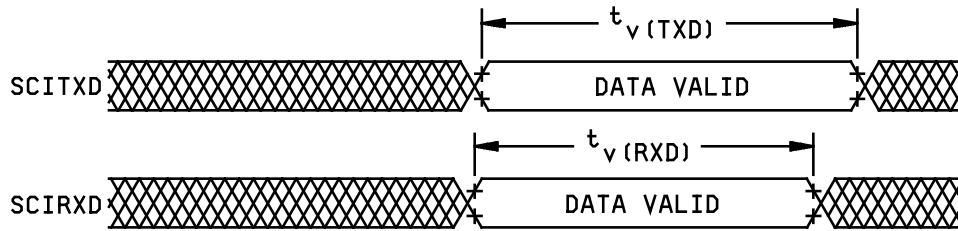
POWER-DRIVE PROTECTION INTERRUPT TIMINGS



GENERAL-PURPOSE OUTPUT TIMINGS



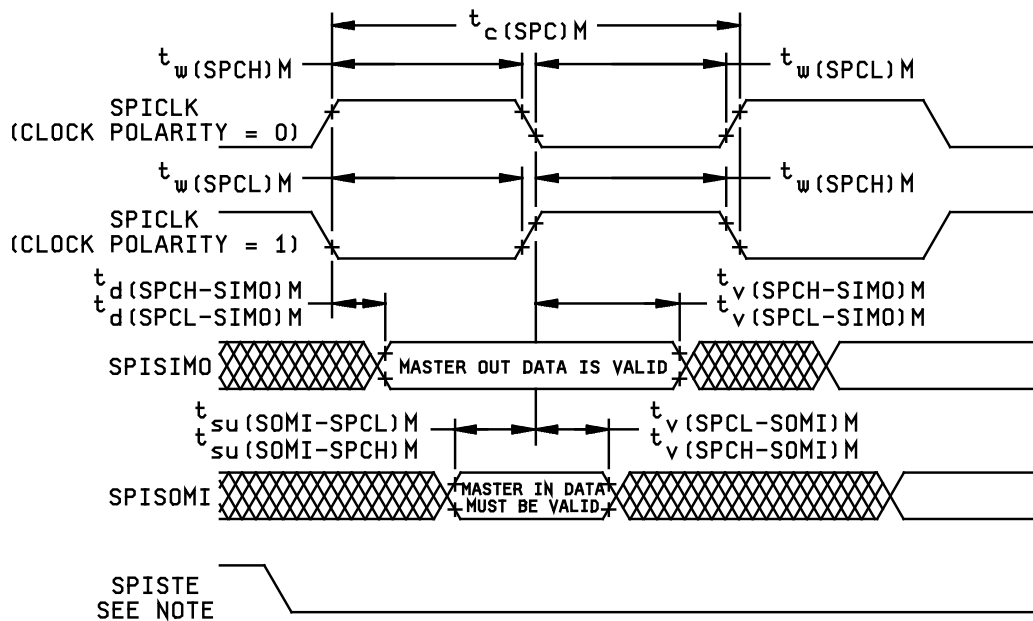
GENERAL-PURPOSE INPUT TIMINGS



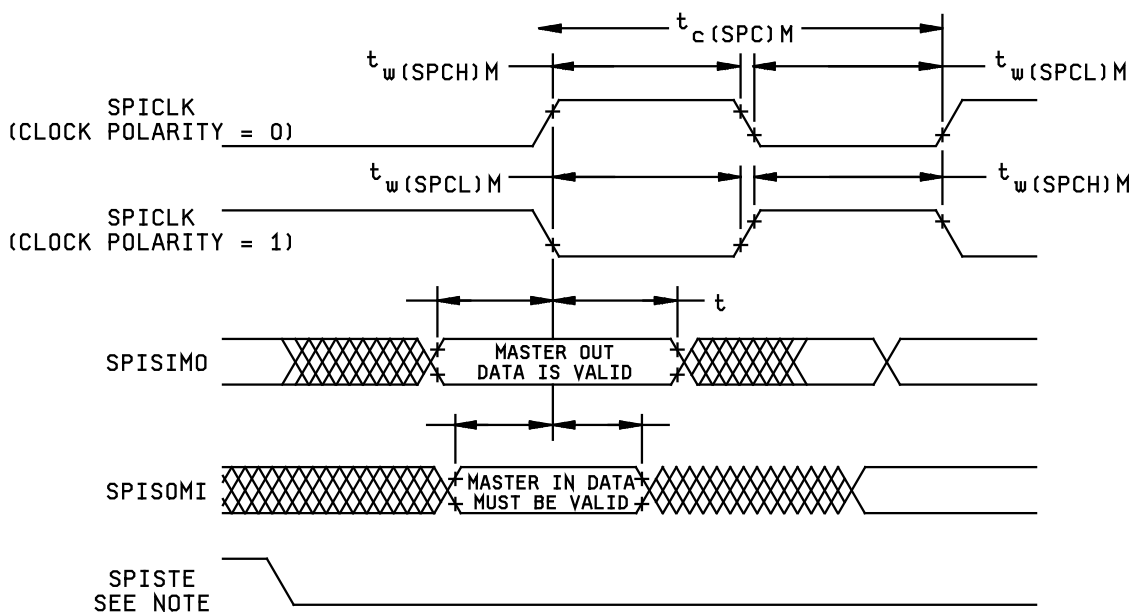
SCI TIMINGS

FIGURE 5. Test circuit and timing waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>34</b>



SPI MASTER MODE EXTERNAL TIMINGS (CLOCK PHASE = 0)

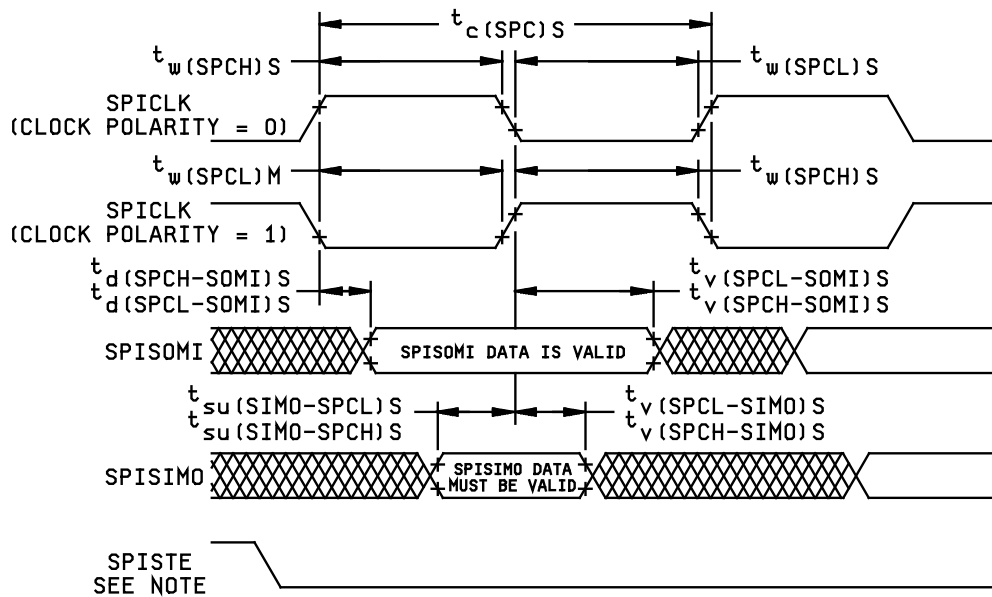


SPI MASTER MODE EXTERNAL TIMINGS (CLOCK PHASE = 1)

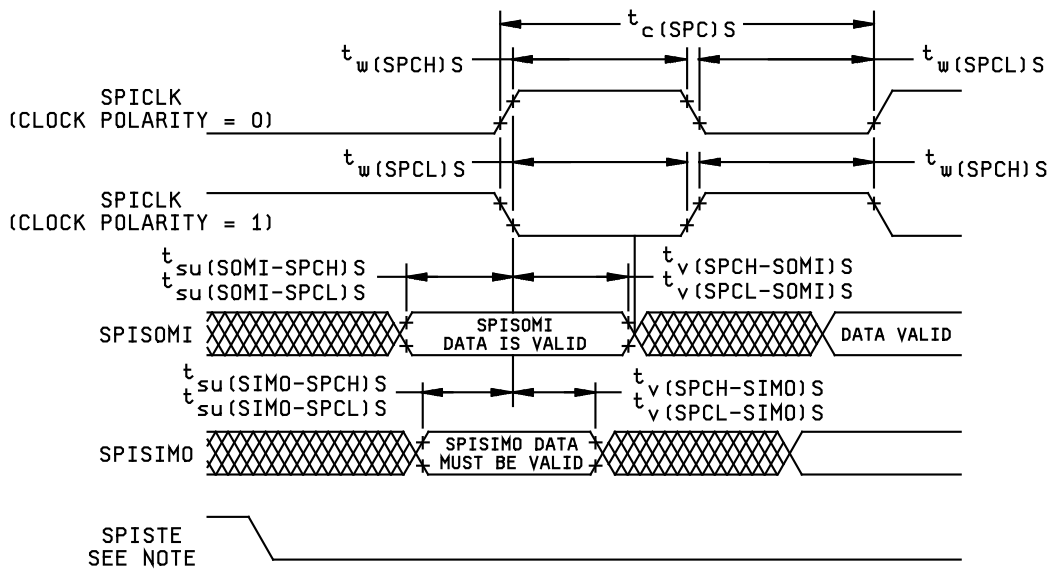
NOTE: The SPISTE signal must be active before the SPI communication stream starts; the SPISTE signal must remain active until the SPI communication stream is complete.

FIGURE 5. Test circuit and timing waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	<b>SIZE A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>35</b>



SPI SLAVE MODE EXTERNAL TIMING (CLOCK PHASE = 0)

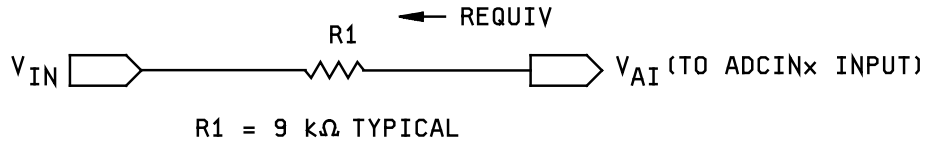


SPI SLAVE MODE EXTERNAL TIMING (CLOCK PHASE = 1)

NOTE: The SPISTE signal must be active before the SPI communication stream starts; the SPISTE signal must remain active until the SPI communication stream is complete.

FIGURE 5. Test circuit and timing waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>36</b>



TYPICAL ADC INPUT PIN CIRCUIT

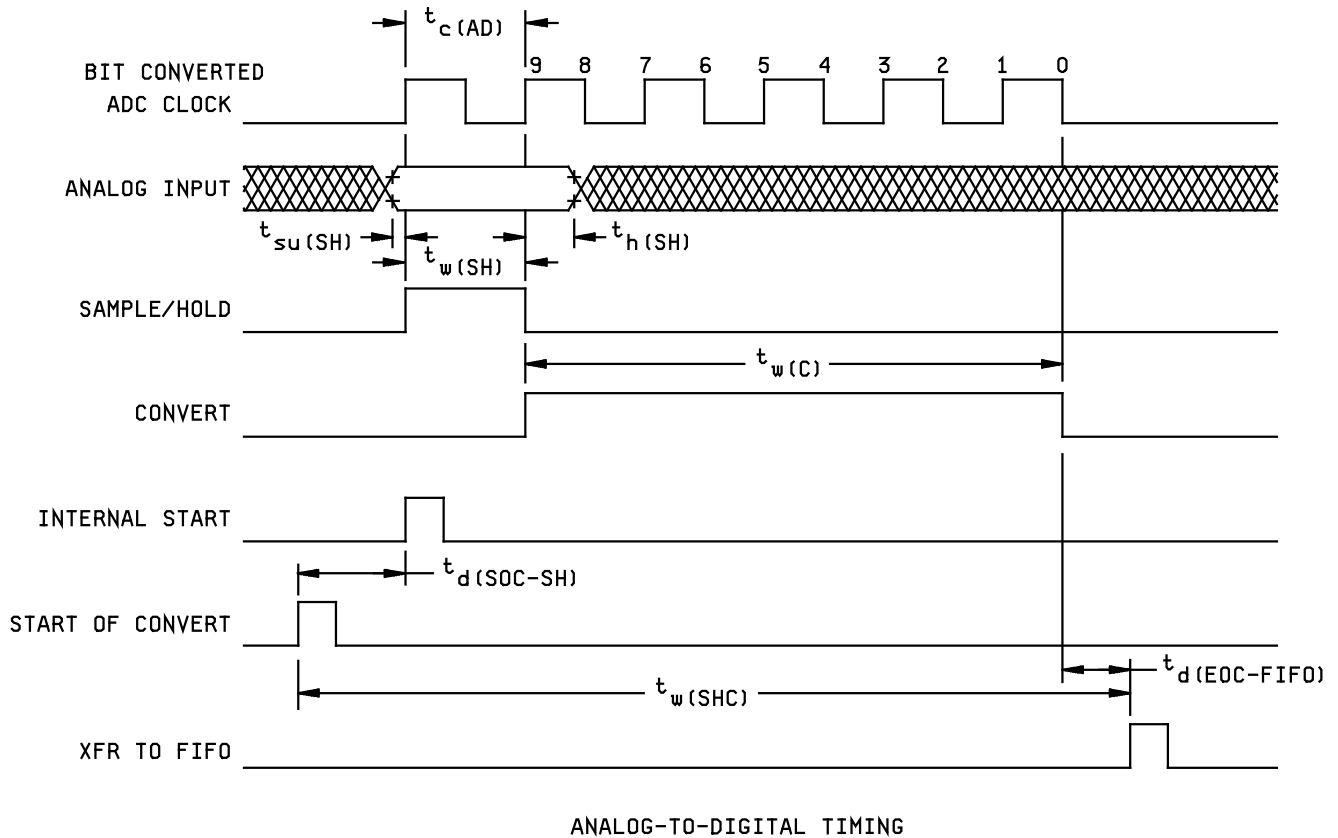
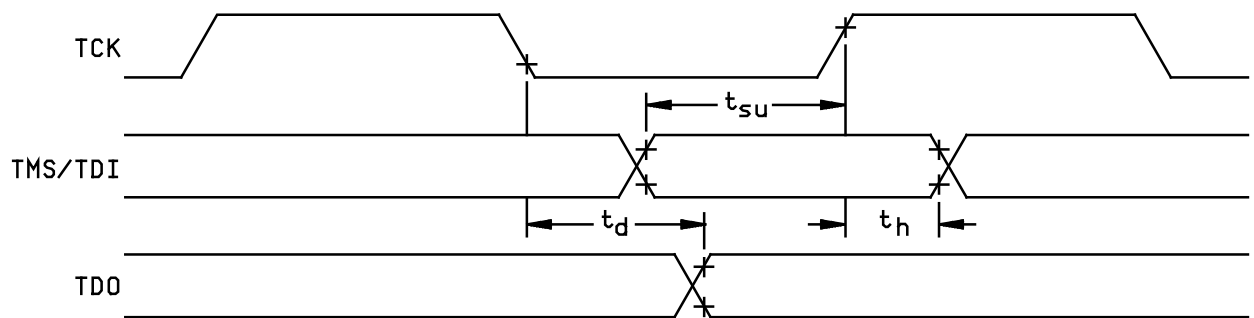


FIGURE 5. Test circuit and timing waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>37</b>



JTAG TIMING

FIGURE 5. Test circuit and timing waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>38</b>

#### 4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

##### 4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

##### 4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. Subgroup 4 ( $C_i$  and  $C_o$  measurements) shall be measured only for initial test and after process or design changes which may affect input and output capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ , after exposure, to the subgroups specified in table II herein.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>41</b>

TABLE III. Terminal descriptions.

Terminal name	Type 1/	Description
<b>EXTERNAL INTERFACE DATA/ADDRESS SIGNALS</b>		
A0 through A15	O/Z	Parallel address bus A0 [least significant bit (LSB)] through A15 [most significant bit (MSB)]. A15-A0 are multiplexed to address external data/program memory or I/O. A15-A0 are placed in the high-impedance state when EMU1/ $\overline{\text{OFF}}$ is active low and hold their previous states in power-down modes.
D0 through D15	I/O/Z	Parallel data bus D0 (LSB) through D15 (MSB). D15-D0 are multiplexed to transfer data between the device and external data/program memory and I/O space (devices). D15-D0 are placed in the high-impedance state when not outputting, when in power-down mode, when reset ( $\overline{\text{RS}}$ ) is asserted, or when EMU1/ $\overline{\text{OFF}}$ is active low.
<b>EXTERNAL INTERFACE CONTROL SIGNALS</b>		
$\overline{\text{DS}}$ , $\overline{\text{PS}}$ , $\overline{\text{IS}}$	O/Z	Data, program, and I/O space select signals. $\overline{\text{DS}}$ , $\overline{\text{PS}}$ , and $\overline{\text{IS}}$ are always high unless low-level asserted for communication to a particular external space. They are placed in the high-impedance state during reset, power down, and when EMU1/ $\overline{\text{OFF}}$ is active low.
READY	I	Data ready. READY indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again.
R/ $\overline{\text{W}}$	O/Z	Read/write signal. R/ $\overline{\text{W}}$ indicates transfer direction during communication to an external device. It is normally in read mode (high), unless low level is asserted for performing a write operation. It is placed in the high-impedance state during reset, power down, and when EMU1/ $\overline{\text{OFF}}$ is active low.
$\overline{\text{STRB}}$	O/Z	Strobe. $\overline{\text{STRB}}$ is always high unless asserted low to indicate an external bus cycle. It is placed in the high-impedance state during reset, power down, and when EMU1/ $\overline{\text{OFF}}$ is active low.
$\overline{\text{WE}}$	O/Z	Write enable. The falling edge of $\overline{\text{WE}}$ indicates that the device is driving the external data bus (D15-D0). Data can be latched by an external device on the rising edge of $\overline{\text{WE}}$ . $\overline{\text{WE}}$ is active on all external program, data, and I/O writes. $\overline{\text{WE}}$ goes in the high-impedance state following reset and when EMU1/ $\overline{\text{OFF}}$ is active low.
W/ $\overline{\text{R}}$	O/Z	Write/read. W/ $\overline{\text{R}}$ is an inverted form of R/ $\overline{\text{W}}$ and can connect directly to the output enable of external devices. W/ $\overline{\text{R}}$ is placed in the high-impedance state following reset and when EMU1/ $\overline{\text{OFF}}$ is active low.
$\overline{\text{BR}}$	O/Z	Bus request. $\overline{\text{BR}}$ is asserted during access of external global data memory space. $\overline{\text{BR}}$ can be used to extend the data memory address space by up to 32K words. $\overline{\text{BR}}$ goes in the high-impedance state during reset, power down, and when EMU1/ $\overline{\text{OFF}}$ is active low.
V <sub>CCP</sub> /WDDIS	I	Flash-programming voltage supply. If V <sub>CCP</sub> = 5 V, then WRITE/ERASE can be made to the ENTIRE on-chip flash memory block - that is, for programming the flash. If V <sub>CCP</sub> = 0 V, then WRITE/ERASE of the flash memory is not allowed, thereby protecting the entire memory block from being overwritten. WDDIS also functions as a hardware watchdog disable. The watchdog timer is disabled when V <sub>CCP</sub> /WDDIS = 5 V and bit 6 in WDCR is set to 1.

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-98612</b>
		REVISION LEVEL <b>F</b>	SHEET <b>42</b>

TABLE III. Terminal descriptions – Continued.

Terminal name	Type 1/	Description
<b>ADC INPUTS (UNSHARED)</b>		
ADCIN2 through ADCIN7	I	Analog inputs to the first ADC.
ADCIN10 through ADCIN15	I	Analog inputs to the second ADC
<b>BIT I/O AND SHARED FUNCTIONS PINS</b>		
ADCIN0/IOPA0	I/O	Bidirectional digital I/O. Analog input to the first ADC. ADCIN0/IOPA0 is configured as a digital input by all device resets.
ADCIN1/IOPA1	I/O	Bidirectional digital I/O. Analog input to the first ADC. ADCIN1/IOPA1 is configured as a digital input by all device resets.
ADCIN9/IOPA2	I/O	Bidirectional digital I/O. Analog input to the second ADC. ADCIN9/IOPA2 is configured as a digital input by all device resets.
ADCIN8/IOPA3	I/O	Bidirectional digital I/O. Analog input to the second ADC. ADCIN8/IOPA3 is configured as a digital input by all device resets.
PWM7/CMP7/ IOPB0	I/O/Z	Bidirectional digital I/O. Simple compare/PWM 1 output. The state of PWM7/CMP7/IOPB0 is determined by the simple compare/PWM and the simple action control register (SACTR). It goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. PWM7/CMP7/IOPB0 is configured as a digital input by all device resets.
PWM8/CMP8/ IOPB1	I/O/Z	Bidirectional digital I/O. Simple compare/PWM 2 output. The state of PWM8/CMP8/IOPB1 is determined by the simple compare/PWM and the SACTR. It goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. PWM8/CMP8/IOPB1 is configured as a digital input by all device resets.
PWM9/CMP9/ IOPB2	I/O/Z	Bidirectional digital I/O. Simple compare/PWM 3 output. The state of PWM9/CMP9/IOPB2 is determined by the simple compare/PWM and the SACTR. It goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. PWM9/CMP9/IOPB2 is configured as a digital input by all device resets.
T1PWM/T1CMP/ IOPB3	I/O/Z	Bidirectional digital I/O. Timer 1 compare output. T1PWM/T1CMP/IOPB3 goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. This pin is configured as a digital input by all device resets.
T2PWM/T2CMP/ IOPB4	I/O/Z	Bidirectional digital I/O. Timer 2 compare output. T2PWM/T2CMP/IOPB4 goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. This pin is configured as a digital input by all device resets.
T3PWM/T3CMP/ IOPB5	I/O/Z	Bidirectional digital I/O. Timer 3 compare output. T3PWM/T3CMP/IOPB5 goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. This pin is configured as a digital input by all device resets.
TMRDIR/IOPB6	I/O	Bidirectional digital I/O. Direction signal for the timers. Up-counting direction if TMRDIR/IOPB6 is low, down-counting direction if this pin is high. This pin is configured as a digital input by all device resets.
TMRCLK/IOPB7	I/O	Bidirectional digital I/O. External clock input for general-purpose timers. This pin is configured as a digital input by all device resets.

See footnotes at end of table.

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TABLE III. Terminal descriptions – Continued.

Terminal name	Type 1/	Description
<b>BIT I/O AND SHARED FUNCTIONS PINS – CONTINUED</b>		
ADCSOC/IOPC0	I/O	Bidirectional digital I/O. External start of conversion input for ADC. This pin is configured as a digital input by all device resets.
CAP1/QEP1/ IOPC4	I/O	Bidirectional digital I/O. Capture 1 or QEP 1 input. This pin is configured as a digital input by all device resets.
CAP2/QEP2/ IOPC5	I/O	Bidirectional digital I/O. Capture 2 or QEP 2 input. This pin is configured as a digital input by all device resets.
CAP3/IOPC6	I/O	Bidirectional digital I/O. Capture 3 input. This pin is configured as a digital input by all device resets.
CAP4/IOPC7	I/O	Bidirectional digital I/O. Capture 4 input. This pin is configured as a digital input by all device resets.
XF/IOPC2	I/O	Bidirectional digital I/O. External flag output (latched software-programmable signal). XF is used for signaling other processors in multiprocessing configurations or as a general-purpose output pin. This pin is configured as an external flag output by all device resets.
$\overline{\text{BIO}}$ /IOPC3	I/O	Bidirectional digital I/O. Branch control input. $\overline{\text{BIO}}$ is polled by the BIOZ instruction. If $\overline{\text{BIO}}$ is low, the CPU executes a branch. If $\overline{\text{BIO}}$ is not used, it should be pulled high. This pin is configured as a branch-control input by all device resets.
CLKOUT/IOPC1	I/O	Bidirectional digital I/O. Clock output. Clock output is selected by the CLKSRC bits in the SYSCR register. This pin is configured as a DSP clock output by a power-on reset.
<b>SERIAL COMMUNICATIONS INTERFACE (SCI) AND BIT I/O PINS</b>		
SCITXD/IO	I/O	SCI asynchronous serial port transmit data, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SCIRXD/IO	I/O	SCI asynchronous serial port receive data, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
<b>SERIAL PERIPHERAL INTERFACE (SPI) AND BIT I/O PINS</b>		
SPISIMO/IO	I/O	SPI slave in, master out, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SPISOMI/IO	I/O	SPI slave out, master in, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SPICLK/IO	I/O	SPI clock, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SPISTE/IO	I/O	SPI slave transmit enable (optional), or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
<b>COMPARE SIGNALS</b>		
PWM1/CMP1 through PWM6/CMP6	O/Z	Compare units compare or PWM outputs. The state of these pins is determined by the compare/PWM and the full action control register (ACTR). CMP1-CMP6 go to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low, and when reset ( $\overline{\text{RS}}$ ) is asserted.

See footnotes at end of table.

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TABLE III. Terminal descriptions – Continued.

Terminal name	Type 1/	Description
<b>INTERRUPT AND MISCELLANEOUS SIGNALS</b>		
$\overline{RS}$	I/O	Reset input. $\overline{RS}$ causes the device to terminate execution and sets PC = 0. When $\overline{RS}$ is brought to a high level, execution begins at location zero of program memory. $\overline{RS}$ affects (or sets to zero) various registers and status bits. $\overline{RS}$ is a bidirectional (open-drain output) pin.
MP/ $\overline{MC}$	I	MP/ $\overline{MC}$ (microprocessor/microcomputer) select. If MP/ $\overline{MC}$ is low, internal program memory is selected. If it is high, external program memory is selected.
NMI	I	Nonmaskable interrupt. When NMI is activated, the device is interrupted regardless of the state of the INTM bit of the status register. NMI has programmable polarity.
$\overline{PORESET}$	I	Power-on reset. $\overline{PORESET}$ causes the device to terminate execution and sets PC = 0. When $\overline{PORESET}$ is brought to a high level, execution begins at location zero of program memory. $\overline{PORESET}$ affects (or sets to zero) the same registers and status bits as $\overline{RS}$ . In addition, $\overline{PORESET}$ initializes the PLL control registers.
XINT1	I	External user interrupt no. 1.
XINT2/IO	I/O	External user interrupt no. 2. General-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
XINT3/IO	I/O	External user interrupt no. 3. General-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
$\overline{PDPINT}$	I	Maskable power-drive protection interrupt. If $\overline{PDPINT}$ is unmasked and it goes active low, the timer compare outputs immediately go to the high-impedance state.
<b>CLOCK SIGNALS</b>		
XTAL2	O	PLL oscillator output. XTAL2 is tied to one side of a reference crystal when the device is in PLL mode (CLKMD[1:0] = 1x, CKCR0.7-6). This pin can be left unconnected in oscillator bypass mode ( $\overline{OSCBYP} \leq V_{IL}$ ). This pin goes in the high-impedance state when EMU1/ $\overline{OFF}$ is active low.
XTAL1/CLKIN	I/Z	PLL oscillator input. XTAL1/CLKIN is tied to one side of a reference crystal in PLL mode (CLKMD[1:0] = 1x, CKCR0.7-6), or is connected to an external clock source in oscillator bypass mode ( $\overline{OSCBYP} \leq V_{IL}$ ).
$\overline{OSCBYP}$	I	Bypass oscillator if low.
<b>SUPPLY SIGNALS</b>		
CV <sub>SS</sub>	I	Digital core logic ground reference.
V <sub>SS</sub>	I	Digital logic ground reference.
V <sub>SSA</sub>	I	Analog ground reference.
DV <sub>DD</sub> <u>2/</u>	I	Digital I/O logic supply voltage.
CV <sub>DD</sub> <u>2/</u>	I	Digital core logic supply voltage.

See footnotes at end of table.

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TABLE III. Terminal descriptions – Continued.

Terminal name	Type 1/	Description
<b>SUPPLY SIGNALS – CONTINUED</b>		
V <sub>CCA</sub>	I	Analog supply voltage.
V <sub>REFHI</sub>	I	ADC analog voltage reference high.
V <sub>REFLO</sub>	I	ADC analog voltage reference low.
<b>TEST SIGNALS</b>		
TCK	I	IEEE standard test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test-access port (TAP) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test data register of the device core on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard test data input (TDI). TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state when $\overline{\text{OFF}}$ is active low.
TMS	I	IEEE standard test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$	I	IEEE standard test reset. $\overline{\text{TRST}}$ , when active low, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored.
EMU0	I/O/Z	Emulator pin 0. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output through the scan.
EMU1/ $\overline{\text{OFF}}$	I/O/Z	Emulator pin 1/disable all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/ $\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output through JTAG scan. When $\overline{\text{TRST}}$ is driven low, this pin is configured as $\overline{\text{OFF}}$ . When EMU1/ $\overline{\text{OFF}}$ is active low, it puts all output drivers in the high-impedance state. $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications); therefore, for $\overline{\text{OFF}}$ condition, the following conditions apply: $\overline{\text{TRST}}$ = low, EMU0 = high, EMU1/ $\overline{\text{OFF}}$ = low.
RESERVED	I	Reserved for test. This pin has an internal pulldown and must be left unconnected for the device.

1/ I = Input; O = Output; Z = High impedance.

2/ V<sub>DD</sub> refers to supply voltage types CV<sub>DD</sub> (digital core supply voltage), DV<sub>DD</sub> (digital I/O supply voltage), and V<sub>DDP</sub> (programming voltage supply). All voltages are measured with respect to V<sub>SS</sub>.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-05-08

Approved sources of supply for SMD 5962-98612 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9861201QXA	01295	SMJ320F240HFPM40
5962-9861202QXA	<u>3/</u>	SMJ320F240HFPW40

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE  
number

01295

Vendor name  
and address

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

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