REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. - gap	07-02-12	Joseph D. Rodenbeck
B	Update drawing to current MIL-PRF-38535 requirements. Remove class M references. - jt	14-08-04	Charles F. Saffle
C	Update drawing to current MIL-PRF-38535 requirements. - rdc	19-03-27	Charles F. Saffle

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Lee Surowiec

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Larry E. Shaw

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
98-03-31

REVISION LEVEL
C

MICROCIRCUIT, DIGITAL, BIPOLAR, BCD-TO-SEVEN-SEGMENT DECODER/DRIVER MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-98564**

SHEET 1 OF 12

DSCC FORM 2233
APR 97

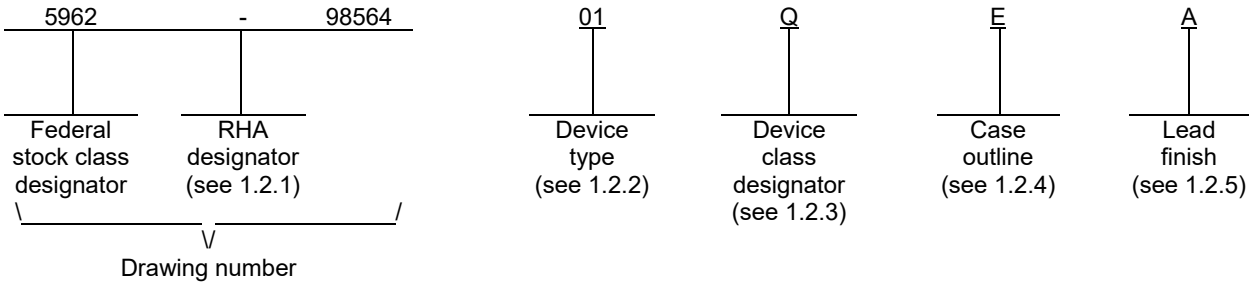
5962-E287-19

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	SN5447A	BCD-to-seven-segment decoder/driver w/ open-collector outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC}) (with respect to ground terminal)	7 V dc
Input voltage	5.5 V dc
Current forced into any output in the off state	1 mA
Case operating temperature range (T_C)	-55°C to +125°C
Maximum power dissipation (P_D)	595 mW
Thermal resistance, junction to case (θ_{JC})	See MIL-STD 1835
Junction temperature (T_J)	175°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Off-state output voltage ($V_{O(off)}$) (a thru g)	15 V dc
On-state output current ($I_{O(on)}$) (a thru g)	40 mA
High-level output current (I_{OH}) ($\overline{BI}$ / $\overline{RBO}$)	-200 µA
Low-level output current (I_{OL}) ($\overline{BI}$ / $\overline{RBO}$)	8 mA
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. T

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Segment identification, numerical designations and displays. The segment identification, numerical designation and resultant displays shall be as specified on figure 1.

3.2.3 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.4 Function table. The function table shall be as specified on figure 3.

3.2.5 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.6 Voltage waveforms and load circuit. The voltage waveforms and load circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test		Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level input voltage		V_{IH}		1, 2, 3	01	2		V
Low-level input voltage		V_{IL}		1, 2, 3	01		0.8	V
Input clamp voltage		V_{IK}	V_{CC} = 4.5 V, I_I = -12 mA	1, 2, 3	01		-1.5	V
High-level output voltage	$\overline{BI}$ / $\overline{RBO}$	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -200µA	1, 2, 3	01	2.4		V
Low-level output voltage	$\overline{BI}$ / $\overline{RBO}$	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA	1, 2, 3	01		0.4	V
Off-state output current	a thru g	$I_{O(OFF)}$	V_{CC} = 5.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(OFF)}$ = 15 V	1, 2, 3	01		250	µA
On-state output voltage	a thru g	$V_{O(ON)}$	V_{CC} = 4.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(ON)}$ = 40 mA	1, 2, 3	01		0.4	V
Input current at maximum input voltage	Any input except $\overline{BI}$ / $\overline{RBO}$	I_I	V_{CC} = 5.5 V, V_I = 5.5 V	1, 2, 3	01		1	mA
High-level input current	Any input except $\overline{BI}$ / $\overline{RBO}$	I_{IH}	V_{CC} = 5.5 V, V_I = 2.4 V	1, 2, 3	01		40	µA
Low-level input current	Any input except $\overline{BI}$ / $\overline{RBO}$	I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V	1, 2, 3	01		-1.6	mA
	$\overline{BI}$ / $\overline{RBO}$						-4	
Short-circuit output current	$\overline{BI}$ / $\overline{RBO}$	I_{OS}	V_{CC} = 5.5 V	1, 2, 3	01		-4	mA
Supply current	$\overline{BI}$ / $\overline{RBO}$	I_{CC}	V_{CC} = 5.5 V, All inputs at 4.5 V, All outputs open.	1, 2, 3	01		85	mA
Functional tests			See 4.4.1b	7, 8A, 8B	01			
Turn-off time from A input		t_{PLH}	V_{CC} = 5 V, R_L = 120 Ω, C_L = 15 pF T_A = 25°C See Figure 5	9	01		100	ns
Turn-on time from A input		t_{PHL}					100	
Turn-off time from $\overline{RBI}$ input		t_{PLH}					100	
Turn-on time from $\overline{RBI}$ input		t_{PHL}					100	

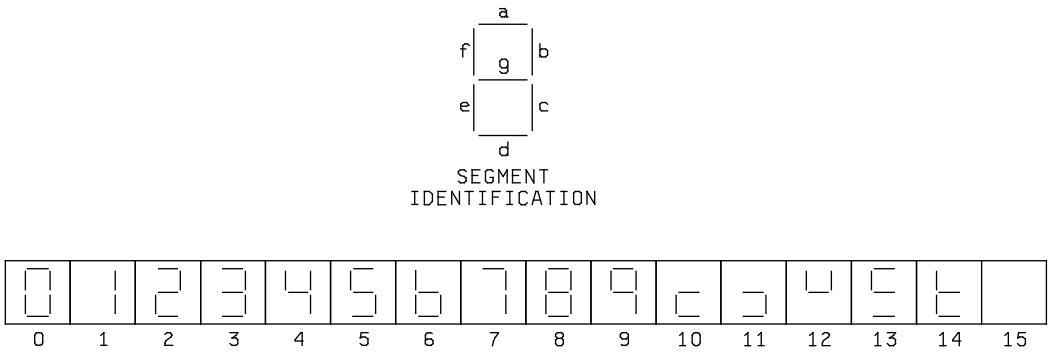


FIGURE 1 Segment identification, numerical designations and displays.

Device type	01
Case outlines	E and F
Terminal number	Terminal symbol
1	B
2	C
3	$\overline{LT}$
4	$\overline{BI}$ / $\overline{RBO}$
5	$\overline{RBI}$
6	D
7	A
8	GND
9	e
10	d
11	c
12	b
13	a
14	g
15	f
16	V_{CC}

FIGURE 2. Terminal connections

Decimal or Function	INPUTS						$\overline{BI}$ / $\overline{RBO}$ *	OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	1
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES:
1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ($\overline{BI}$), all segment outputs are off regardless of the level of any other input.
3. When ripple blanking input ($\overline{RBI}$) and inputs A, B, C and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output ($\overline{RBO}$) goes to a low level (response condition).
4. When the blanking input/ripple blanking output ($\overline{BI}$ / $\overline{RBO}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

* $\overline{BI}$ / $\overline{RBO}$ is wire AND logic serving as blanking input ($\overline{BI}$) and/or ripple blanking output ($\overline{RBO}$).

FIGURE 3. Function table.

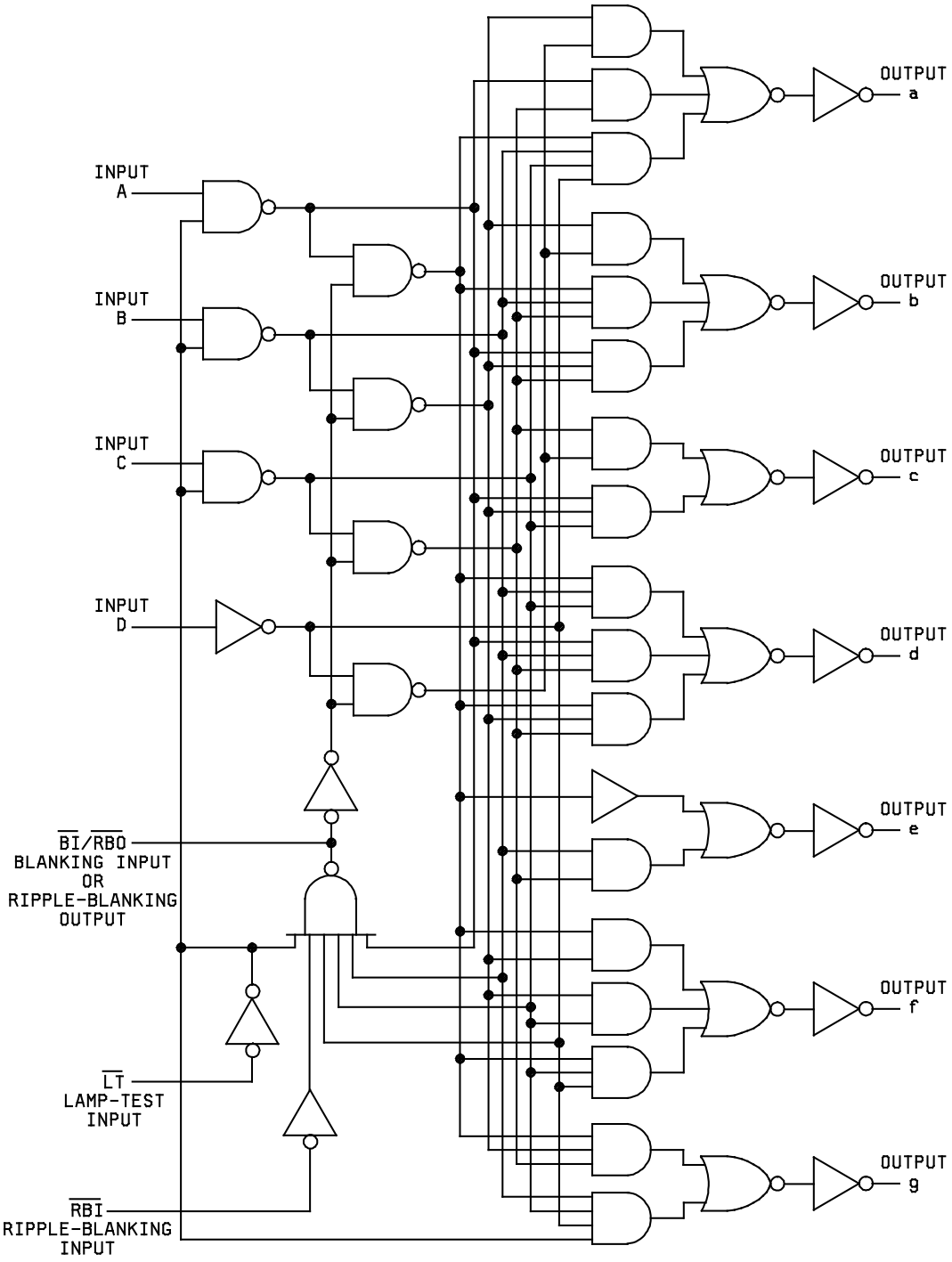
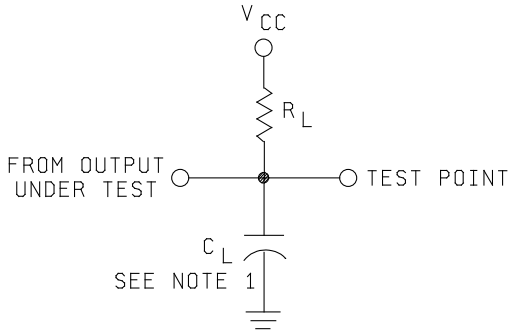
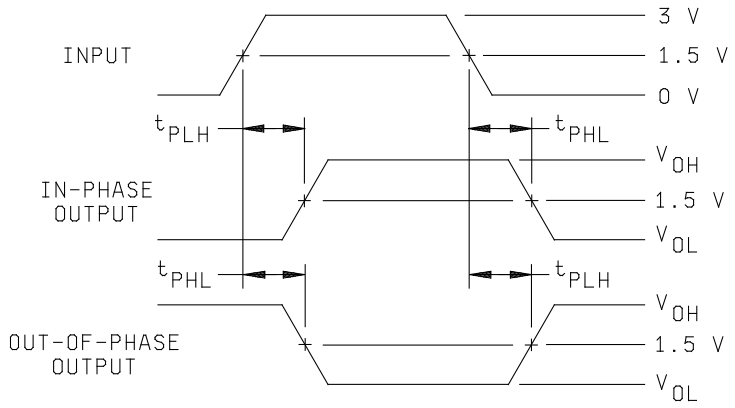


FIGURE 4 Logic diagram



LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

Notes:
1. C_L includes probe and jig capacitance. See Table I.
2. All input pulses are supplied with a generator having the following characteristics:
   PRR ≤ 1MHz, t_r ≤ 7 ns, t_f ≤ 7 ns, Z_{OUT} = 50Ω.

FIGURE 5. Voltage waveforms and load circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7, 8A and 8B shall include verifying the functionality of the device.

c. Subgroups 4, 5, 6, 10 and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8A, 8B, 9	2/ 1, 2, 3, 7, 8A, 8B, 9
Group A test requirements (see 4.4)	1, 2, 3, 7, 8A, 8B, 9	1, 2, 3, 7, 8A, 8B, 9
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	- - -	- - -

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-03-27

Approved sources of supply for SMD 5962-98564 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9856401QEA	01295	SNJ5447AJ
5962-9856401QFA	01295	SNJ5447AW

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.