

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. - drw	06-03-09	Raymond Monnin

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A												
SHEET	15	16	17	18	19	20	21	22												
REV STATUS OF SHEETS	REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Rajesh Pithadia	<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Rajesh Pithadia																		
	APPROVED BY Raymond Monnin	<p align="center">MICROCIRCUIT, DIGITAL-LINEAR, CMOS, LOW-VOLTAGE 10-BIT ANALOG TO DIGITAL CONVERTER WITH SERIAL CONTROL AND 8 ANALOG INPUTS, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 98-06-24																		
	REVISION LEVEL A	<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-98538</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-98538														
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		SHEET 1 OF 22																	

1.3 Absolute maximum ratings. 1/, 2/

Supply voltage range (V_{CC})	-0.5 V dc to +6.5 V dc 2/
Input voltage range (V_I) (any input)	-0.3 V to $V_{CC}+0.3$ V
Output voltage (V_O)	-0.3 V to $V_{CC}+0.3$ V
Positive reference voltage, V_{REF+}	$V_{CC}+0.1$ V
Negative reference voltage, V_{REF-}	-0.1 V
Peak input current I_I (any input)	± 20 mA
Peak total input current (all inputs)	-30 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds	+260°C
Maximum power dissipation, $T_A \leq 25^\circ\text{C}$: 3/	
Case R	1894 mW
Case 2	1375 mW
Thermal resistance, junction-to-case (θ_{JC}):	
Case R	28°C/W
Case 2	20°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case R	66°C/W
Case 2	65°C/W
Junction temperature (T_J)	150 °C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+2.7 V dc to +5.5 V dc
Positive reference Voltage, (V_{REF+})	V_{CC} 4/
Negative reference Voltage, (V_{REF-})	0 V 4/
Differential reference Voltage, $V_{REF+} - V_{REF-}$	+2.5 V dc to $V_{CC} + 0.2$ V dc 4/
Analog input voltage range (V_I)	0 to V_{CC} 4/
High level input voltage, (V_{IH})	2.1 V dc
Low level input voltage, (V_{IL})	0.6 V dc
Setup time, input data bits valid before I/O CLK $\uparrow\downarrow$, t_{su} (A)	100 ns
Hold time, input data bits valid after I/O CLK $\uparrow\downarrow$, t_h (A)	5 ns
Setup time, \overline{CS} \downarrow to I/O CLK \uparrow , t_{su} (CS)	5 ns
Hold time, I/O CLK \downarrow to \overline{CS} \downarrow , t_h (CS)	65 ns
Pulse duration, FS high, t_{WH} (FS)	1 I/O CLK periods

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ All voltage values are with respect to GND with REF- and GND wired together. (unless otherwise noted).
- 3/ Derate factor at $T_A > 25^\circ\text{C}$ for case R is 15.1 mW/°C, and for case 2 is 11.0 mW/°C.
- 4/ Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltage less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

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1.4 Recommended operating conditions - Continued.

Pulse duration, \overline{CSTART} , t_w (CSTART).....	0.84 μ s
Setup time, $\overline{CS} \uparrow$ to $\overline{CSTART} \downarrow$, t_{su} (CSTART).....	10 ns
Clock frequency at I/O CLK, f_{CLK} ; $V_{CC} = 5.5$ V.....	0.1 to 10 MHz
$V_{CC} = 2.7$ V.....	0.1 to 2.81 MHz
Pulse duration, I/O CLK high, t_{WH} (I/O); $V_{CC} = 5.5$ V.....	50 ns
$V_{CC} = 2.7$ V.....	100 ns
Pulse duration, I/O CLK low, t_{WL} (I/O); $V_{CC} = 5.5$ V.....	50 ns
$V_{CC} = 2.7$ V.....	100 ns
Transition time, I/O CLK t_t (I/O).....	1 μ s <u>5/</u>
Transition time, DATA IN, t_t (DATA IN).....	10 μ s
Transition time, \overline{CS} , t_t (CS).....	10 μ s
Transition time, FS, t_t (FS).....	10 μ s
Transition time, \overline{CSTART} , t_t (CSTART).....	10 μ s
Operating ambient temperature range (T_A).....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

5/ This is the time required for the I/O CLK signal to fall from V_{IH} max to V_{IL} min or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with an input clock transition time as slow as 1 μ s for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block or logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	I _{OH} = -0.2 mA, V _{CC} = 5.5 V	1, 2, 3	01	2.4		V
		I _{OH} = -20 μA, V _{CC} = 2.7 V			V _{CC} - 0.1		
Low level output voltage	V _{OL}	I _{OL} = 0.8 mA, V _{CC} = 5.5 V	1, 2, 3	01		0.4	V
		I _{OL} = 20 μA, V _{CC} = 2.7 V				0.1	
High impedance output current	I _{OZ}	V _{OUT} = V _{CC} , \overline{CS} = V _{CC}	1, 2, 3	01		2.5	μA
		V _{OUT} = 0 V, \overline{CS} = V _{CC}				-2.5	
High level input current	I _{IH}	V _{IN} = V _{CC}	1, 2, 3	01		2.5	μA
Low level input current	I _{IL}	V _{IN} = 0 V	1, 2, 3	01		2.5	μA
Operating supply current	I _{CC}	I/O CLK = GND, V _{CC} = 3.3 V to 5.5 V, Conversion speed = fast, For all digital inputs, 0 ≤ V _{IN} ≤ 0.3 V or V _{IN} ≥ V _{CC} - 0.3 V	1, 2, 3	01		1.5	mA
		I/O CLK = GND, V _{CC} = 3.3 V to 5.5 V, Conversion speed = slow, For all digital inputs, 0 ≤ V _{IN} ≤ 0.3 V or V _{IN} ≥ V _{CC} - 0.3 V				1.0	
		I/O CLK = GND, V _{CC} = 2.7 V to 3.3 V, Conversion speed = slow, For all digital inputs, 0 ≤ V _{IN} ≤ 0.3 V or V _{IN} ≥ V _{CC} - 0.3 V				0.75	
Power down supply current	I _{CC(PD)}	For all digital inputs, 0 ≤ V _{IN} ≤ 0.3 V or V _{IN} ≥ V _{CC} - 0.3 V	1, 2, 3	01		25	μA
Selected channel leakage current	I _{lkg}	Selected channel at V _{CC} , Unselected channel at 0 V	1, 2, 3	01		1.0	μA
		Selected channel at 0 V, Unselected channel at V _{CC}				-1.0	
Maximum static analog reference current into REF+	----	V _{ref+} = V _{CC} = 5.5V, V _{ref-} = GND	1, 2, 3	01		1	μA
Input capacitance, analog inputs	C _{IN}	<u>2/</u>	1, 2, 3	01		55	pF
Input capacitance, control inputs	C _{IN}	<u>2/</u>	1, 2, 3	01		15	pF
Input multiplexer resistance	Z _{IN}	V _{CC} = 4.5 V <u>2/</u>	1, 2, 3	01		1	kΩ
		V _{CC} = 2.7 V <u>2/</u>				5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Linearity Error	E _L	<u>3/</u>	1, 2, 3	01		±1	LSB
Differential linearity error	E _D	<u>4/</u>	1, 2, 3	01		±1	LSB
Offset error	E _O	<u>4/ 5/</u>	1, 2, 3	01		±1.5	LSB
Gain error	E _G	<u>4/ 5/</u>	1, 2, 3	01		±1	LSB
Total unadjusted error	E _T	<u>6/</u>	1, 2, 3	01		±1.75	LSB
Functional tests		See 4.4.1C	7, 8A, 8B	01	L	H	
Conversion time	t _{CONV}	Fast conversion speed See figure 4	9, 10, 11	01		10	μs
		Slow conversion speed See figure 4				25	
Total cycle time (access, sample, conversion and EOC↑ to \overline{CS} ↓ delay)	t _C	Fast conversion speed See figure 4 <u>7/ 8/ 9/</u>	9, 10, 11	01		10.1 + 10 I/O CLK	μs
		Slow conversion speed See figure 4 <u>7/ 9/</u>				40.1 +10 I/O CLK	
Channel acquisition time (sample)	t _{acq}	See figure 4 <u>7/</u>	9, 10, 11	01		6	I/O CLK periods
Valid time, DATA OUT remains valid after I/O CLK↓	t _V	See figure 4	9, 10, 11	01	50		ns
Delay time, I/O CLK high to FS high	t _{d1(FS)}	See figure 4	9, 10, 11	01	5	50	ns
Delay time, I/O CLK high to FS low	t _{d2(FS)}	See figure 4	9, 10, 11	01	10	60	ns
Delay time, EOC↑ to \overline{CS} low	t _{d(EOC↑ - CS↓)}	See figure 4 <u>10/</u>	9, 10, 11	01	100		ns
Delay time \overline{CS} ↓ to FS↑	t _{d(CS↓ - FS↑)}	See figure 4	9, 10, 11	01	1	7	I/O CLK periods
Delay time, 10th I/O CLK low to \overline{CS} low to abort conversion.	t _{d(I/O - CS)}	See figure 4 <u>11/</u>	9, 10, 11	01		1.1	μs

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, I/O CLK low to DATA OUT valid	t _d (I/O - DATA)	See figure 4	9, 10, 11	01		50	ns
Delay time, 10th I/O CLK ↓ to EOC low	t _d (I/O - EOC)	See figure 4	9, 10, 11	01		240	ns
Enable time, \overline{CS} low to DATA OUT valid (MSB driven)	t _{PZH} , t _{PZL}	See figure 4	9, 10, 11	01		1.3	μs
Disable time, \overline{CS} high to DATA OUT invalid (high impedance)	t _{PHZ} , t _{PLZ}	See figure 4	9, 10, 11	01		150	ns
Fall time, EOC	t _f (EOC)	See figure 4	9, 10, 11	01		50	ns
Rise time, output data bus at 2.2 MHz I/O CLK	t _r (bus)	See figure 4	9, 10, 11	01		250	ns
Fall time, output data bus at 2.2 MHz I/O CLK	t _f (bus)	See figure 4	9, 10, 11	01		250	ns

1/ VCC = V_{ref+} = 2.7 V to 5.5 V, I/O frequency = 2.2 MHz.

2/ Tested initially and after any design or process changes which affect this parameter.

3/ Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.

4/ Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltage less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (V_{ref+} - V_{ref-}); however, the electrical specifications are no longer applicable.

5/ Zero error is the difference between 0000000000 and the converted output for zero input voltage. Full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.

6/ Total unadjusted error comprises linearity, zero-scale and full-scale errors.

7/ I/O CLK period = 1/ (I/O CLK frequency).

8/ For 3.3 V to 5.5 V only.

9/ For microprocessor mode.

10/ For all operating modes.

11/ Any transactions of \overline{CS} are recognized as valid only when the level is maintained for a setup time after the transition.

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Device type	01
Case outlines	R and 2
Terminal number	Terminal symbol
1	A0
2	A1
3	A2
4	A3
5	A4
6	A5
7	A6
8	A7
9	$\overline{\text{CSTART}}$
10	GND
11	$\overline{\text{INV CLK}}$
12	FS
13	REF-
14	REF+
15	$\overline{\text{CS}}$
16	DATA OUT
17	DATA IN
18	I/O CLK
19	EOC
20	V _{CC}

Pin description	
Terminal	Description
An (n = 0 to 7)	Analog signal inputs
$\overline{\text{CSTART}}$	Sampling/conversion start control
$\overline{\text{INV CLK}}$	Inverted clock input
FS	DSP frame synchronization input
REF-	Lower reference voltage
REF+	Upper reference voltage
$\overline{\text{CS}}$	Chip select
DATA OUT	Serial data output
DATA IN	Serial data input
I/O CLK	Input-output clock
EOC	End of conversion

FIGURE 1. Terminal connections.

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Condition Clock		I/O CLK Active Edge	
$\overline{\text{INV CLK}}$	FS at $\overline{\text{CS}} \downarrow$	Output data changes on	Input data sampled on
High	High (MP mode)	↓	↑
High	Low (DSP mode)	↑	↓
Low	High (MP mode)	↓	↓
Low	Low (DSP mode)	↑	↑

FIGURE 2. Truth table.

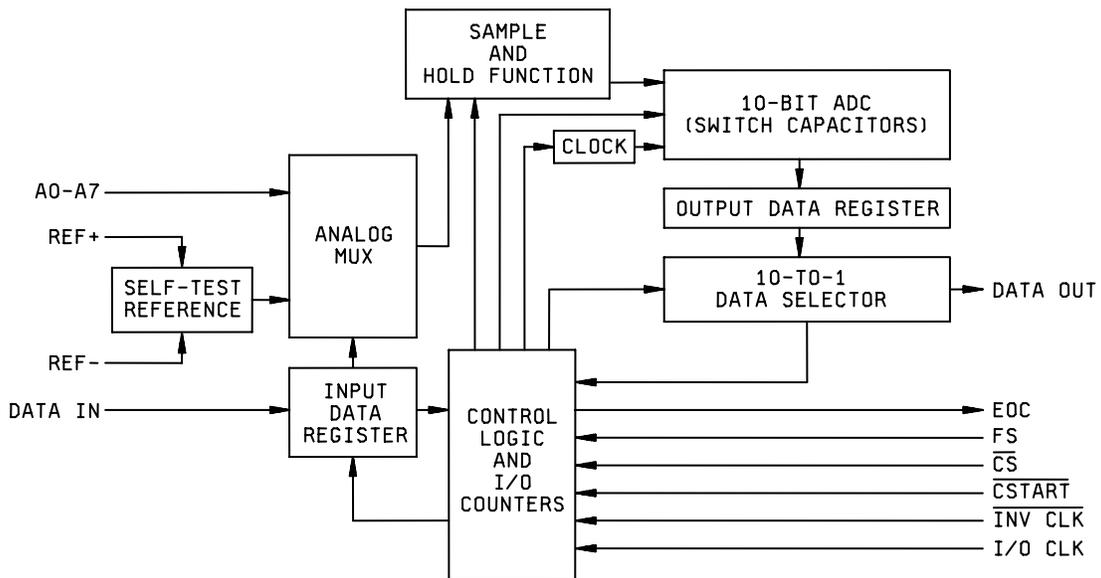
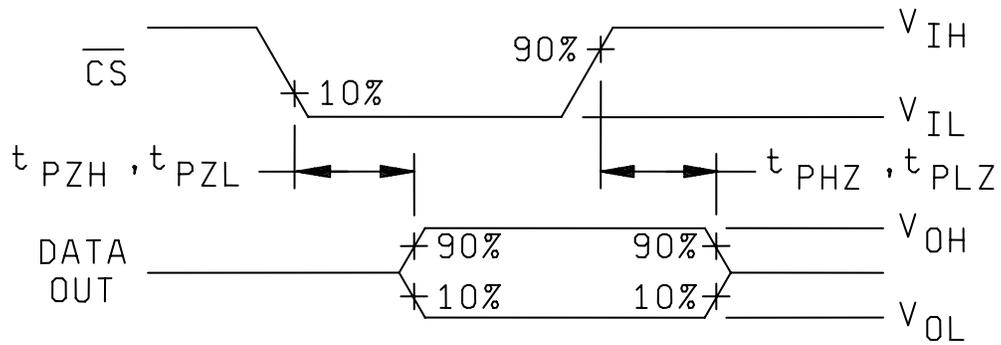


FIGURE 3. Block diagram.

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DATA OUT to HI-Z voltage



\overline{CS} and I/O CLK voltage

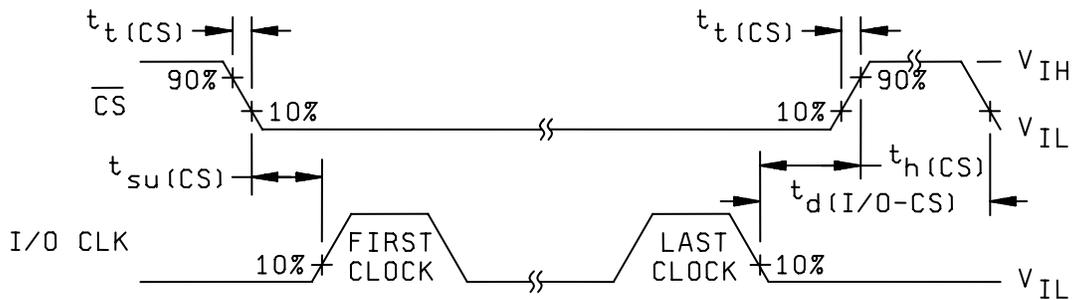
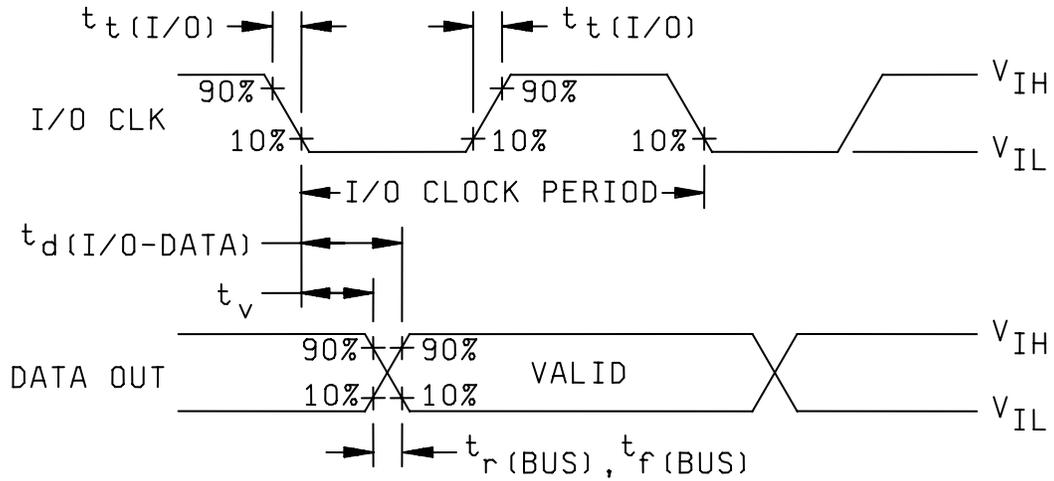


FIGURE 4. Switching waveforms and test circuit.

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DATA OUT and I/O CLK voltage



\overline{CS} low to FS low

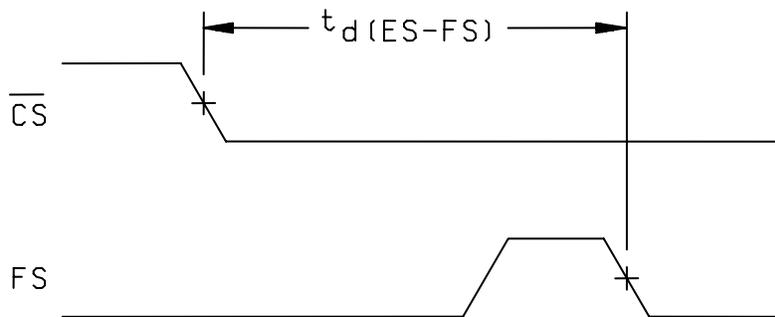
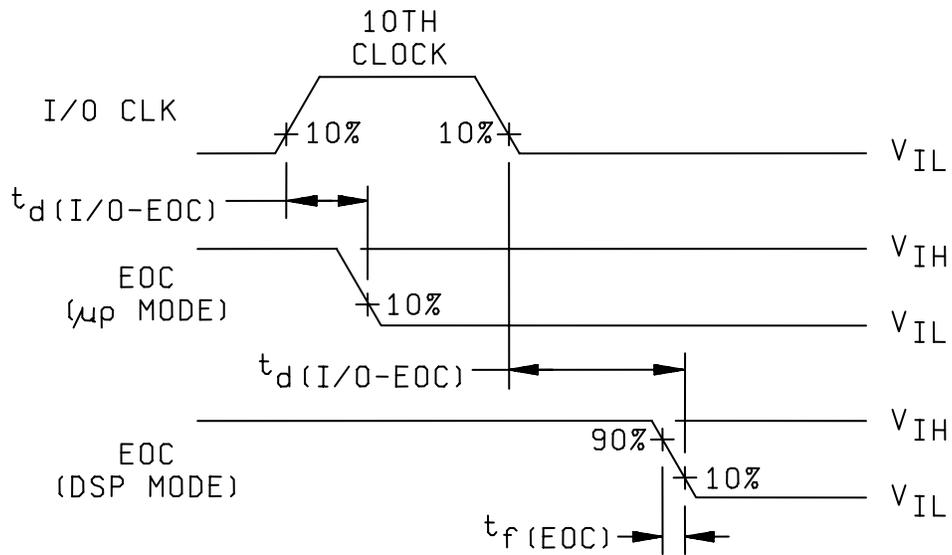


FIGURE 4. Switching waveforms and test circuit - continued.

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I/O CLK and EOC voltage



FS and I/O CLK voltage

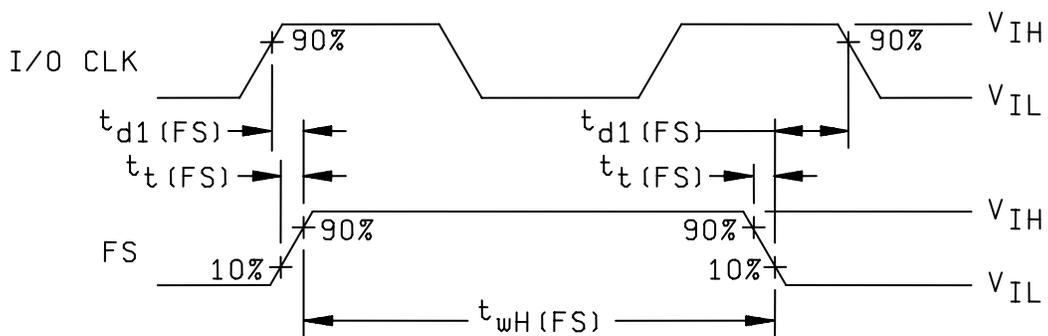


FIGURE 4. Switching waveforms and test circuit - continued.

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$\overline{\text{CSTART}}$ and $\overline{\text{CS}}$

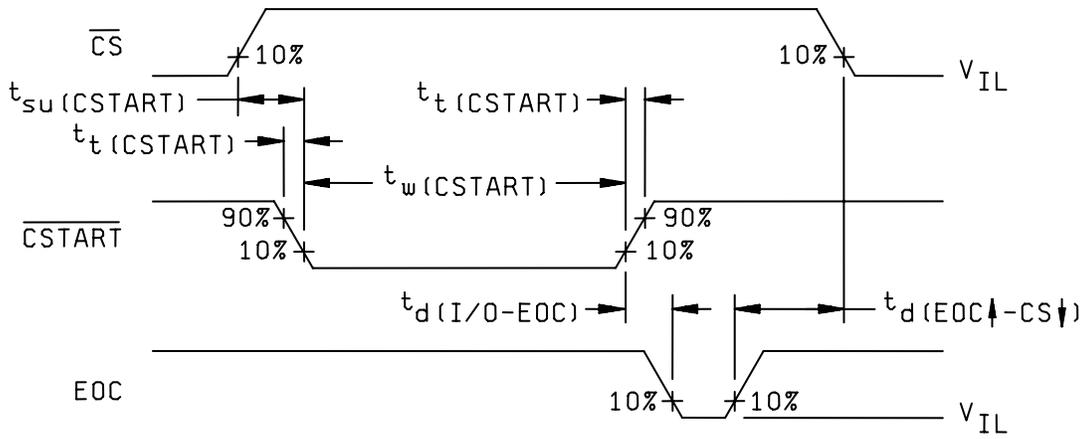
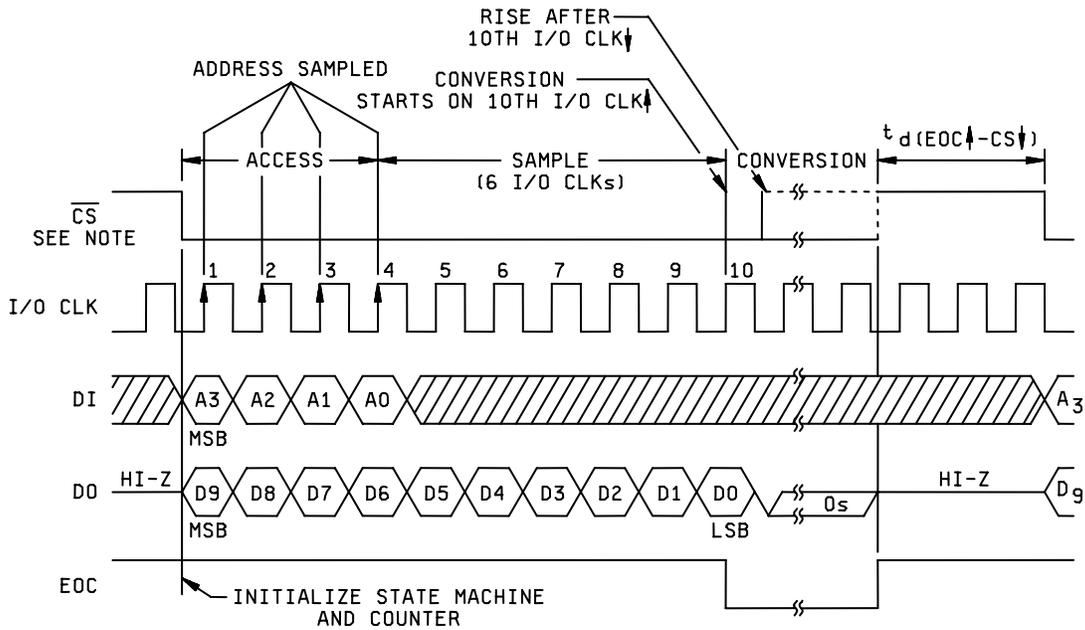


FIGURE 4. Switching waveforms and test circuit - continued.

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Microprocessor interface timing (normal sample mode, $\overline{\text{INV CLK}} = \text{High}$)

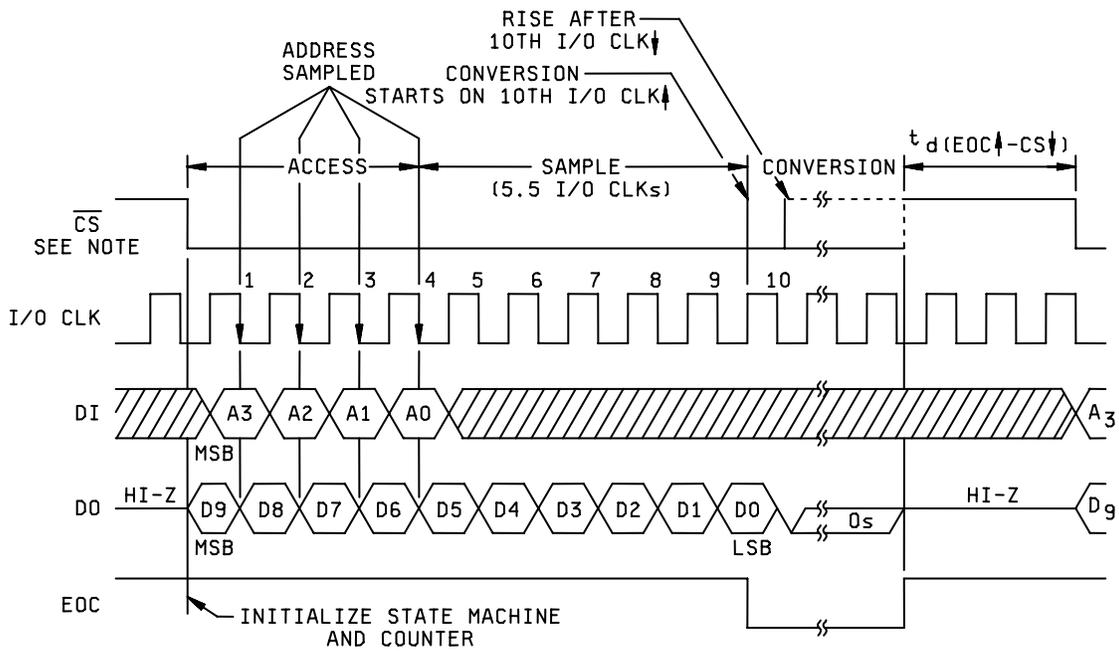


NOTE: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

FIGURE 4. Switching waveforms and test circuit - continued.

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Microprocessor interface timing (normal sample mode, $\overline{\text{INV CLK}} = \text{Low}$)

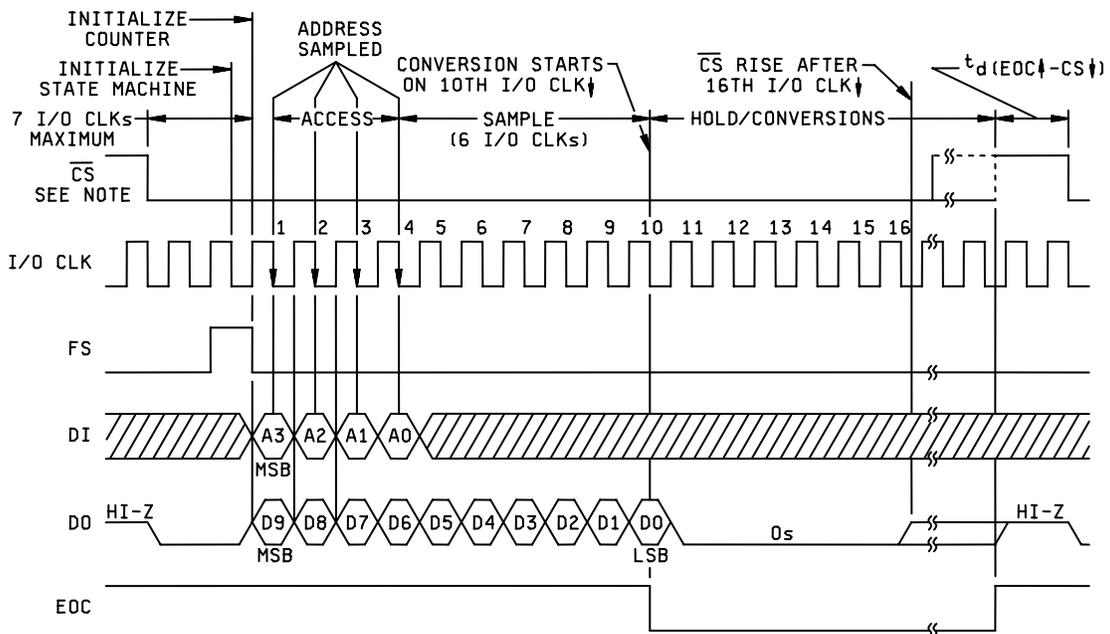


NOTE: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

FIGURE 4. Switching waveforms and test circuit - continued.

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DSP interface timing (16-clock transfer, normal sample mode, $\overline{\text{INV CLK}} = \text{High}$)

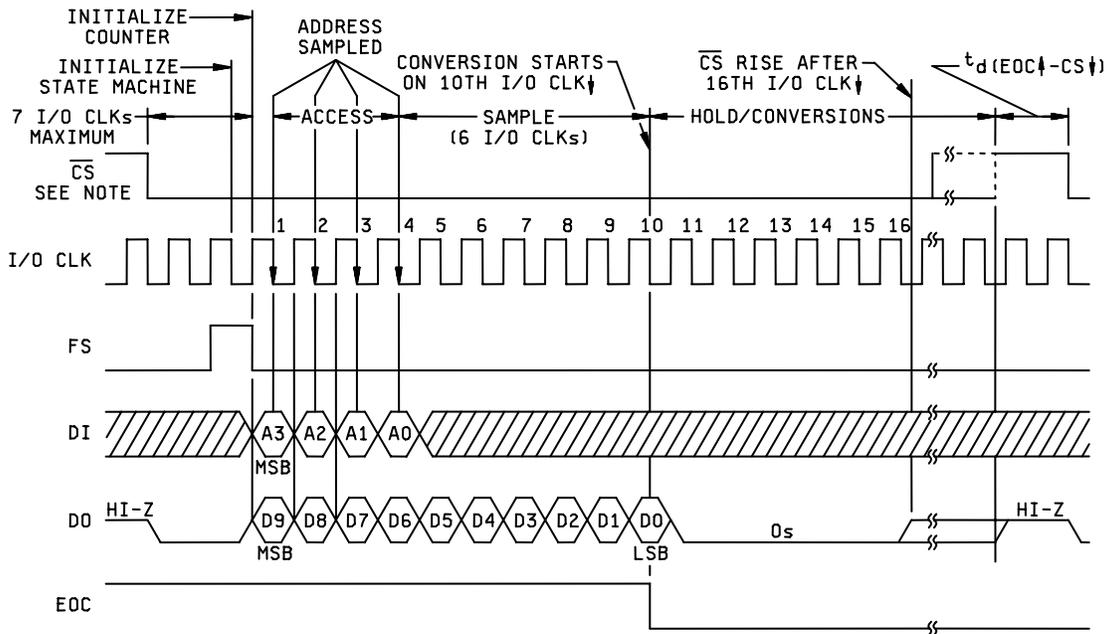


NOTE: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

FIGURE 4. Switching waveforms and test circuit - continued.

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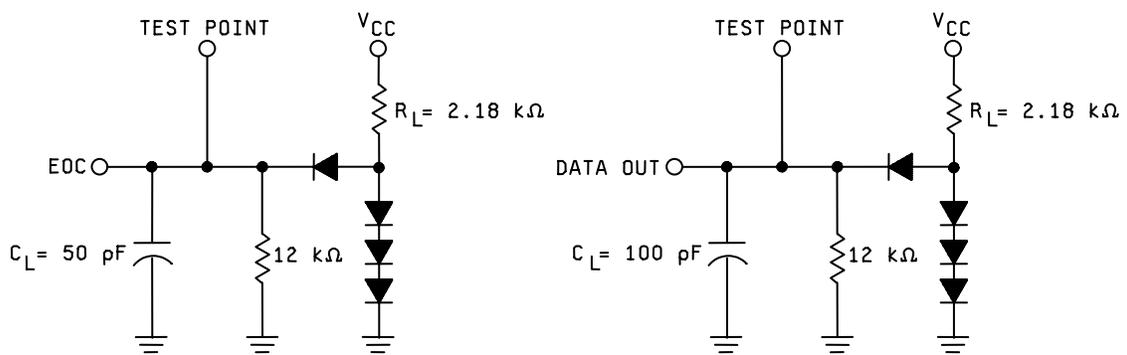
DSP interface timing (16-clock transfer, normal sample mode, $\overline{\text{INV CLK}} = \text{Low}$)



NOTE: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

FIGURE 4. Switching waveforms and test circuit - continued.

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NOTE: C_L includes probe and jig capacitance.

FIGURE 4. Switching waveforms and test circuit - continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8A, 8B, 9, 10, 11	<u>1/</u> 1, 2, 3, 7, 8A, 8B, 9, 10, 11	<u>2/</u> 1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

- 1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD- 883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-03-09

Approved sources of supply for SMD 5962-98538 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9853801QRA	01295	TLV1548MJB
5962-9853801Q2A	01295	TLV1548MFKB

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
PO Box 660199
Dallas, TX 75243

Point of contact:
U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

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