

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct terminal connections table in Figure 1. - CFS	00-05-19	Monica L. Poelking
B	Add JESD 7-A in section 2.2 and correct to JESD 7-A in 4.4.1 herein. Update the boilerplate to current requirements as specified in MIL-PRF-38535. - jak	07-10-22	Thomas M. Hess
C	Update the boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. Update source of supply information. - jwc	14-07-23	Thomas M. Hess
D	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. Delete class M requirement throughout. - TTM	21-02-22	Muhammad A. Akbar



REV																				
SHEET																				
REV	D	D	D	D	D	D														
SHEET	15	16	17	18	19	20														

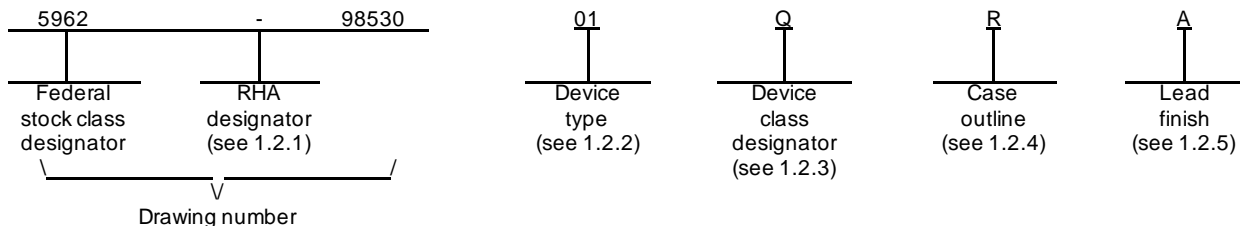
REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	PREPARED BY Joseph A. Kerby	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime</p>		
	CHECKED BY Charles F. Saffle, Jr.			
	APPROVED BY Monica L. Poelking	MICROCIRCUIT, DIGITAL, ADVANCED HIGH SPEED CMOS, OCTAL D-TYPE FLIP-FLOP WITH CLEAR, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 98-05-19			
REVISION LEVEL D	SIZE A	CAGE CODE 67268	5962-98530	
SHEET 1 OF 20				

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54AHC273	Octal D-Type Flip-Flop with Clear

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}).....	-0.5 V dc to +7.0 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to $V_{CC} + 0.5$ V dc 4/
DC input clamp current (I_{IK}) ($V_{IN} < 0.0$).....	-20 mA
DC output clamp current (I_{OK}) ($V_{OUT} < 0.0$ or $V_{OUT} > V_{CC}$)	± 20 mA
Continuous output current (I_O) ($V_{OUT} = 0.0$ to V_{CC}).....	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Maximum Power Dissipation $T_A = +25^\circ\text{C}$ (in still air)	500 mW
Thermal resistance, junction-to-case (θ_{JC}).....	See MIL-STD-1835
Storage temperature range (T_{STG}).....	-65°C to $+150^\circ\text{C}$
Junction temperature (T_J)	$+175^\circ\text{C}$
Lead temperature (soldering, 10 seconds)	$+300^\circ\text{C}$

1.4 Recommended operating conditions. 2/ 3/ 5/

Supply voltage range (V_{CC})	+2.0 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH}):	
$V_{CC} = 2.0$ V.....	+1.5 V
$V_{CC} = 3.0$ V.....	+2.1 V
$V_{CC} = 5.5$ V.....	+3.85 V
Maximum low level input voltage (V_{IL}):	
$V_{CC} = 2.0$ V.....	+0.5 V
$V_{CC} = 3.0$ V.....	+0.9 V
$V_{CC} = 5.5$ V.....	+1.65 V
Input voltage range (V_{IN}).....	+0.0 V dc to 5.5 V dc
Output voltage range (V_{OUT}).....	+0.0 V dc to V_{CC}
Maximum high level output current (I_{OH}):	
$V_{CC} = 2.0$ V.....	-50 μA
$V_{CC} = 3.3$ V ± 0.3 V.....	-4 mA
$V_{CC} = 5.0$ V ± 0.5 V.....	-8 mA
Maximum low level output current (I_{OL}):	
$V_{CC} = 2$ V.....	+50 μA
$V_{CC} = 3.3$ V ± 0.3 V.....	+4 mA
$V_{CC} = 5.0$ V ± 0.5 V.....	+8 mA
Maximum input rise or fall rate ($\Delta t/\Delta V$):	
$V_{CC} = 3.3$ V ± 0.3 V.....	100 ns/V
$V_{CC} = 5.0$ V ± 0.5 V.....	20 ns/V
Case operating temperature range (T_C).....	-55°C to $+125^\circ\text{C}$

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to $+125^\circ\text{C}$.
- 4/ The input and output voltage ratings may be exceeded provided that the input and output current ratings are observed.
- 5/ Unused inputs must be held high or low to prevent them from floating.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD7 - Standard for Description of 54/74HCXXXX and 54/74HCTXXXX High-Speed CMOS Devices.

(Copies of these documents are available online at <https://www.jedec.org/>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 4.

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3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +2.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
					Min	Max	
High level output voltage 3006	V _{OH}	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND	2.0 V	1, 2, 3	1.9		V
					2.9		
					4.4		
			3.0 V	1	2.58		
					2, 3	2.48	
				4.5 V	1	3.94	
2, 3	3.8						
Low level output voltage 3007	V _{OL}	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} For all other inputs V _{IN} = V _{CC} or GND	2.0 V	1, 2, 3		0.1	V
						0.1	
						0.1	
			3.0 V	1		0.36	
					2, 3	0.5	
				4.5 V	1	0.36	
2, 3	0.5						
Input current high 3010	I _{IH}	For input under test, V _{IN} = V _{CC} For all other inputs, V _{IN} = V _{CC} or GND	5.5 V	1		+0.1	μA
				2, 3		+1.0	
Input current low 3009	I _{IL}	For input under test, V _{IN} = GND For all other inputs, V _{IN} = V _{CC} or GND	5.5 V	1		-0.1	μA
				2, 3		-1.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +2.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
					Min	Max	
Quiescent supply current 3005	I _{CC}	For all inputs, V _{IN} = V _{CC} or GND I _{OUT} = 0.0 A	5.5 V	1		4.0	μA
				2, 3		40.0	
Input capacitance 3012	C _{IN}	T _C = +25°C V _{IN} = V _{CC} or GND See 4.4.1c	5.0 V	4		10.0	pF
Power dissipation capacitance	C _{PD} <u>4/</u>	C _L = 50 pF minimum f = 1 MHz, T _A = +25°C See 4.4.1c	5.0 V	4		14.0	pF
Low level ground bounce noise	V _{OLP} <u>5/</u>	V _{IH} = V _{CC} , V _{IL} = 0.0 V T _A = +25°C See 4.4.1d See figure 4	5.0 V	4		1200	mV
Low level ground bounce noise	V _{OLV} <u>5/</u>		5.0 V	4		-1000	
High level V _{CC} bounce noise	V _{OHP} <u>5/</u>		5.0 V	4		1000	
High level V _{CC} bounce noise	V _{OHV} <u>5/</u>		5.0 V	4		-1200	
Functional test 3014	<u>6/</u>	V _{IN} = V _{IH} or V _{IL} Verify output V _{OUT} See 4.4.1b	2.0 V	7, 8	L	H	
			3.0 V				
			5.5 V				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ 125°C +2.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified		V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Pulse duration	t _w	C _L = 50 pF, minimum See figure 5	CLR low	3.0 V and 3.6 V	9	5.0		ns
					10,11	6.0		
				4.5 V and 5.5 V	9, 10,11	5.0		
			CLK high or low	3.0 V and 3.6 V	9	5.0		
					10,11	6.5		
				4.5 V and 5.5 V	9, 10,11	5.0		
Set up time	t _s	C _L = 50 pF, minimum See figure 5	Data before CLK↑	3.0 V and 3.6 V	9	5.5		ns
					10,11	6.5		
				4.5 V and 5.5 V	9, 10,11	4.5		
			CLR before CLK↑	3.0 V and 3.6 V	9, 10,11	2.5		
					4.5 V and 5.5 V	9, 10,11	2.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +2.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
					Min	Max	
Hold time, data after CLK↑	t _h	C _L = 50 pF minimum See figure 5	3.0 V and 3.6 V	9	1.5		ns
				10,11	2.0		
			4.5 V and 5.5 V	9	1.5		
				10,11	2.0		
Maximum operating frequency	f _{max}	C _L = 15 pF <u>7/</u>	3.0 V and 3.6 V	9	75		MHz
				10,11	65		
			C _L = 50 pF	9	50		
				10,11	45		
		C _L = 15 pF <u>7/</u>	4.5 V and 5.5 V	9	120		
				10,11	100		
			C _L = 50 pF	9	80		
				10,11	70		
Propagation delay time, CLR to mQ 3003	t _{PHL1}	C _L = 15 pF minimum See figure 5 <u>7/</u>	3.0 V and 3.6 V	9		13.6	ns
				10, 11	1.0	16.0	
			4.5 V and 5.5 V	9		8.5	
				10, 11	1.0	10.0	
		C _L = 50 pF minimum See figure 5	3.0 V and 3.6 V	9		17.1	
				10, 11	1.0	19.5	
			4.5 V and 5.5 V	9		10.5	
				10, 11	1.0	12.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +2.0 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
					Min	Max	
Propagation delay time, CLK to mQ 3003	t _{PLH1}	C _L = 15 pF minimum See figure 5 <u>7/</u>	3.0 V and 3.6 V	9		13.6	ns
				10, 11	1.0	16.0	
			4.5 V and 5.5 V	9		9.0	
		10, 11		1.0	10.5		
		C _L = 50 pF minimum See figure 5	3.0 V and 3.6 V	9		17.1	
				10, 11	1.0	19.5	
4.5 V and 5.5 V	9			11.0			
	10, 11	1.0	12.5				
Propagation delay time, CLK to mQ 3003	t _{PHL2}	C _L = 15 pF minimum See figure 5 <u>7/</u>	3.0 V and 3.6 V	9		13.6	ns
				10, 11	1.0	16.0	
			4.5 V and 5.5 V	9		9.0	
		10, 11		1.0	10.5		
		C _L = 50 pF minimum See figure 5	3.0 V and 3.6 V	9		17.1	
				10, 11	1.0	19.5	
4.5 V and 5.5 V	9			11.0			
	10, 11	1.0	12.5				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

- 1/ For tests not listed in the referenced MIL-STD-883, utilize the general test procedure of 883 under the conditions listed herein.
- 2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} test, where the output terminals shall be open. When performing the I_{CC} test, the current meter shall be placed in the circuit such that all current flows through the meter. The values to be used for V_{IH} and V_{IL} shall be the V_{IH} minimum and V_{IL} maximum values listed in section 1.4 herein.
- 3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.
- 4/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and current consumption (I_S). Where:

$$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$$

$$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC}$$
 f is the frequency of the input signal; and C_L is the external output load capacitance.
- 5/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

 The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHF} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

 The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.
- 6/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances per MIL-STD-883 may be incorporated. For outputs, L = V_{IL} max, H = V_{IH} min, where V_{IL} max and V_{IH} min are listed in section 1.4 herein.
- 7/ On products compliant to MIL-PRF-38535, this parameter is not production tested.

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Device type	01
Case outlines	R, S and 2
Terminal number	Terminal symbol
1	$\overline{\text{CLR}}$
2	1Q
3	1D
4	2D
5	2Q
6	3Q
7	3D
8	4D
9	4Q
10	GND
11	CLK
12	5Q
13	5D
14	6D
15	6Q
16	7Q
17	7D
18	8D
19	8Q
20	V _{cc}

FIGURE 1. Terminal connections

(Each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	mD	mQ
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

X = Irrelevant

L = Low level

H = High level

↑ = Low-to-high transition of the clock

Q₀ = The level of Q before the indicated steady-state input conditions were established

FIGURE 2. Truth table.

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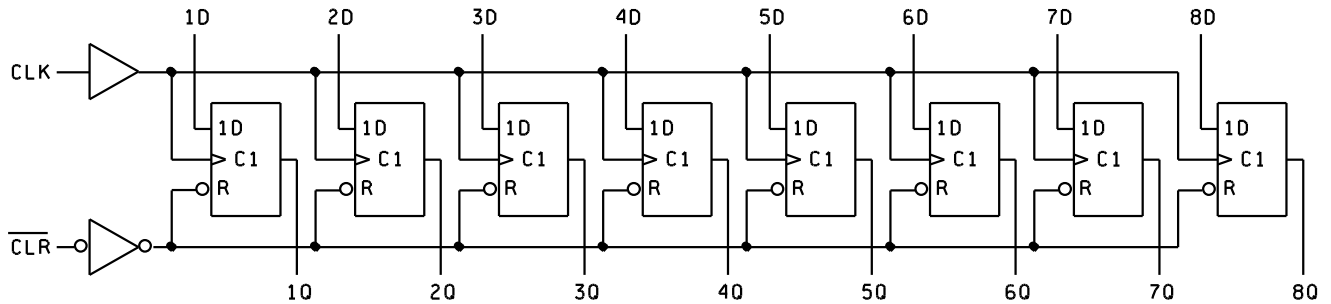
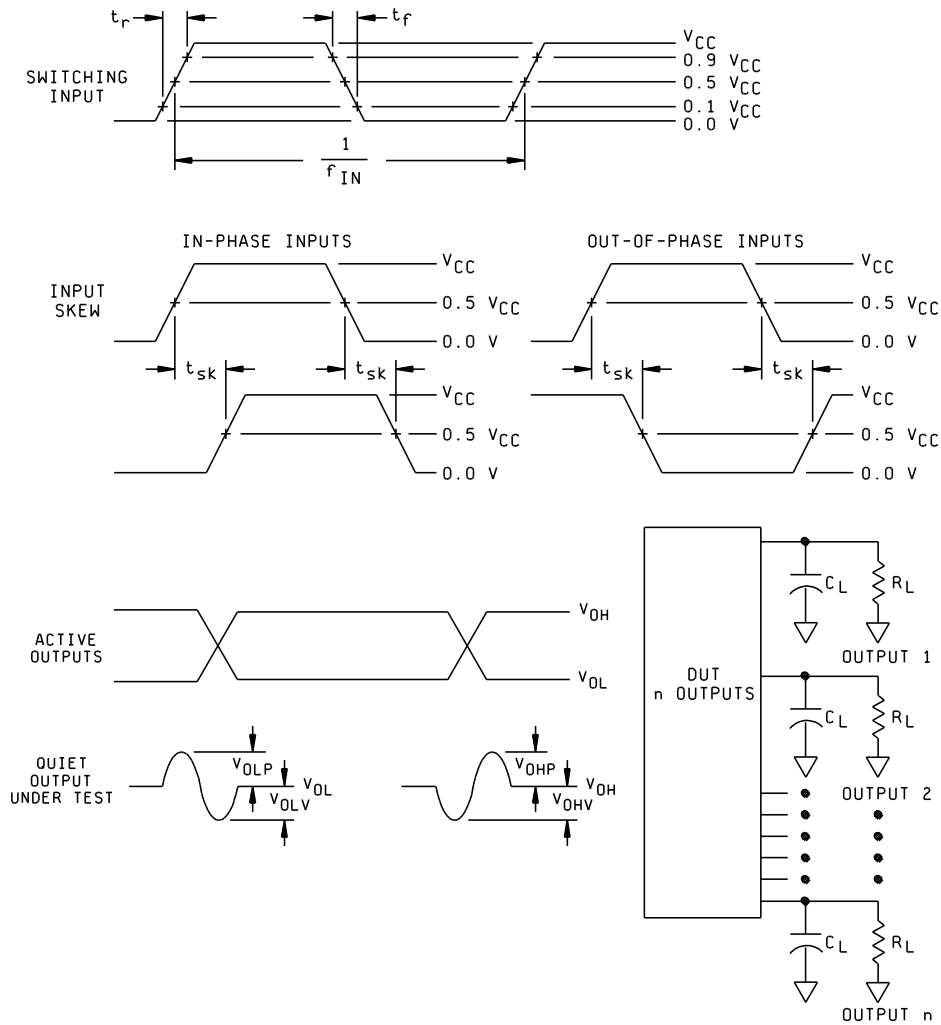


FIGURE 3. Logic diagram.

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NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. $R_L = 5.0 \text{ k}\Omega \pm 1 \text{ percent}$, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
 - a. $V_{IN} = 0.0 \text{ V to } V_{CC}$; duty cycle = 50 percent; $f_{IN} \geq 1 \text{ MHz}$.
 - b. $t_r, t_f = 3.0 \text{ ns} \pm 1.0 \text{ ns}$. For input signal generators incapable of maintaining these values of t_r and t_f , the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the $\pm 1.0 \text{ ns}$ tolerance and guaranteeing the results at $3.0 \text{ ns} \pm 1.0 \text{ ns}$; skew between any two switching inputs signals (t_{sk}): $\leq 250 \text{ ps}$.

FIGURE 4. Ground bounce load circuit and waveforms.

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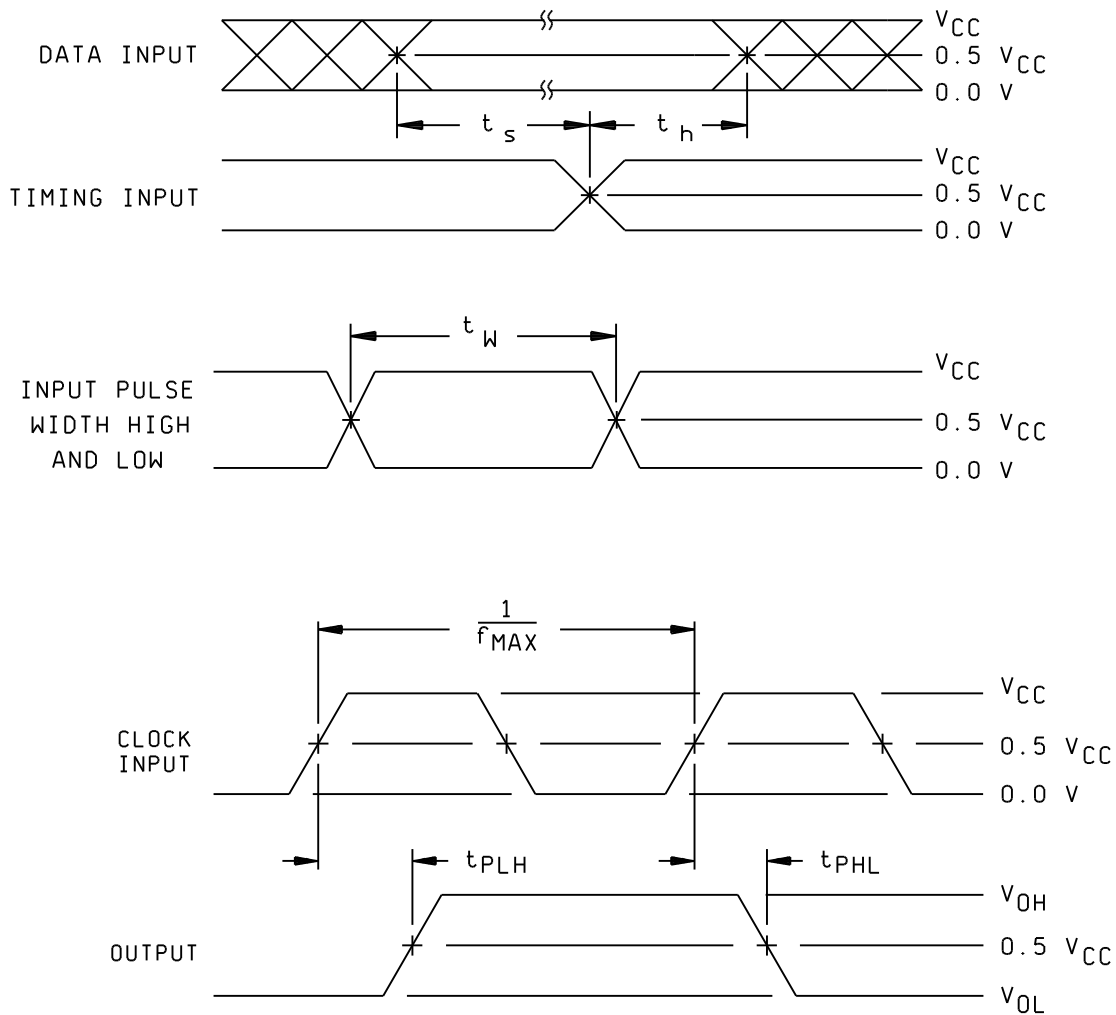


FIGURE 5. Switching waveforms and test circuit.

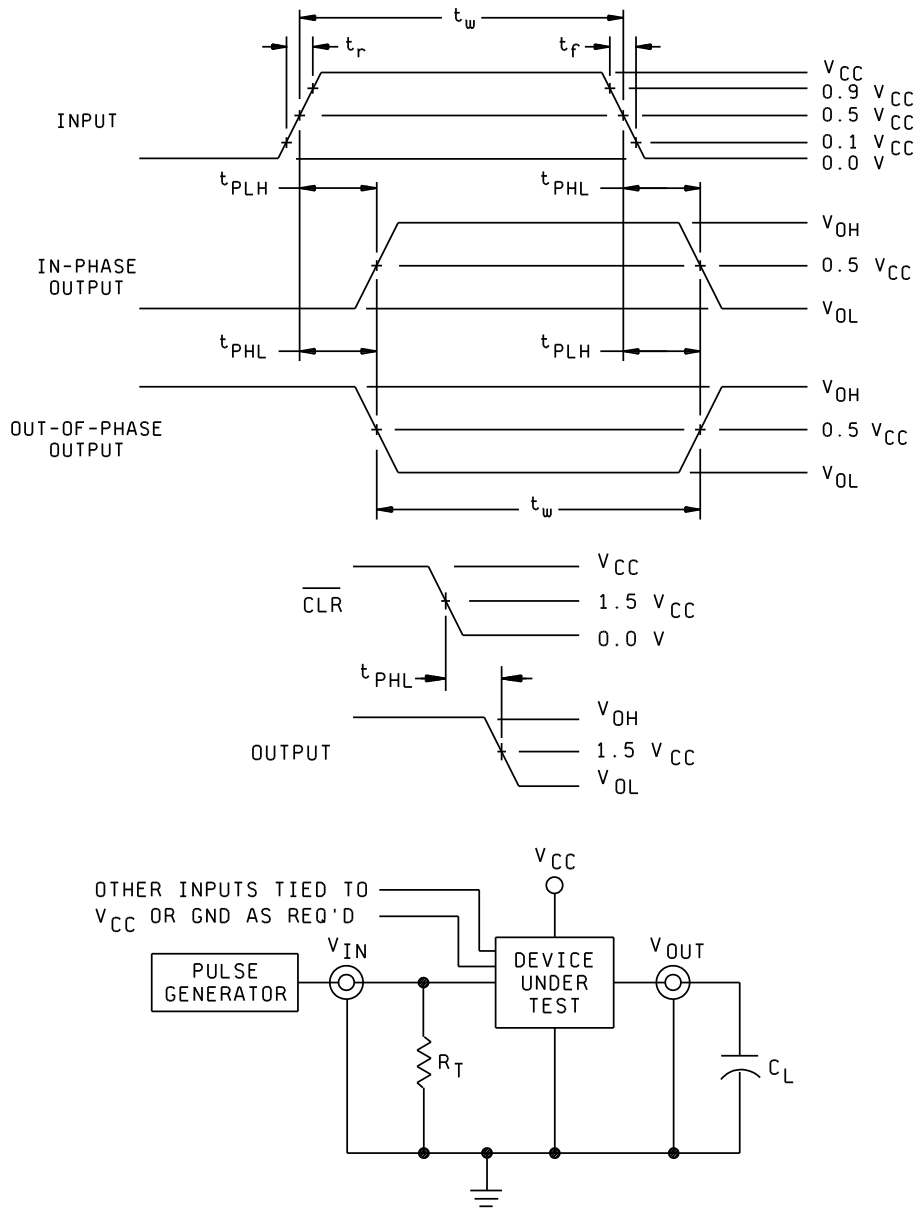
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NOTES:

1. $C_L = 50 \text{ pF}$ (includes test jig and probe capacitance).
2. $R_T = 50\Omega$ or equivalent
3. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to V_{CC} ; $PRR \leq 1 \text{ MHz}$; $t_r = 3.0 \text{ ns}$; $t_f = 3.0 \text{ ns}$; t_r and t_f shall be measured from $0.1 V_{CC}$ to $0.9 V_{CC}$ and from $0.9 V_{CC}$ to $0.1 V_{CC}$, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, method 5012 (see 1.5 herein).
- c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD 7-A and table I herein. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN} and C_{PD} , test all applicable pins on five devices with zero failures.

For C_{IN} , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the C_{IN} tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results for each device tested.

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

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6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 21-02-22

Approved sources of supply for SMD 5962-98530 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9853001QRA	01295	SNJ54AHC273J
5962-9853001QSA	01295	SNJ54AHC273W
5962-9853001Q2A	01295	SNJ54AHC273FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
PO Box 660199
Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.