REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate to include class N. Added case outline X. Editorial changes throughout. – TMH	98-01-27	Monica L. Poelking
B	Changes in accordance with NOR 5962-R043-99.	99-03-04	Monica L. Poelking
C	Added junction temperature to paragraph 1.3. Made technical change to supply current in table I. – LTG	00-01-28	Monica L. Poelking
D	Update boilerplate to MIL-PRF-38535 requirements. – LTG	01-04-13	Thomas M. Hess
E	Change V_{DD}, V_{IN}, V_{OUT}, P_D, Θ_{JC} in section 1.3. Make following changes to table I: Change V_{DD} for I_Z; delete I_{IC} test; change I_{CC} limit; delete V_{DD} for C_{IN}, C_{OUT}, C_X; change t_{d6}, t_{d30}, t_{w6}, t_{d33}, t_w limits; delete footnote 2/. Correct signal names in figures 3 and A-1. Change $\overline{\text{RESET}}$ and TIMER PIN TIMINGS waveforms. Add $\overline{\text{SHZ}}$ TIMING waveform. Add application note to section 6. Editorial changes throughout. – TVN	02-02-26	Thomas M. Hess
F	Update boilerplate to current MIL-PRF-38535 requirements. – CFS	07-12-05	Thomas M. Hess
G	Update boilerplate to current MIL-PRF-38535 requirements. – PHN	13-05-06	Thomas M. Hess
H	Update boilerplate to current MIL-PRF-38535 requirements. – PHN	19-01-23	Thomas M. Hess
J	Update boilerplate to MIL-PRF-38535 requirements. – DRH	24-05-08	Muhammad A. Akbar

REV	J	J																		
SHEET	35	36																		
REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
97-08-04

REVISION LEVEL
J

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-97606**

SHEET 1 OF 36

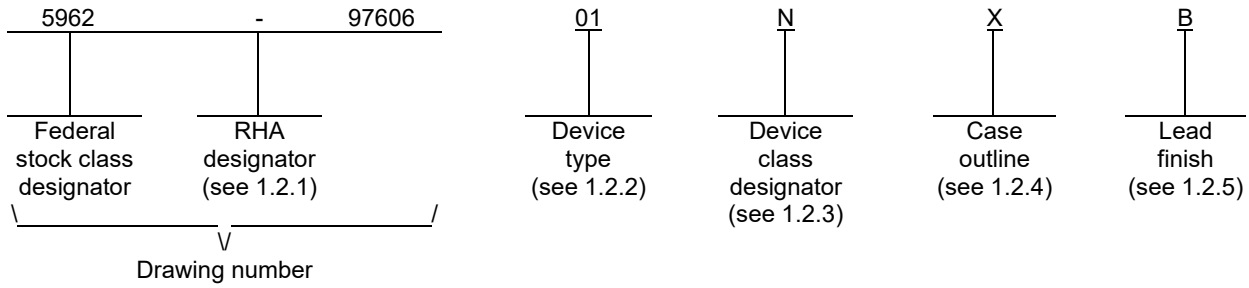
DSCC FORM 2233
APR 97

5962-E348-24

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320LC31	Digital signal processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment (encapsulated in plastic)
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, JEDEC Publication 95, and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Document
X	See figure 1	132	Plastic quad flatpack	JEP 95

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD})	-0.3 V dc to +5.0 V dc
DC input voltage range (V_{IN})	-0.3 V dc to +5.0 V dc
DC output voltage range (V_{OUT})	-0.3 V dc to +5.0 V dc
Continuous power dissipation (P_D) 3/	850 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature (T_J):	
Die code 9	+125°C
Case outline X	+150°C
Thermal resistance, junction to case (θ_{JC}):	
Case outline X	11.0°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+3.13 V dc to +3.47 V dc
Supply voltage range (CVSS, etc.) (V_{SS})	0 V dc nominal
High-level input voltage range (V_{IH}): 4/	
(except $\overline{\text{RESET}}$)	+1.8 V dc to V_{DD} + 0.3 V dc
For $\overline{\text{RESET}}$	+2.2 V dc to V_{DD} + 0.3 V dc
Low-level input voltage range (V_{IL}) 4/	-0.3 V dc to 0.6 V dc
Maximum high-level output current (I_{OH})	-300 µA
Maximum low-level output current (I_{OL})	+2 mA
CLKIN high level input voltage (V_{TH}) 4/	+2.5 V dc to V_{DD} to +0.3 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values are with respect to V_{SS}.
3/ Actual operating power is less. This value was obtained under specially produced worst-case test conditions which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible.
4/ Maximum V_{IH}, minimum V_{IL} and maximum V_{TH} are not production tested.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices.

(Copies of these documents are available online at https://www.jedec.org/.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions for device classes N, Q, and V shall be as specified in MIL-PRF-38535 and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. A certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime - VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	V_{DD}	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_{OH} = -300 µA	3.13 V	1, 2, 3	2.0		V
Low level output voltage	V_{OL}	I_{OL} = 2 mA	3.13 V	1, 2, 3		0.4	
Three-state current	I_Z		3.47 V	1, 2, 3	-20	20	µA
Input current	I_I	For input under test $V_{IN} = V_{SS}$ to V_{DD}	3.13 V to 3.47 V	1, 2, 3	-10	+10	
Input current with internal pull-ups 2/	I_{IP}		3.13 V to 3.47 V	1, 2, 3	-600	+10	
Supply current 3/	I_{CC}	T_A = 25°C, f_x = 40 MHz	3.47 V	1, 2, 3		300	mA
Input capacitance	C_{IN}	T_C = +25°C, See 4.4.1b		4		15	pF
Output capacitance	C_{OUT}			4		20	
X2/CLKIN capacitance	C_X			4		25	
Functional testing		See 4.4.1d		7, 8			
Fall time, CLKIN 4/	t_{f1}	X2/CLKIN timing See figure 4		9, 10, 11		5	ns
Pulse duration, CLKIN low	t_{w1}		t_{C1} = 25 ns		9		
Pulse duration, CLKIN high	t_{w2}		t_{C1} = 25 ns		9		
Rise time, CLKIN 4/	t_{r1}					5	
Cycle time, CLKIN	t_{c1}				25	303	
Fall time, H1/H3	t_{f2}	H1/H3 timing See figure 4				3	
Pulse duration, H1/H3 low	t_{w3}		P = t_{C1}		P-5		
Pulse duration, H1/H3 high	t_{w4}		P = t_{C1}		P-6		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Rise time, H1/H3	t_{r2}	H1/H3 timing See figure 4	9, 10, 11		3	ns
Delay time, from H1(H3) low to H3(H1) high 5/	t_{d1}			0	4	
Cycle time, H1/H3	t_{c2}			50	606	
Delay time, from H1 low to $\overline{\text{STRB}}$ low 5/	t_{d2}	Memory ($\overline{\text{STRB}}$ = 0) See figure 4	9, 10, 11	0	6	ns
Delay time, from H1 low to $\overline{\text{STRB}}$ high 5/	t_{d3}			0	6	
Delay time, from H1 high to R/$\overline{\text{W}}$ low 5/	t_{d4}			0	9	
Delay time, from H1 low to A valid 5/	t_{d6}			0	10	
Setup time, D valid before H1 low (read)	t_{su1}			14		
Hold time, D after H1 low (read) 5/	t_{h1}			0		
Setup time, $\overline{\text{RDY}}$ before H1 high	t_{su3}			8		
Hold time, $\overline{\text{RDY}}$ after H1 high	t_{h2}			0		
Delay time, H1 high to R/$\overline{\text{W}}$ high (write)	t_{d8}				9	
Valid time, D after H1 low (write)	t_{v1}				17	
Hold time, D after H1 high (write)	t_{h3}			0		
Delay time, form H1 high to A valid on back-to-back write cycles	t_{d9}				15	
Delay time, from $\overline{\text{RDY}}$ to A valid 4/	t_{d11}				7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Delay time, H3 high to XF0 low	t_{d17}	Timing for XF0 and XF1 when executing LDFI or LDII See figure 4	9, 10, 11		13	ns
Set-up time, XF1 valid after H1 low	t_{su7}			10		
Hold time, XF1 after H1 low	t_{h7}			0		
Delay time, from H3 high to XF0 high	t_{d18}	Timing for XF0 when executing a STFI or STII See figure 4	9, 10, 11		13	ns
Delay time, from H3 high to XF0 low	t_{d19}	Timing for XF0 and XF1 when executing a SIGI See figure 4	9, 10, 11		13	ns
Delay time, from H3 high to XF0 high	t_{d20}				13	
Set-up time, XF1 valid before H1 low	t_{su8}			10		
Hold time, XF1 after H1 low	t_{h8}			0		
Valid time, H3 high to XF	t_{v3}	Timing for loading XF register when conformed as an output pin See figure 4	9, 10, 11		13	ns
Hold time, XF after H3 high 4/	t_{h9}	Change of XF from output to input mode See figure 4	9, 10, 11		13	ns
Setup time, XF before H1 low	t_{su9}			10		
Hold time, XF after H1 low	t_{h10}			0		
Delay time, from H3 high to XF switching from input to output	t_{d21}	Change of XF from input to output mode See figure 4	9, 10, 11		17	ns
Setup time, for $\overline{\text{RESET}}$ before CLKIN low 4/	t_{su10}	$\overline{\text{RESET}}$ timing See figure 4	9, 10, 11	10	P	ns
Delay time, from CLKIN high to H1 high	t_{d22}			2	14	
Delay time, from CLKIN high to H1 low	t_{d23}			2	14	
Setup time, $\overline{\text{RESET}}$ high before H1 low and after 10 H1 clock cycles	t_{su11}			9		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Delay time, from CLKIN high to H3 low	t_{d24}	$\overline{RESET}$ timing See figure 4		9, 10, 11	2	14	ns
Delay time, from CLKIN high to H3 high	t_{d25}				2	14	
Disable time, from H1 high to D high - Z 4/	t_{dis1}					13	
Disable time, from H3 high to A high - Z 4/	t_{dis2}					9	
Delay time, from H3 high to control signals high 4/	t_{d26}					9	
Delay time, from H1 high to R/$\overline{W}$ high 4/	t_{d27A}					9	
Delay time, from H1 high to $\overline{IACK}$ high 4/	t_{d27B}					9	
Disable time, from $\overline{RESET}$ low to asynchronously reset signals (high - Z) 4/	t_{dis3}					21	
Setup time, $\overline{INT(3-0)}$ before H1 low	t_{su12}	$\overline{INT(3-0)}$ response timing See figure 4		9, 10, 11	15		ns
Pulse duration, to guarantee one interrupt seen 4/ 5/ 6/	t_{w5}				P	2P	
Delay time, from H1 high to $\overline{IACK}$ low	t_{d28}	$\overline{IACK}$ timing See figure 4		9, 10, 11		9	ns
Delay time, from H1 high to $\overline{IACK}$ high during first cycle of $\overline{IACK}$ instruction data read	t_{d29}					9	
Delay time, from H1 high to internal CLKX/R	t_{d30}	Data rate mode See figure 4		9, 10, 11		13	ns
Cycle time, CLKX/R	t_{c3}		CLKX/R ext 5/		t_{c2} x 2.6		
			CLKX/R int 4/		t_{c2} x 2	t_{c2} x 2^{32}	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Pulse width, CLKX/R	t_{w6}	Data rate mode See figure 4	CLKX/R ext 5/	9, 10, 11	t_{c2}+ 10		ns
			CLKX/R int		$(t_{c3}/2)$-5	$(t_{c3}/2)$+5	
Rise time, CLKX/R 4/	t_{r3}					7	
Fall time, CLKX/R 4/	t_{f3}	Fixed data rate mode See figure 4		9, 10, 11		7	ns
Delay time, from CLKX to DX valid	t_{d31}		CLKX ext			30	
			CLKX int			17	
Setup time, DR before CLKR low	t_{su13}		CLKR ext		9		
			CLKR int		21		
Hold time, DR from CLKR low	t_{h11}		CLKR ext		9		
			CLKR int 5/		0		
Delay time, from CLKX to internal FSX high/low	t_{d32}		CLKX ext			27	
			CLKX int			15	
Setup time, FSR before CLKR low	t_{su14}		CLKR ext		9		
			CLKR int		9		
Hold time, FSX/R from CLKX/R low	t_{h12}		CLKX/R ext		9		
			CLKX/R int 5/		0		
Setup time, external FSX before CLKX	t_{su15}		CLKX ext 4/		$-(t_{c2}- 8)$	$(t_{c3}/2- 10)$	
			CLKX int 4/		$-(t_{c2}-21)$	$t_{c3}/2$	
Delay time, from CLKX to first DX bit, FSX precedes CLKX high 4/	t_{d33}	Variable rate data mode See figure 4	CLKX ext	9, 10, 11		30	ns
			CLKX int			18	
Delay time, from FSX to first DX bit, CLKX precedes FSX 4/	t_{d34}					30	
Delay time, from CLKX high to DX high-Z following last data bit 4/	t_{d35}					17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Setup time, $\overline{HOLD}$ valid before H1 low	t_{su16}	$\overline{HOLD}$ / $\overline{HOLDA}$ timing See figure 4	9, 10, 11	13		ns
$\overline{HOLDA}$ valid after H1 low 5/	t_{v4}		9, 10, 11	0	9	ns
Pulse width, $\overline{HOLD}$ low	t_{w7}			2		H1 cycles
Pulse width, $\overline{HOLDA}$ low 5/	t_{w8}			t_{c2}-5		ns
Delay time, from H1 low to $\overline{STRB}$ high for a $\overline{HOLD}$ 5/	t_{d36}			0	9	
Disable time, from H1 low to $\overline{STRB}$ high-Z state 4/ 5/	t_{dis4}			0	9	
Enable time, from H1 low to $\overline{STRB}$ active 5/	t_{en1}		9, 10, 11	0	9	ns
Disable time, from H1 low to R/$\overline{W}$ high-Z state 4/ 5/	t_{dis5}			0	9	
Enable time, from H1 low to R/$\overline{W}$ active 5/	t_{en2}			0	9	
Disable time, from H1 low to address high-Z state 4/ 5/	t_{dis6}		9, 10, 11	0	10	ns
Enable time, from H1 low to address valid 5/	t_{en3}			0	13	
Disable time, from H1 high to data high-Z state 4/ 5/	t_{dis7}			0	9	
Setup time, general purpose input before H1 low	t_{su17}	Peripheral pin general General purpose I/O timing See figure 4	9, 10, 11	10		ns
Hold time, general-purpose input after H1 low	t_{h13}			0		
Delay time, general purpose output after H1 high	t_{d37}				13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Setup time, TCLK ext before H1 low	t_{su18}	Timer pin timing See figure 4		9, 10, 11	10		ns
Hold time, TCLK ext after H1 low	t_{h14}				0		
Delay time, TCLK int valid after H1 high	t_{d38}					9	
Cycle time, TCLK	t_c		External		t_{c2} x 2.6		
			Internal		t_{c2}x 2	t_{c2} x 2^{32}	
Pulse width, TCLK high/low	t_w		External		t_{c2}+ 10		
			Internal		t_{c4}/2-5	t_{c4}/2+5	
Hold time, peripheral pin after H1 high	t_{h15}	Change of peripheral pin from general purpose output to input mode See figure 4		9, 10, 11		13	ns
Setup time, peripheral pin before H1 low	t_{su19}				9		
Hold time, peripheral pin after H1 low	t_{h16}				0		
Delay time, from H1 high to peripheral pin switching from input to output	t_{d39}	Change of peripheral pin from general purpose input to output mode See figure 4		9, 10, 11		13	ns
Disable time, $\overline{SHZ}$ low to all O, IO high-Z 4/ 5/	t_{dis8}	$\overline{SHZ}$ [P = t_c (CI)] pin timing See figure 4		9, 10, 11	0	2P	ns

1/ Unless otherwise specified, $3.13 V \le V_{DD} \le 3.47 V$. All other test conditions shall be worst case conditions unless otherwise specified.

2/ Pins with internal pull-up devices: $\overline{INT(3-0)}$, MCBL/$\overline{MP}$, RSV (0-10). Although RSV (0-10) have internal pull-up devices, external pull-ups should be used on each pin.

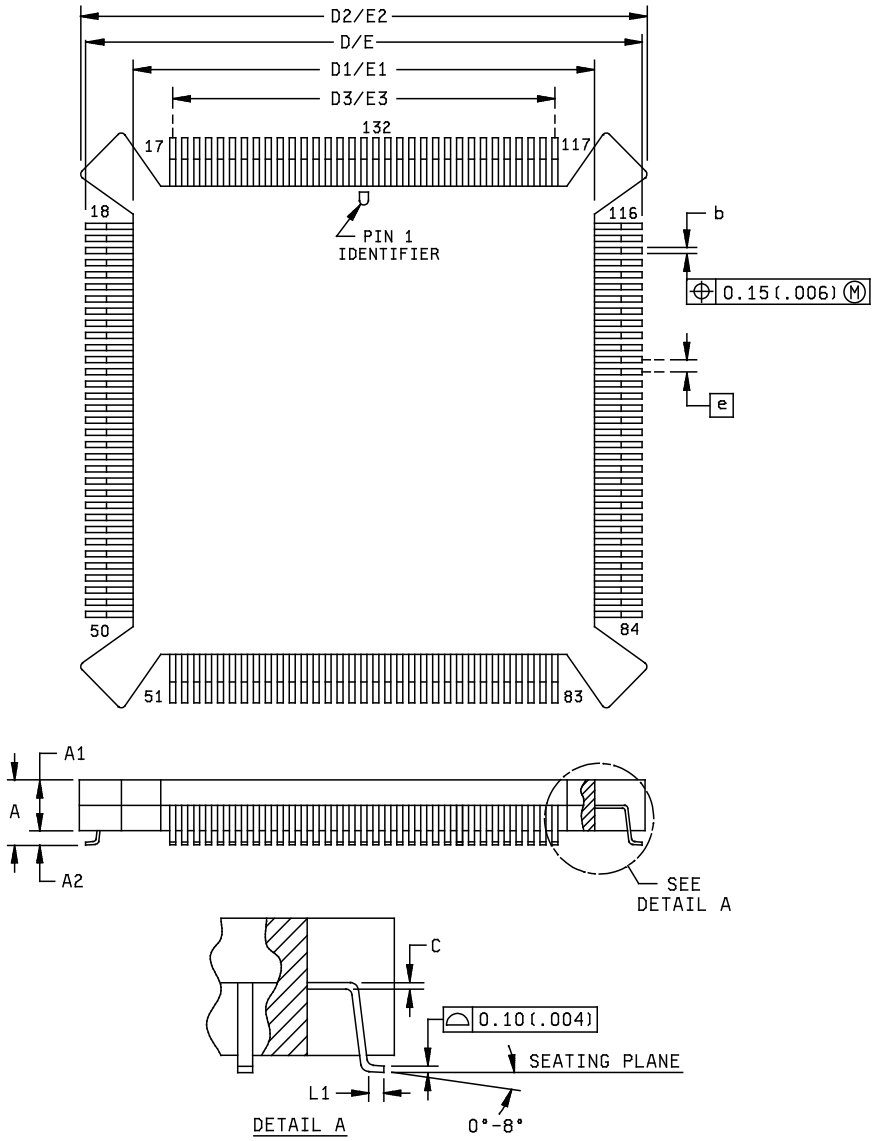
3/ Actual operating current will be less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the primary bus at the maximum rate possible.

4/ Maximum limit is not production tested.

5/ Minimum limit is not production tested.

6/ Interrupt pulse width must be at least 1P wide to guarantee it will be seen. It must be less than 2P wide to guarantee it will be responded to only once. The recommended pulse width is 1.5P. P = one H1 cycle.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		4.57		.180	D1/E1	23.72	24.54	.934	.966
A1	3.30	3.81	.130	.150	D2/E2	27.64	28.25	1.088	1.112
A2	0.51		.020		D3/E3	20.32 BSC		.800 BSC	
b	0.20	0.30	.008	.012	e	0.635 BSC		.025 BSC	
c	0.16 BSC		.006 BSC		L1	0.91	1.17	.036	.046
D/E	27.18	27.69	1.070	1.090					

FIGURE 1. Case outline.

Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A21	34	D30	67	D9	100	$\overline{INT0}$
2	A20	35	V_{SS}	68	D8	101	V_{SS}
3	V_{SS}	36	V_{SS}	69	V_{SS}	102	V_{SS}
4	V_{SS}	37	V_{SS}	70	V_{SS}	103	$\overline{INT1}$
5	A19	38	D29	71	V_{SS}	104	V_{DD}
6	V_{DD}	39	D28	72	D7	105	V_{DD}
7	A18	40	V_{DD}	73	D6	106	$\overline{INT2}$
8	A17	41	D27	74	V_{DD}	107	$\overline{INT3}$
9	A16	42	V_{SS}	75	D5	108	DR0
10	A15	43	D26	76	D4	109	V_{SS}
11	A14	44	D25	77	D3	110	FSR0
12	A13	45	D24	78	D2	111	CLKR0
13	A12	46	D23	79	D1	112	CLKX0
14	A11	47	D22	80	D0	113	V_{SS}
15	V_{DD}	48	D21	81	H1	114	FSX0
16	A10	49	V_{DD}	82	H3	115	V_{DD}
17	V_{SS}	50	D20	83	V_{DD}	116	DX0
18	A9	51	V_{SS}	84	V_{SS}	117	V_{SS}
19	V_{SS}	52	D19	85	V_{SS}	118	$\overline{SHZ}$
20	A8	53	D18	86	V_{SS}	119	V_{SS}
21	A7	54	D17	87	X2/CLKIN	120	TLCK0
22	A6	55	D16	88	X1	121	V_{DD}
23	A5	56	D15	89	$\overline{HOLDA}$	122	TLCK1
24	V_{DD}	57	V_{SS}	90	$\overline{HOLD}$	123	EMU3
25	A4	58	D14	91	V_{DD}	124	EMU0
26	A3	59	V_{DD}	92	$\overline{RDY}$	125	EMU1
27	A2	60	D13	93	$\overline{STRB}$	126	EMU2
28	A1	61	V_{SS}	94	R/$\overline{W}$	127	MCBL/$\overline{MP}$
29	A0	62	D12	95	$\overline{RESET}$	128	V_{SS}
30	V_{SS}	63	D11	96	XF0	129	A23
31	D31	64	D10	97	V_{DD}	130	A22
32	V_{DD}	65	V_{DD}	98	XF1	131	V_{DD}
33	V_{DD}	66	V_{DD}	99	$\overline{IACK}$	132	V_{DD}

FIGURE 2. Terminal connections.

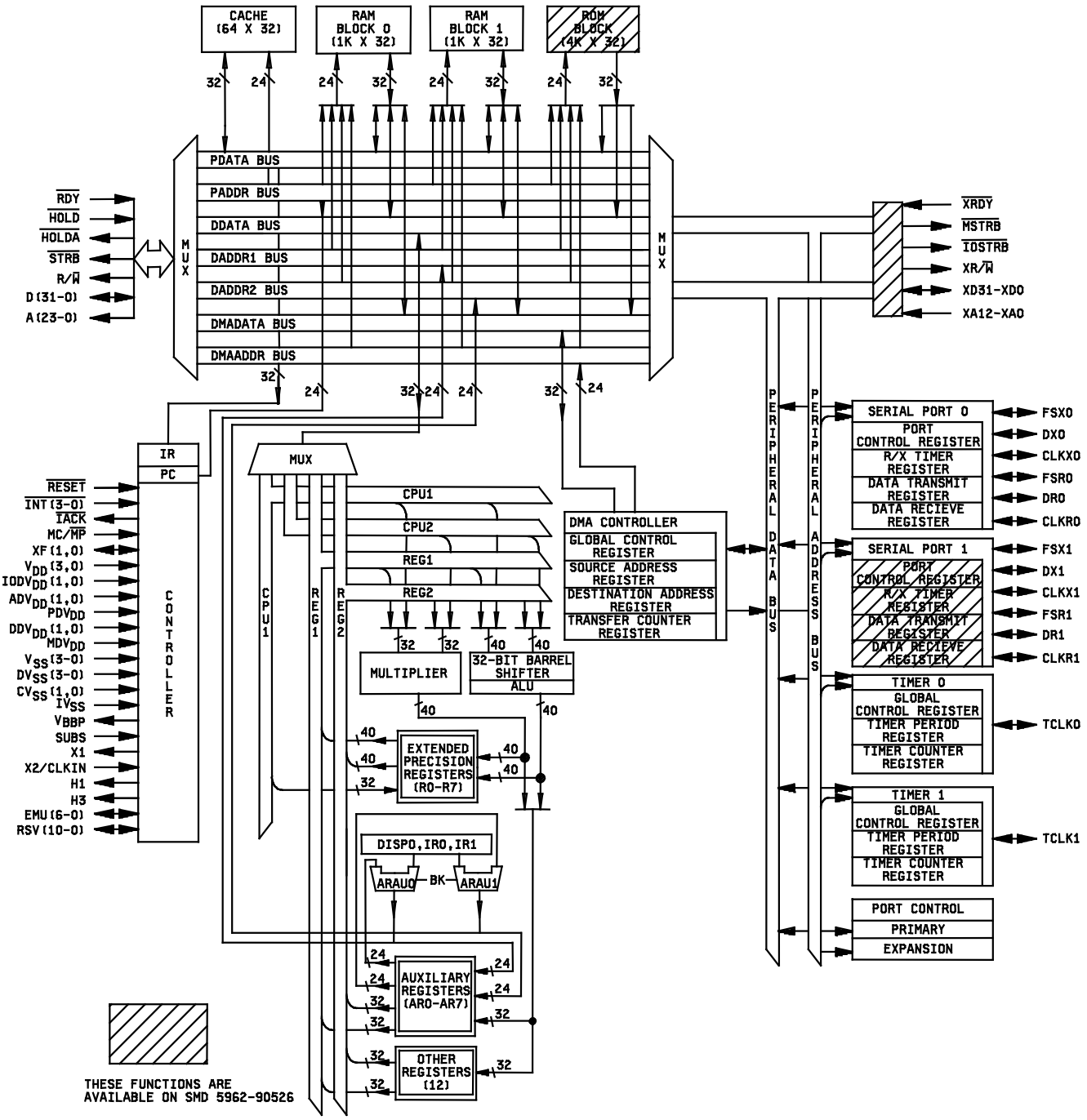
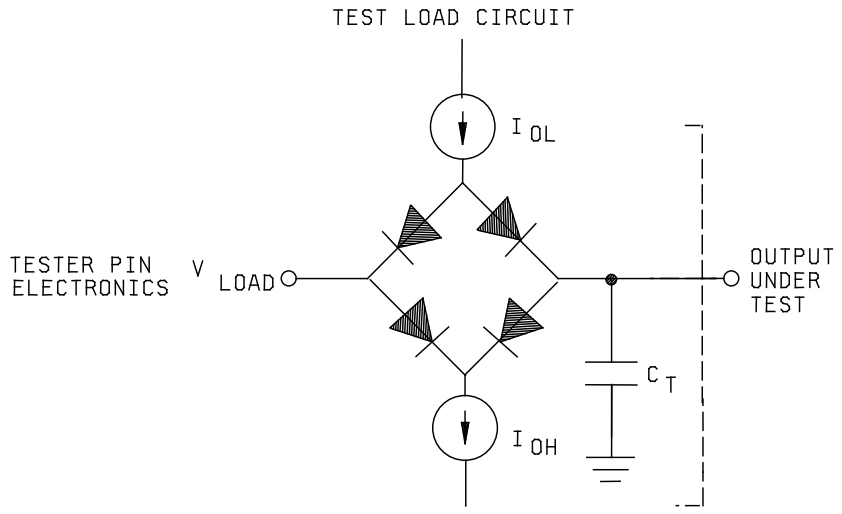


FIGURE 3. Functional block diagram.



Where: I_{OL} = 2.0 mA (all outputs)
I_{OH} = 300 μA (all outputs)
V_{LOAD} =1.54 V to emulate 50Ω
C_T = 80 pF typical load circuit capacitance.

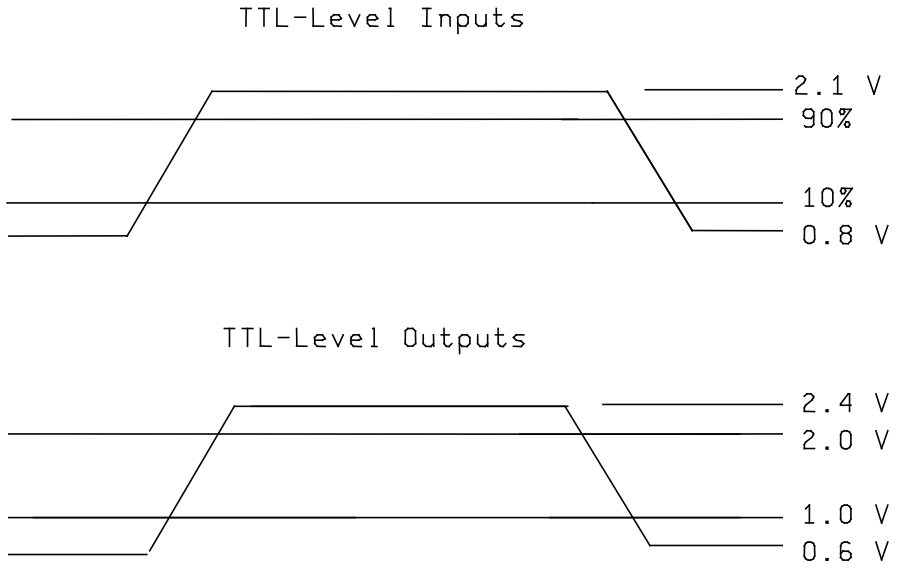
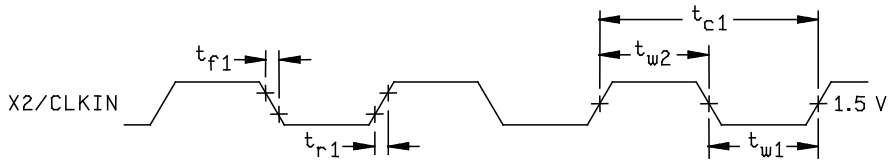
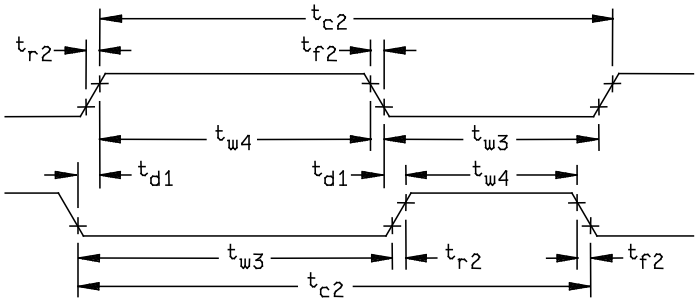


FIGURE 4. Switching waveforms and test circuit.

X2/CLKIN TIMING



H1/H3 TIMING



Memory ((M) $\overline{\text{STRB}}$ = 0) Read

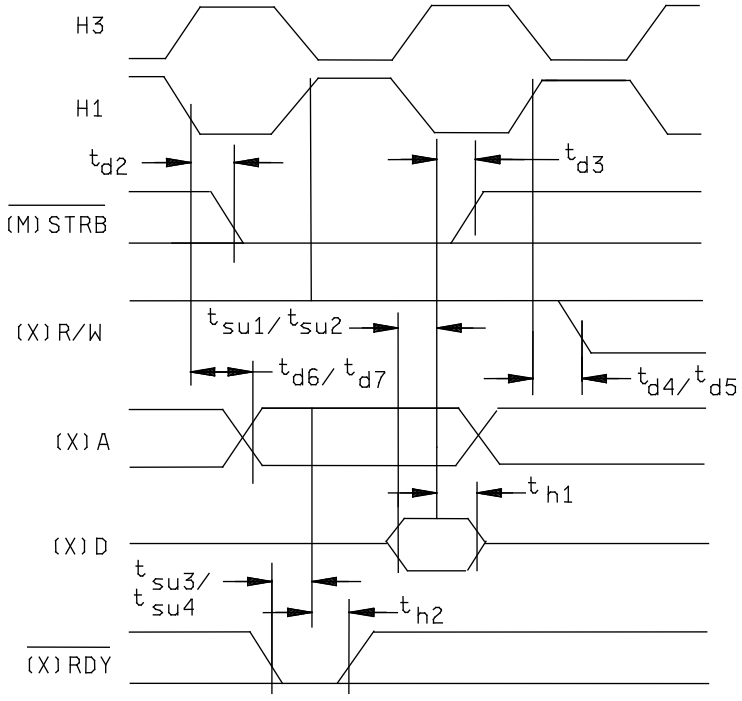
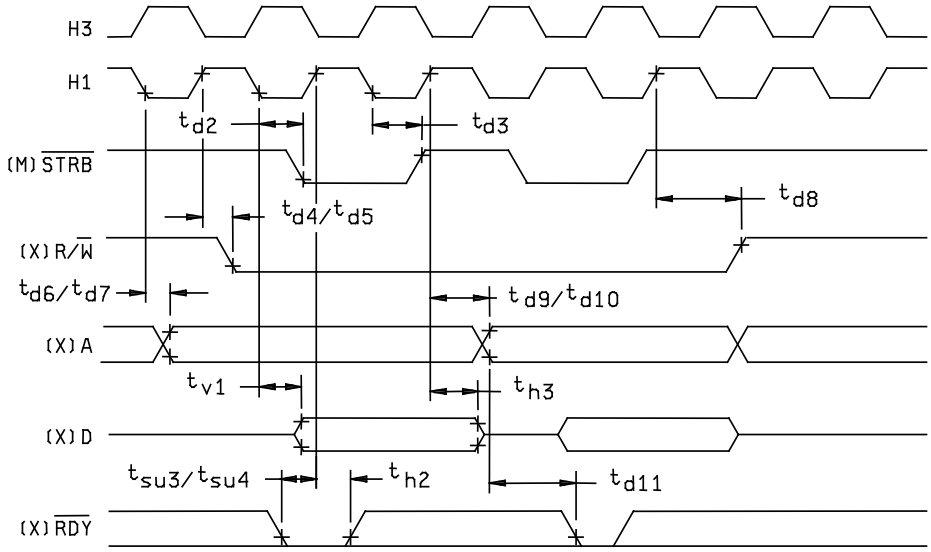


FIGURE 4. Switching waveforms and test circuit - Continued.

MEMORY ((M) $\overline{\text{STRB}}$=0) WRITE



MEMORY ((IO) $\overline{\text{STRB}}$=0) READ

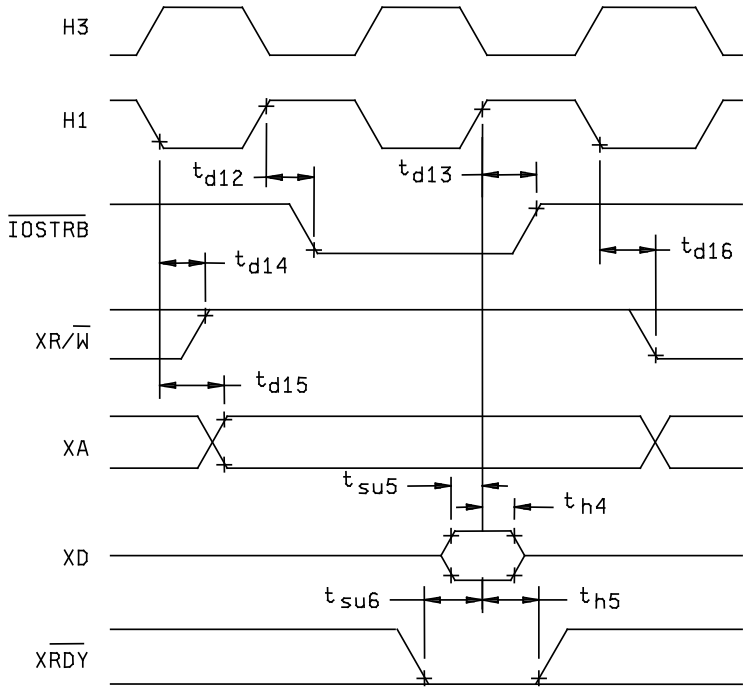
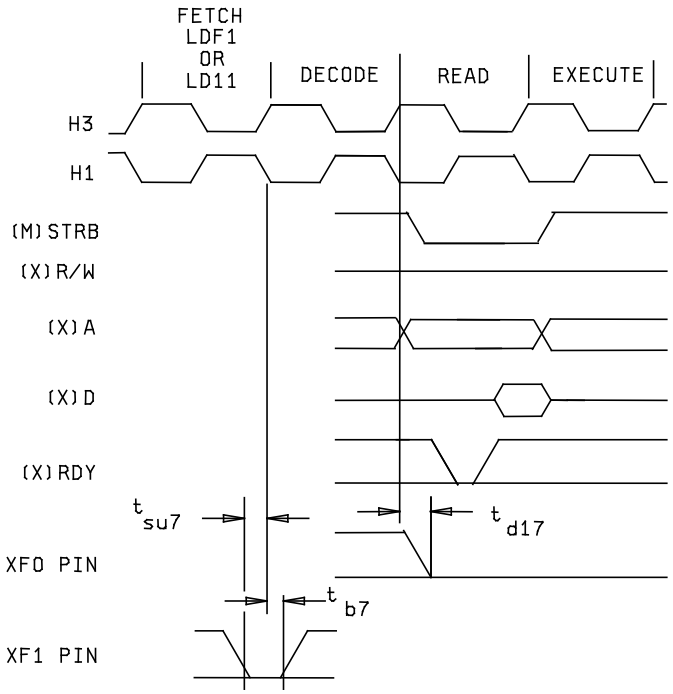


FIGURE 4. Switching waveforms and test circuit - Continued.

TIMING XFO AND XF1 WHEN EXECUTING LDF1 OR LDII



TIMING SFO WHEN EXECUTING STF1 OR STII

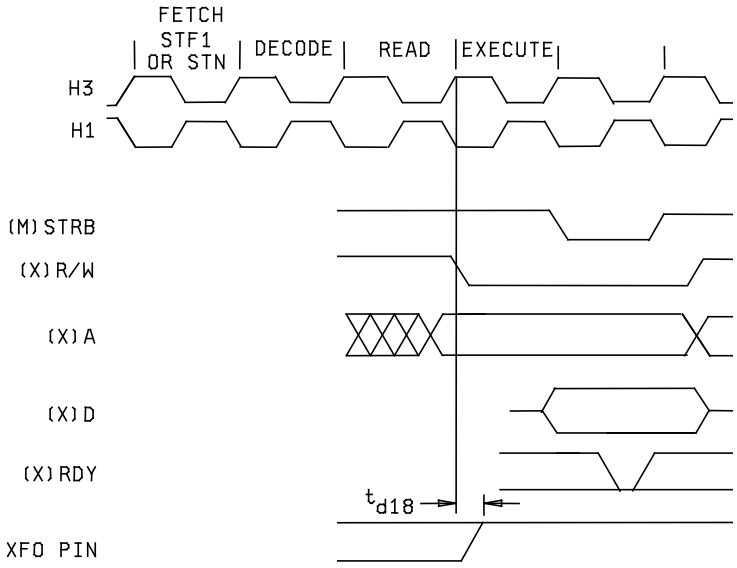
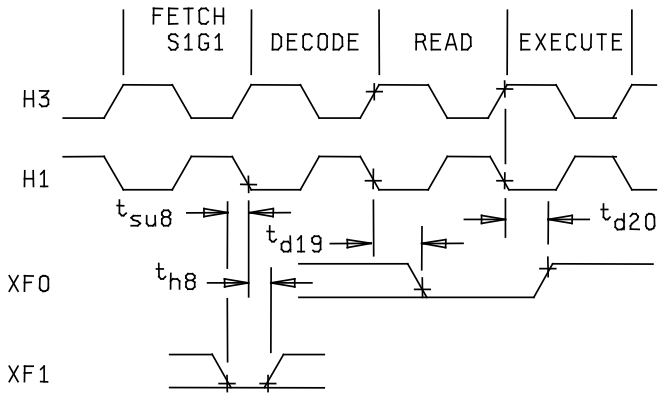


FIGURE 4. Switching waveforms and test circuit - Continued.

TIMING FOR XFO AND XF1 WHEN EXECUTING SIGI



TIMING FOR LOADING XF REGISTER WHEN CONFIGURED AS AN OUTPUT PIN

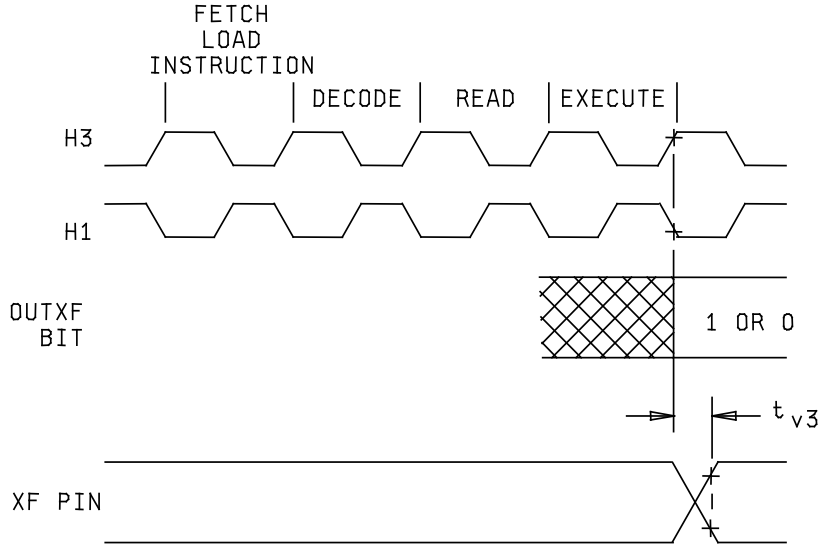
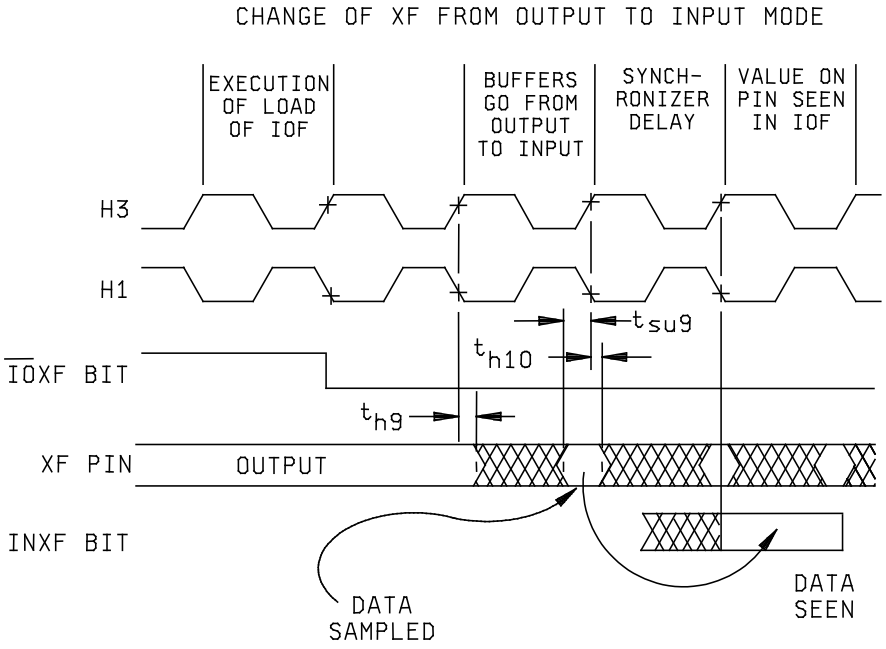


FIGURE 4. Switching waveforms and test circuit - Continued.



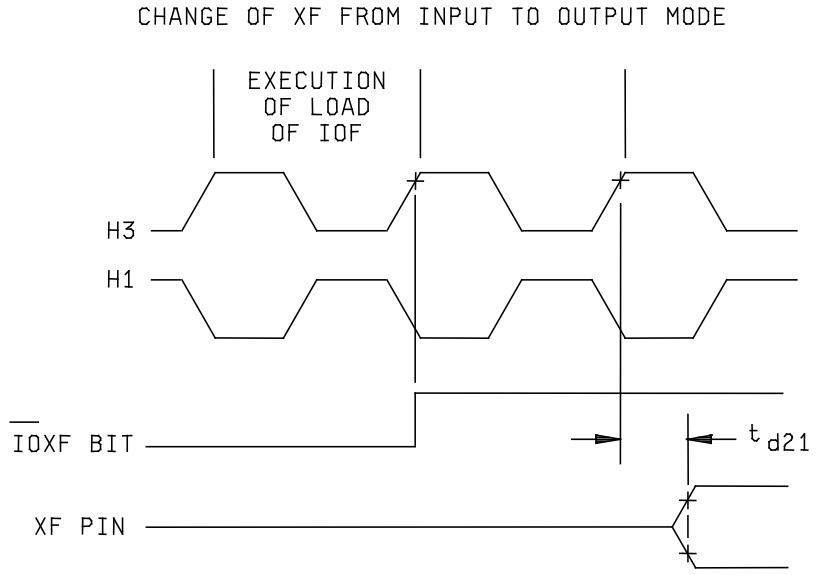
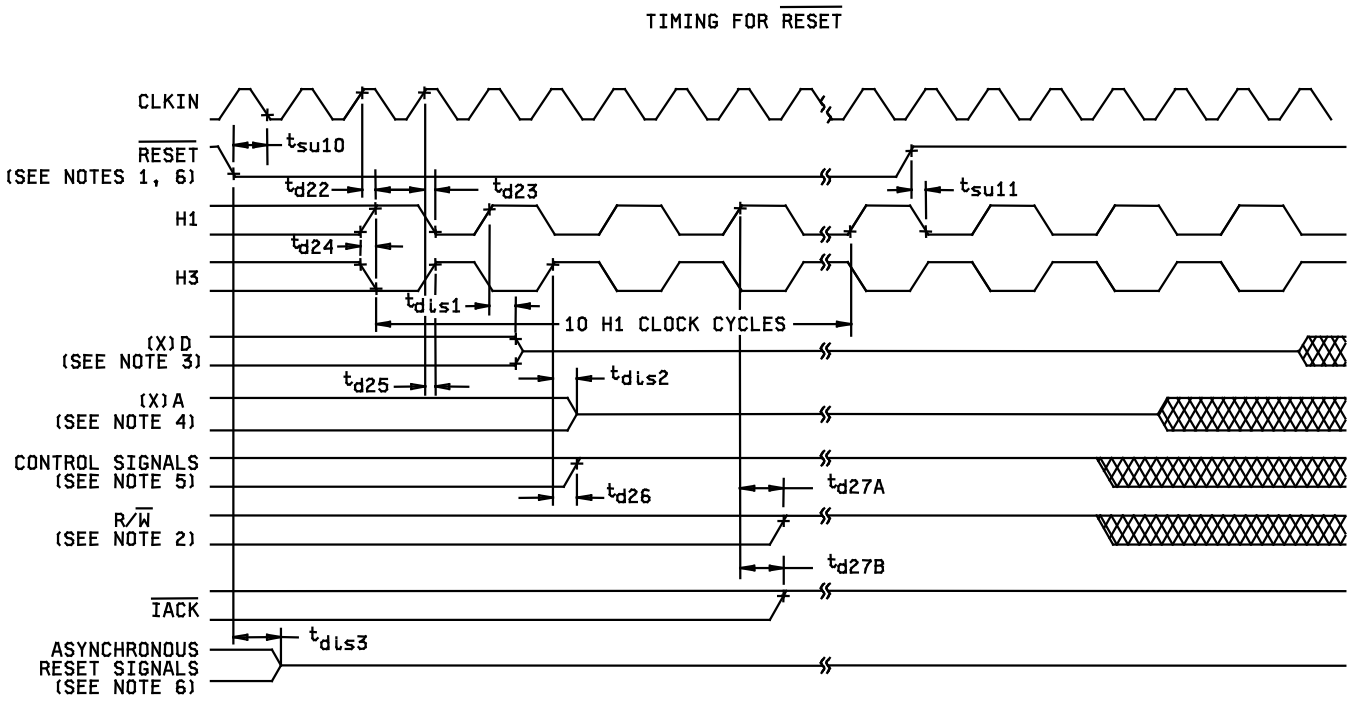


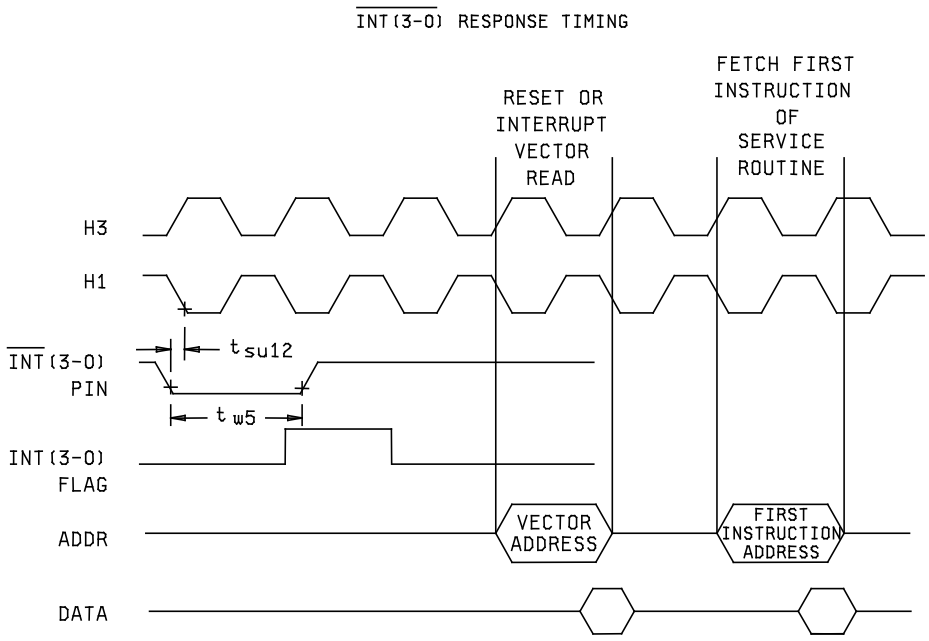
FIGURE 4. Switching waveforms and test circuit - Continued.



NOTES:

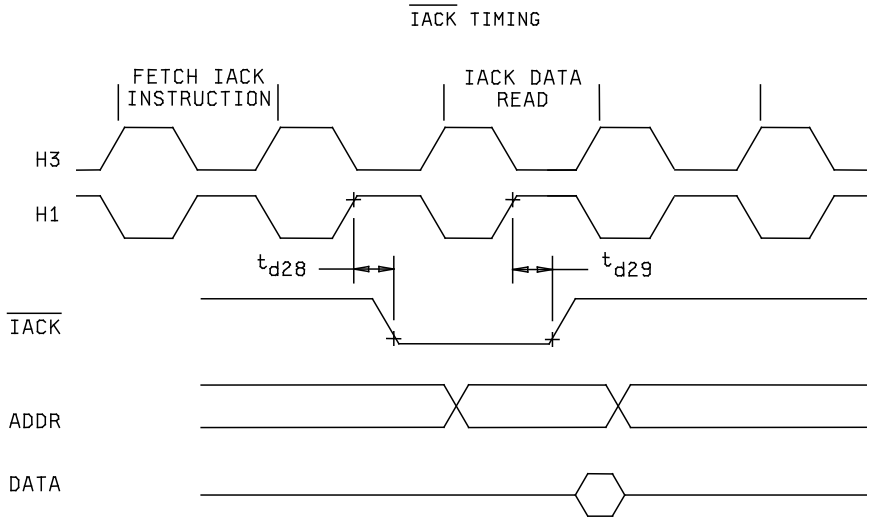
1. $\overline{\text{RESET}}$ is asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.
2. Note that the R/$\overline{\text{W}}$ outputs are placed in a high impedance state during reset and can be provided with a resistive pull-up, nominally 20 KΩ, if desirable spurious writes could be caused when these outputs go low.
3. (X)D includes D(31-0) and XD(31-0).
4. (X)A includes A(23-0), XA(12-0).
5. Control signals include $\overline{\text{STRB}}$, $\overline{\text{MSTRB}}$, and $\overline{\text{IOSTRB}}$.
6. Asynchronously reset signals include XF1, XF0, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, CLKX1, DX1, FSX1, CLKR1, DR1, FSR1, TCLK0, and TCLK1.

FIGURE 4. Switching waveforms and test circuit - Continued.



NOTES:

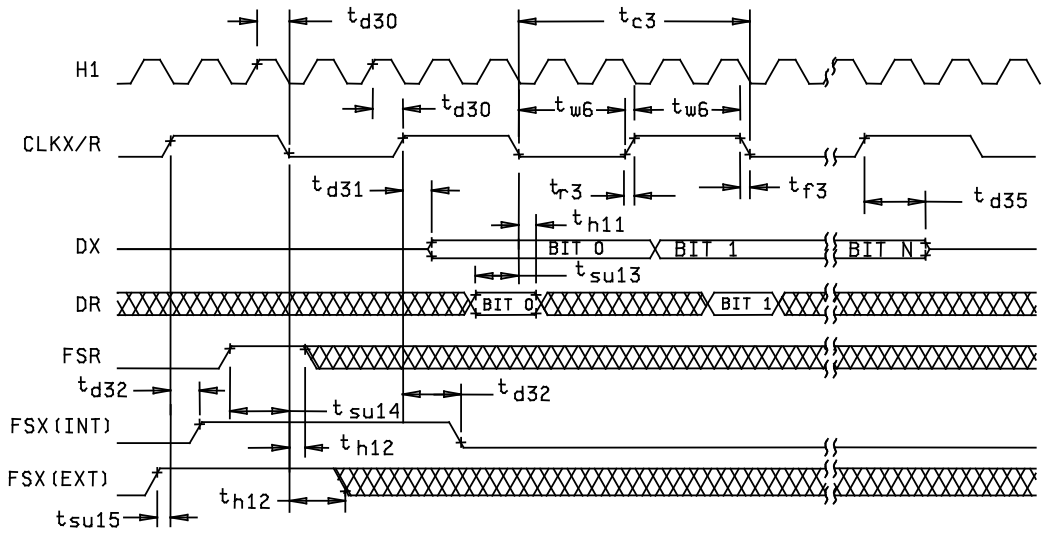
1. Interrupt pulse width must be at least 1P wide to guarantee it will be seen. It must be less than 2P wide to guarantee it will be responded to only once. The recommended pulse width is 1.5P.
2. $\overline{\text{INT}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.



NOTE: The $\overline{\text{IACK}}$ output is active for the entire duration of the bus cycle and is therefore extended if the bus cycle utilized wait states.

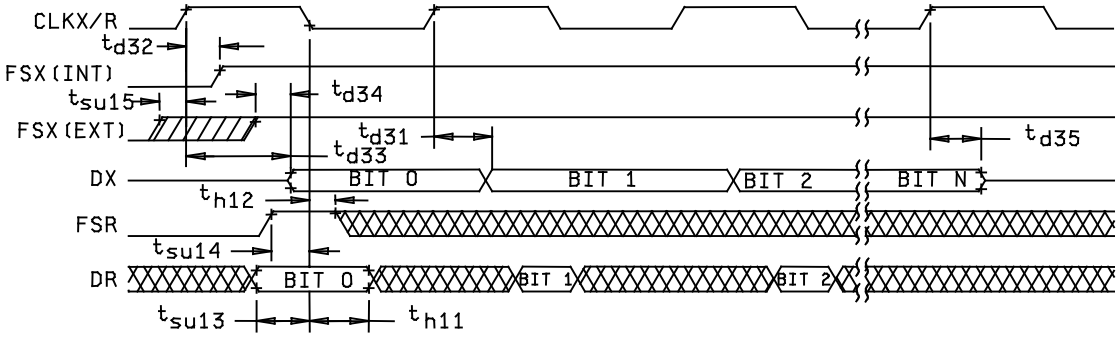
FIGURE 4. Switching waveforms and test circuit - Continued.

FIXED DATA RATE MODE



NOTES:
1. Timings diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0
2. These timings are valid for all serial port modes, including handshake, except where otherwise indicated.

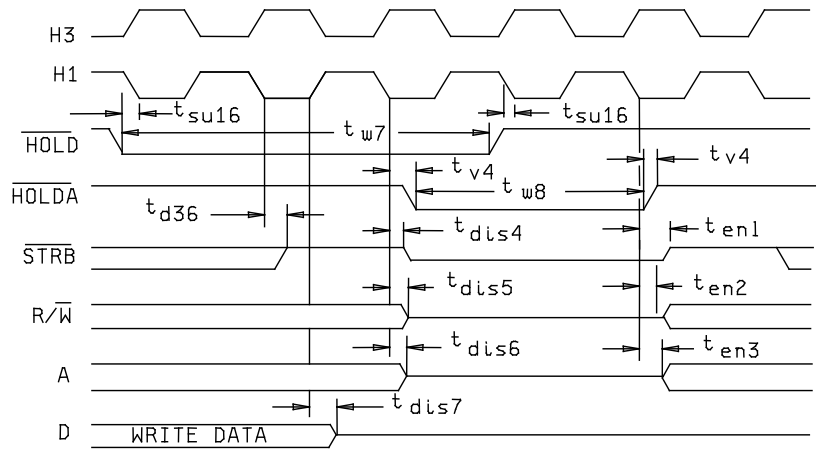
VARIABLE DATA RATE MODE



NOTES:
1. Timing diagrams show operation with CLKXP = XLKRP = FSXP = FSRP = 0
2. Timings not expressly specified for variable data rate mode are the same as those for fixed data rate mode.
3. Timings are valid for all serial port modes, includes handshake mode, except where otherwise indicated.

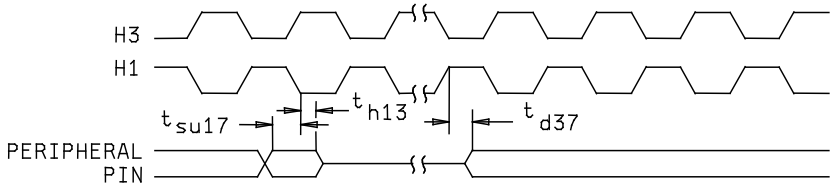
FIGURE 4. Switching waveforms and test circuit - Continued.

$\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ TIMING



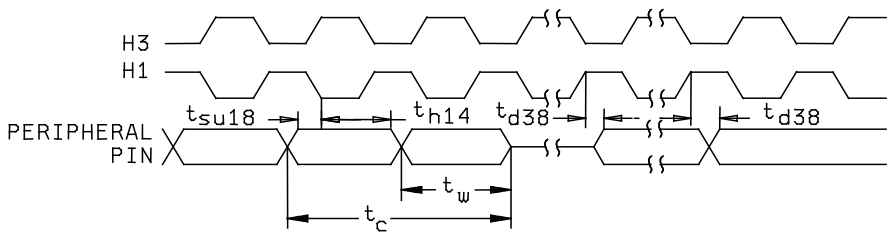
NOTE: $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.

PERIPHERAL PIN GENERAL-PURPOSE I/O TIMING



NOTE: Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1 FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

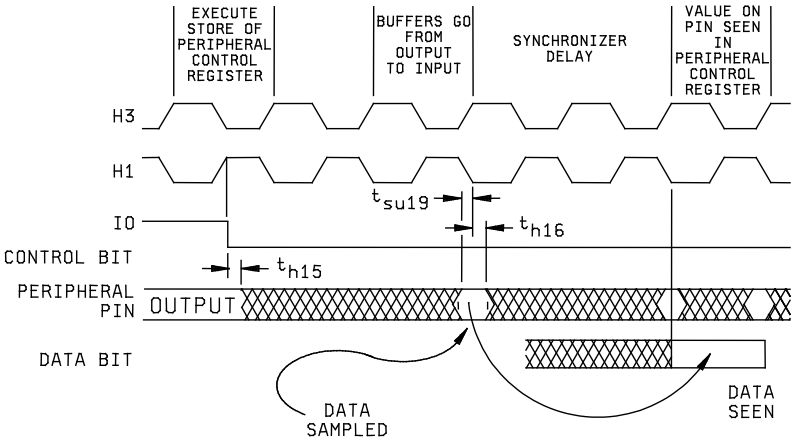
TIMER PIN TIMINGS



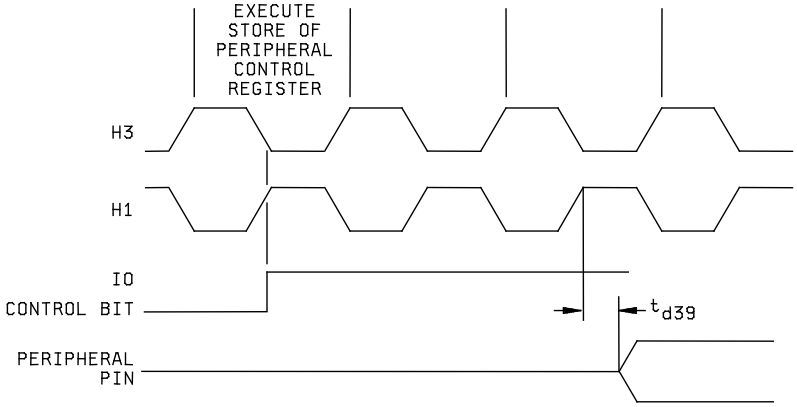
NOTE: Period and polarity of valid logic level are specified by contents of internal control registers.

FIGURE 4. Switching waveforms and test circuit - Continued.

CHANGE OF PERIPHERAL PIN FROM GENERAL PURPOSE OUTPUT TO INPUT MODE



CHANGE OF PERIPHERAL PIN FROM GENERAL PURPOSE INPUT TO OUTPUT MODE



Timing for $\overline{SHZ}$

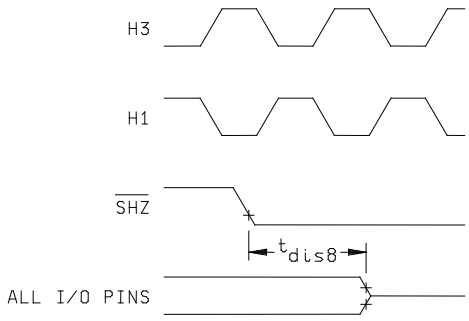


FIGURE 4. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8 9, 10, 11 1/	1, 2, 3, 7, 8 9, 10, 11 1/	1, 2, 3, 7, 8 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply. Sources of supply for device classes N, Q, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Application note. Devices supplied to this drawing have been known to exhibit cold start sensitivity. Contact the device manufacturer for further information or see the manufacture's literature, SGUA001, for more detail information.

TABLE III. Terminal description.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
PRIMARY-BUS INTERFACE			
D31–D0	I/O/Z	32-bit data port	S H R
A23–A0	O/Z	24-bit address port	S H R
R/$\overline{W}$	O/Z	Read/write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S H R
$\overline{STRB}$	O/Z	External-access strobe	S H
$\overline{RDY}$	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion.	
$\overline{HOLD}$	I	Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed, A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are placed in the high-impedance state and all transactions over the primary-bus interface are held until $\overline{HOLD}$ becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.	
$\overline{HOLDA}$	O/Z	Hold acknowledge. $\overline{HOLDA}$ is generated in response to a logic low on $\overline{HOLDA}$. $\overline{HOLDA}$ indicates that A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{HOLDA}$ is high in response to a logic high of $\overline{HOLD}$ or the NOHOLD bit of the primary-bus-control register is set.	S
CONTROL SIGNALS			
$\overline{RESET}$	I	Reset. When $\overline{RESET}$ is a logic low, the device is in the reset condition. When $\overline{RESET}$ becomes a logic high, execution begins from the location specified by the reset vector.	
$\overline{INT3}$ – $\overline{INT0}$	I	External interrupts	
$\overline{IACK}$	O/Z	Interrupt acknowledge. $\overline{IACK}$ is generated by the IACK instruction. $\overline{IACK}$ can be used to indicate the beginning or the end of an interrupt-service routine.	S
MCBL/$\overline{MP}$	I	Microcomputer boot-loader/microprocessor mode-select	
$\overline{SHZ}$	I	Shutdown high-impedance. When active, $\overline{SHZ}$ shuts down the device and places all pins in the high-impedance state. $\overline{SHZ}$ is used for board-level testing to ensure that no dual-drive conditions occur. Caution: A low on $\overline{SHZ}$ corrupts the device memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.	
XF1, XF0	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S R

See footnotes at end of table.

TABLE III. Terminal description - Continued.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/	
SERIAL PORT 0 SIGNALS				
CLKR0	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S	R
CLKX0	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S	R
DR0	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S	R
DX0	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S	R
FSR0	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S	R
FSX0	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S	R
TIMER SIGNALS				
TCLK0	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S	
TCLK1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses, As an output, TCLK1 outputs pulses generated by timer 1.	S	
SUPPLY AND OSCILLATOR SIGNALS				
H1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S	
H3	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S	
V_{DD}	I	3.3-V supply for the device. All must be connected to a common supply plane. 3/		
V_{SS}	I	Ground. All grounds must be connected to a common ground plane.		
X1	O	Output from the internal-crystal oscillator. If a crystal is not used, X1 should be left unconnected.		
X2/CLKIN	I	Internal-oscillator input from a crystal or a clock.		
RESERVED 4/				
EMU2–EMU0	I	Reserved for emulation. Use pullup resistors to V_{DD}		
EMU3	O/Z	Reserved for emulation	S	

1/ I = input, O = output, Z = high-impedance state.

2/ S = $\overline{\text{SHZ}}$ active, H = $\overline{\text{HOLD}}$ active, R = $\overline{\text{RESET}}$ active.

3/ Recommended decoupling capacitor value is 0.1 μF.

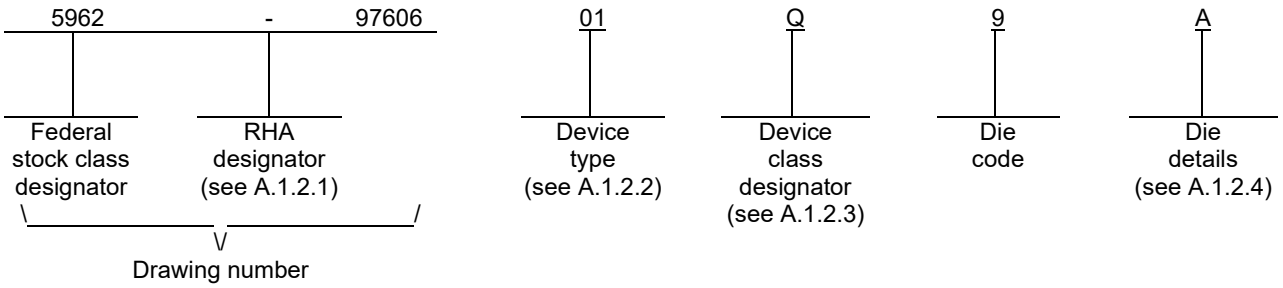
4/ Follow the connections specified for the reserved pins. Use 18-kΩ – 22-kΩ pullup resistors for best results. All V_{DD} supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-97606

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320LC31	Digital signal processor, 40 MHz

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOK

MIL-HDBK-103 - List of Standard Microcircuit Drawings
MIL-HDBK-780 - Standard Microcircuit Drawings

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan, for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stacks of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883, method 5007.

b) 100% wafer probe (see paragraph A.3.4 herein).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883, method 2010 or the alternate procedures allowed within MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0591.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

Die physical dimensions.

Die size:	296 mils x 317 mils.
Die thickness:	19 mils.

Interface materials.

Top metallization:	Ti/TiW/AlSiCu.5 500Å/3kÅ/4.5kÅ
Backside metallization:	Silicon

Glassivation.

Type:	Ox/N
Thickness:	3kÅ/ kÅ

Substrate: Silicon

Assembly related information.

Substrate potential:	Biased to Ground
Special assembly instructions:	None

FIGURE A-1. Die bonding pad locations and electrical functions.

PAD	X CENTER	Y CENTER	PAD NAME	PAD	X CENTER	Y CENTER	PAD NAME
1	0.00	0.00	A9	34	396.72	-7219.80	DV_{SS}
2	0.00	-224.46	DV_{SS}	35	577.44	-7219.80	D19
3	0.00	-426.24	A8	36	780.30	-7219.80	D18
4	0.00	-650.70	A7	37	990.36	-7219.80	D17
5	0.00	-875.16	A6	38	1200.42	-7219.80	D16
6	0.00	-1099.62	A5	39	1410.48	-7219.80	D15
7	0.00	-1302.48	AV_{DD}	40	1598.94	-7219.80	CV_{SS}
8	0.00	-1504.26	A4	41	1786.32	-7219.80	D14
9	0.00	-1728.72	A3	42	1974.78	-7219.80	DV_{DD}
10	0.00	-1953.18	A2	43	2162.16	-7219.80	D13
11	0.00	-2177.64	A1	44	2350.62	-7219.80	IV_{SS}
12	0.00	-2402.10	A0	45	2538.00	-7219.80	D12
13	0.00	-2604.96	CV_{SS}	46	2748.06	-7219.80	D11
14	0.00	-2828.34	D31	47	2958.12	-7219.80	D10
15	0.00	-3100.32	V_{DDL}	48	3150.90	-7219.80	V_{DDL}
16	0.00	-3262.68	V_{DDL}	49	3313.26	-7219.80	V_{DDL}
17	0.00	-3463.20	D30	50	3499.38	-7219.80	D9
18	0.00	-3670.38	V_{SSL}	51	3709.44	-7219.80	D8
19	0.00	-3832.74	V_{SSL}	52	3897.90	-7219.80	DV_{SS}
20	0.00	-4011.66	DV_{SS}	53	4068.00	-7219.80	V_{SSL}
21	0.00	-4256.64	D29	54	4230.36	-7219.80	V_{SSL}
22	0.00	-4481.10	D28	55	4416.48	-7219.80	D7
23	0.00	-4669.56	DV_{DD}	56	4626.54	-7219.80	D6
24	0.00	-4950.54	D27	57	4815.00	-7219.80	DV_{DD}
25	0.00	-5153.40	IV_{SS}	58	5002.38	-7219.80	D5
26	0.00	-5333.58	D26	59	5212.44	-7219.80	D4
27	0.00	-5536.44	D25	60	5422.50	-7219.80	D3
28	0.00	-5739.30	D24	61	5632.56	-7219.80	D2
29	0.00	-5942.16	D23	62	5842.62	-7219.80	D1
30	0.00	-6145.02	D22	63	6052.68	-7219.80	D0
31	0.00	-6347.88	D21	64	6262.74	-7219.80	H1
32	0.00	-6522.48	DV_{DD}	65	6472.80	-7219.80	H3
33	0.00	-6699.46	D20	66	6646.86	-7219.80	DV_{DD}

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

PAD	X CENTER	Y CENTER	PAD NAME	PAD	X CENTER	Y CENTER	PAD NAME
67	7136.64	-6714.54	DV_{SS}	100	6705.00	452.52	SUBSTRATE
68	7136.64	-6555.96	CV_{SS}	101	6480.90	452.52	$\overline{SHZ}$
69	7136.64	-6402.42	IV_{SS}	102	6298.92	452.52	DV_{SS}
70	7136.64	-6241.86	X2/CLKIN	103	6125.94	452.52	TCLK0
71	7136.64	-6072.30	X1	104	5951.88	452.52	PV_{DD}
72	7136.64	-5780.16	$\overline{HOLDA}$	105	5721.30	452.52	TCLK1
73	7136.64	-5574.60	$\overline{HOLD}$	106	5439.24	452.52	EMU3
74	7136.64	-5392.62	CV_{DD}	107	5248.08	452.52	EMU0
75	7136.64	-5116.14	$\overline{RDY}$	108	5063.40	452.52	EMU1
76	7136.64	-4898.16	$\overline{STRB}$	109	4878.72	452.52	EMU2
77	7136.64	-4673.70	R/ $\overline{W}$	110	4694.04	452.52	MCBL/ $\overline{MP}$
78	7136.64	-4453.74	$\overline{RESET}$	111	4526.46	452.52	CV_{SS}
79	7136.64	-4235.76	XF0	112	4324.68	452.52	A23
80	7136.64	-4032.90	CV_{DD}	113	4129.02	452.52	A22
81	7136.64	-3809.52	XF1	114	3862.62	452.52	V_{DDL}
82	7136.64	-3585.06	$\overline{IACK}$	115	3700.26	452.52	V_{DDL}
83	7136.64	-3365.10	$\overline{INT0}$	116	3421.98	452.52	A21
84	7136.64	-3168.72	DV_{SS}	117	3226.50	452.52	A20
85	7136.64	-2988.54	V_{SSL}	118	3052.44	452.52	V_{SSL}
86	7136.64	-2791.26	$\overline{INT1}$	119	2901.06	452.52	DV_{SS}
87	7136.64	-2590.56	V_{DDL}	120	2728.08	452.52	A19
88	7136.64	-2428.20	V_{DDL}	121	2554.02	452.52	AV_{DD}
89	7136.64	-2232.18	$\overline{INT2}$	122	2381.04	452.52	A18
90	7136.64	-2018.70	$\overline{INT3}$	123	2185.38	452.52	A17
91	7136.64	-1750.32	DR0	124	1989.72	452.52	A16
92	7136.64	-1547.46	CV_{SS}	125	1794.06	452.52	A15
93	7136.64	-1345.68	FSR0	126	1598.40	452.52	A14
94	7136.64	-1121.22	CLKR0	127	1316.34	452.52	A13
95	7136.64	-896.76	CLKX0	128	1120.68	452.52	A12
96	7136.64	-693.90	IV_{SS}	129	925.02	452.52	A11
97	7136.64	-492.12	FSX0	130	750.96	452.52	AV_{DD}
98	7136.64	-289.26	PV_{DD}	131	577.98	452.52	A10
99	7136.64	-15.48	DX0	132	403.92	452.52	CV_{SS}

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-05-08

Approved sources of supply for SMD 5962-97606 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9760601Q9A	3/	SMJ320LC31KGDM40B
5962-9760601NXB	01295	SMQ320LC31PQM40

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243