

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. - gap	07-01-18	Raymond Monnin
B	Remove all class M references. Update to current MIL-PRF-38535 requirements. - rdc	17-01-20	Charles Saffle
C	Update drawing to latest MIL-PRF-38535 requirements. - jt	21-12-07	James R. Eschmeyer



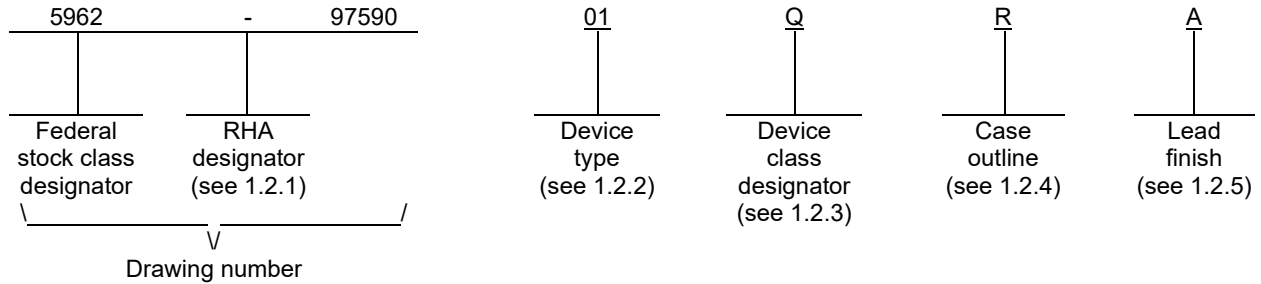
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REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13						

PMIC N/A	PREPARED BY Rick Officer	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY Rajesh Pithadia																		
	APPROVED BY Raymond Monnin	<p align="center">MICROCIRCUIT, DIGITAL, ADVANCED SCHOTTKY TTL, OCTAL EDGE TRIGGERED D-TYPE FLIP FLOPS WITH THREE STATE OUTPUTS, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 97-06-19																		
	AMSC N/A	REVISION LEVEL C	SIZE A	CAGE CODE 67268	5962-97590														
		SHEET		1 OF 13															

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54F374	Octal edge triggered D-type flip flops with three state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. ^{1/}

Supply voltage range (V _{CC})	-0.5 V to +7.0 V
Input voltage range (V _{IN})	-1.2 V to +7.0 V ^{2/}
Input current range (I _{IN})	-30 mA and +5 mA
Voltage range applied to any output in the high state	-0.5 V to V _{CC}
Voltage range applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Current into any output in the low state	40 mA
Power dissipation (P _D)	700 mW
Storage temperature range	-65°C to +150°C
Junction temperature (T _J)	+175°C
Thermal resistance, junction-to-case (θ _{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V _{CC})	4.5 V to 5.5 V
High-level input voltage (V _{IH})	2 V
Low-level input voltage (V _{IL})	0.8 V
Input clamp current (I _{IK})	-18 mA
High-level output current (I _{OH})	-3 mA
Low-level output current (I _{OL})	20 mA
Case operating free-air temperature (T _c)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

^{1/} Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

^{2/} The input voltage ratings may be exceeded provided the input current ratings are observed.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Timing diagram. The timing diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	1, 2, 3	All		-1.2	V
High-level output voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -1 mA	1, 2, 3	All	2.5		V
		V _{CC} = 4.5 V, I _{OH} = -3 mA			2.4		
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA	1, 2, 3	All		0.5	V
High level output impedance current	I _{ozH}	V _{CC} = 5.5 V, V _O = 2.7 V	1, 2, 3	All		50	μA
Low level output impedance current	I _{ozL}	V _{CC} = 5.5 V, V _O = 0.5 V	1, 2, 3	All		-50	μA
Input current	I _I	V _{CC} = 5.5 V, V _I = 7 V	1, 2, 3	All		0.1	mA
High level input current	I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	1, 2, 3	All		20	μA
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _I = 0.5 V	1, 2, 3	All		-0.6	mA
Output short circuit <u>1/</u> current	I _{os}	V _{CC} = 5.5 V, V _O = 0 V	1, 2, 3	All	-60	-150	mA
Impedance supply current	I _{cc}	V _{CC} = 5.5 V <u>2/</u>	1, 2, 3	All		86	mA
Functional test	<u>3/</u>	V _{IN} = V _{IH} min or V _{IL} max verify output V _O , see 4.4.1c	7, 8	All	L	H	
Clock frequency	f _{CLK}	V _{CC} = 5 V	9	All	0	100	MHz
		V _{CC} = 4.5 V to 5.5 V	10, 11		0	60	
Pulse duration	t _w	V _{CC} = 5 V, CLK high,	9, 10, 11	All	7		ns
		V _{CC} = 5 V, CLK low			6		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, data before CLK ↑	t _{SU}	High, V _{CC} = 5.5 V	9	All	2		ns
			10, 11		2.5		
		Low, V _{CC} = 4.5 V	9, 10,11		2		
Hold time, data after CLK ↑	t _H	High, V _{CC} = 5.5 V	9,10, 11	All	2		ns
			9		2		
		Low, V _{CC} = 4.5 V	10, 11		2.5		
Maximum frequency	f _{MAX}	4/	9	All	100		MHz
		5/	10, 11		60		
CLK input to Q output timing	t _{PLH}	4/	9	All	3.2	8.5	ns
		5/	10, 11		3.2	10.5	
	t _{PHL}	4/	9		3.2	8.5	
		5/	10, 11		3.2	11	
Propagation delay time, $\overline{\text{OE}}$ input to Q output	t _{PZH}	4/	9	All	1.2	11.5	ns
		5/	10, 11		1.2	14	
	t _{PZL}	4/	9		1.2	7.5	
		5/	10, 11		1.2	10	
Propagation delay time, $\overline{\text{OE}}$ input to Q output	t _{PHZ}	4/	9	All	1.2	7	ns
		5/	10, 11		1.2	8	
	t _{PLZ}	4/	9		1.2	5.5	
		5/	10, 11		1.2	7.5	

1/ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

2/ I_{CCZ} is measured with $\overline{\text{OE}}$ at 4.5 V and all other inputs grounded.

3/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Function tests shall be performed in sequence as approved by the qualifying activity on qualified devices.

4/ For group A subgroup 9, V_{CC} = 5 V, C_L = 50 pF, and R_L = 500 Ω.

5/ For group A subgroups 10, 11, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, and R_L = 500 Ω.

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Device type	01
Case outlines	R, S, and 2
Terminal number	Terminal symbol
1	\overline{OE}
2	1 Q
3	1 D
4	2 D
5	2 Q
6	3 Q
7	3 D
8	4 D
9	4 Q
10	GND
11	CLK
12	5 Q
13	5 D
14	6 D
15	6 Q
16	7 Q
17	7 D
18	8 D
19	8 Q
20	V _{CC}

FIGURE 1. Terminal connections.

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

NOTE: Table applies to each flip flop.

FIGURE 2. Truth table.

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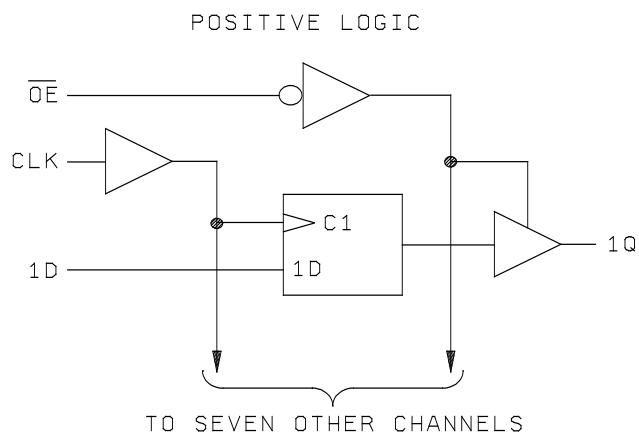
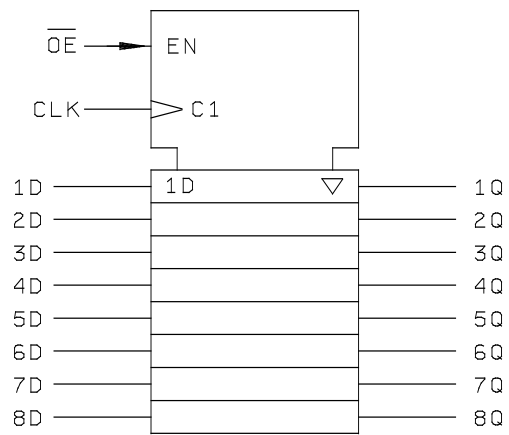


FIGURE 3. Block diagram.

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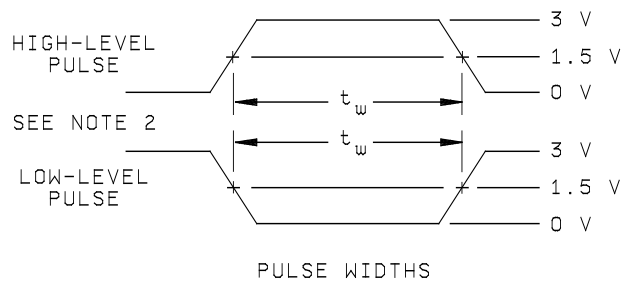
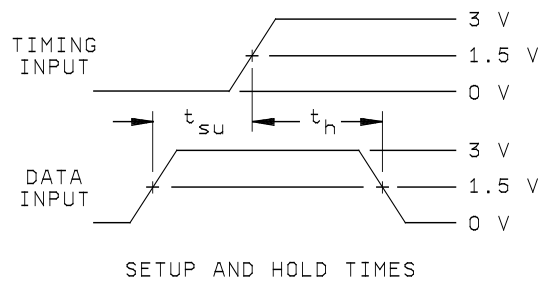
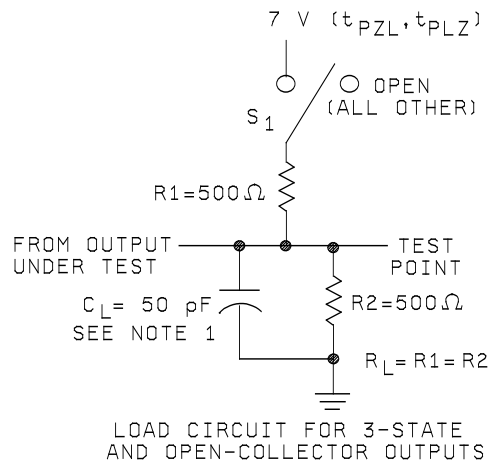


FIGURE 4. Timing diagram.

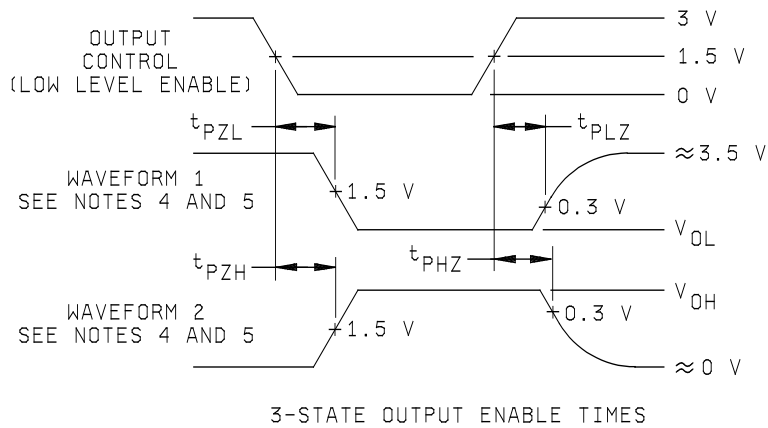
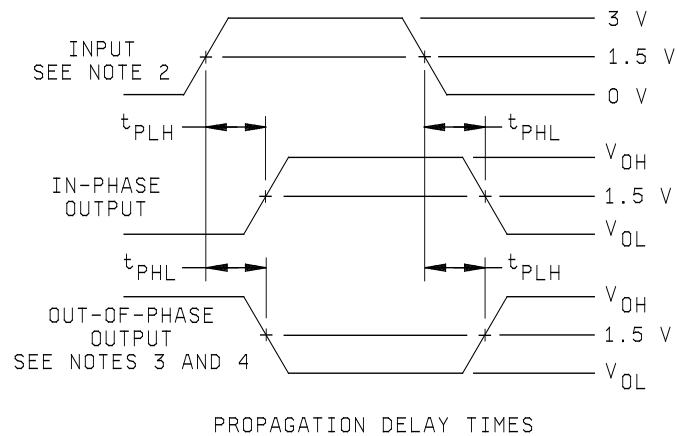
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NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics; PRR = 1 MHz, $t_R = t_F \leq 2.5$ ns, and duty cycle = 50 %.
3. When measuring propagation delay times of three-state outputs, switch S1 is open.
4. The outputs are measured one at a time with one transition per measurement.
5. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control

FIGURE 4. Timing diagram - continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

- 1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-12-07

Approved sources of supply for SMD 5962-97590 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military number
5962-9759001QRA	01295	SNJ54F374J	M38510/34105BRA
5962-9759001QSA	01295	SNJ54F374W	M38510/34105BSA
5962-9759001Q2A	01295	SNJ54F374FK	M38510/34105B2A

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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