REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. - gap	06-12-12	Raymond Monnin
B	Remove all class M references. Update drawing to current MIL-PRF-38535 requirements. - rdc	16-11-22	Charles Saffle
C	Update drawing to latest MIL-PRF-38535 requirements. - jt	21-10-15	James R. Eschmeyer

REV																				
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REV																				
SHEET																				

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
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DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

CHECKED BY
Tuan D. Nguyen

APPROVED BY
Raymond L. Monnin

DRAWING APPROVAL DATE
97-04-30

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY TTL, OCTAL BUFFERS W/ACTIVE LOW ENABLED 3-STATE INVERTED OUTPUTS, MONOLITHIC SILICON

AMSC N/A

REVISION LEVEL
C

SIZE	CAGE CODE	
A	**67268**	**5962-97585**

SHEET 1 OF 13

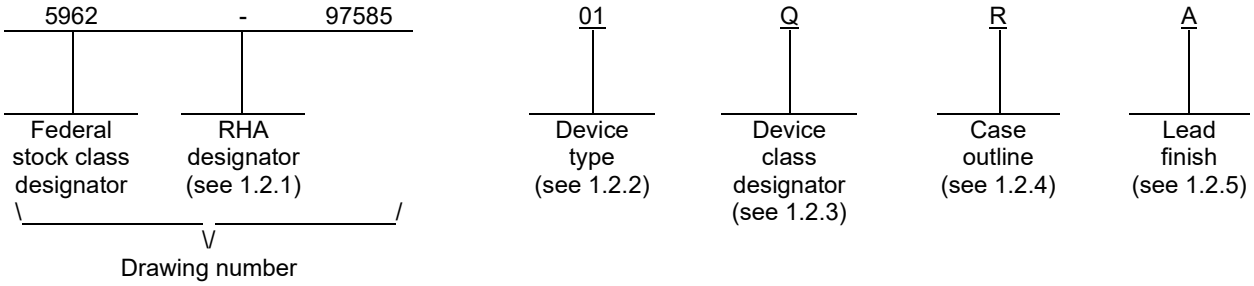
DSCC FORM 2233
APR 97

5962-E559-21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F240	Octal buffers w/active low enabled 3-state inverted outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line package
S	GDFP2-F20 or CDFP3-F20	20	Flat package
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to 7.0 V dc
Input voltage range (V_I)	-1.2 V dc to 7.0 V dc
Input current range	-30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage range applied to any output in the high state	-0.5 V to V_{CC}
Current into any output in the low state	96 mA
Operating free-air temperature range (T_A)	-55°C to +125°C
Maximum power dissipation (P_D)	71.5 mW
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	+2.0 V
Maximum low level input voltage (V_{IL})	+0.8 V
Input clamp current (I_{IK})	-18mA
Maximum high level output current (I_{OH})	-12 mA
Maximum low level output current (I_{OL})	+48 mA
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and waveforms. The test circuit and waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V 2/	I_{OH} = -3 mA	1, 2, 3	01	2.4		V
		V_{CC} = 4.5 V 2/	I_{OH} = -12 mA		01	2		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V 2/	I_{OL} = 48 mA	1, 2, 3	01		0.55	V
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V	I_I = -18 mA	1, 2, 3	01		-1.2	V
High level input current	I_{IH}	V_{CC} = 5.5 V	V_I = 2.7 V	1, 2, 3	01		20	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V	V_I = 0.5 V	1, 2, 3	01		-1	mA
Input current	I_I	V_{CC} = 5.5 V	V_I = 7 V	1, 2, 3	01		0.1	mA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V 3/	V_O = 0 V	1, 2, 3	01	-100	-225	mA
Supply current	I_{CCH}	V_{CC} = 5.5 V	Outputs high	1, 2, 3	01		29	mA
	I_{CCL}		Outputs low		01		75	
	I_{CCZ}		Outputs disabled		01		63	
Off-state output leakage current	I_{OZH}	V_{CC} = 5.5 V	V_O = 2.7 V	1, 2, 3	01		50	µA
	I_{OZL}	V_{CC} = 5.5 V	V_O = 0.5 V	1, 2, 3	01		-50	µA
Functional tests		See 4.4.1b, V_{CC} = 4.5 V, 5.5 V		7, 8	01			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, low-to-high level output, from any A to Y	t_{PLH}	4/ 5/	9	01	2.2	7	ns
			10, 11	01	2.2	9	
Propagation delay time, high-to-low level output, from any A to Y	t_{PHL}		9	01	1.2	4.7	ns
			10, 11	01	1.2	6	
Output enable time, high level output, $\overline{OE}$ to Y	t_{PZH}		9	01	1.2	5.2	ns
			10, 11	01	1.2	6.5	
Output enable time, low level output, $\overline{OE}$ to Y	t_{PZL}		9	01	3.2	9	ns
			10, 11	01	3.2	10.5	
Output disable time, high level output, $\overline{OE}$ to Y	t_{PHZ}		9	01	1.2	5.3	ns
			10, 11	01	1.2	6.5	
Output disable time, low level output, $\overline{OE}$ to Y	t_{PLZ}		9	01	1.2	8	ns
			10, 11	01	1.2	12.5	

1/ Unused inputs that do not directly control the pin under test must be put at +2.5 V or - 0.4 V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.
2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.
3/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and duration of the test condition shall not exceed one second.
4/ For group A subgroup 9, V_{CC} = 5 V, C_L = 50 pF, and R_L = 500 Ω.
5/ For group A subgroups 10, 11, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, and R_L = 500 Ω.

Case outlines	R, S, and 2
Terminal number	Terminal symbol
1	1 $\overline{OE}$
2	1A1
3	2Y4
4	1A2
5	2Y3
6	1A3
7	2Y2
8	1A4
9	2Y1
10	GND
11	2A1
12	1Y4
13	2A2
14	1Y3
15	2A3
16	1Y2
17	2A4
18	1Y1
19	2 $\overline{OE}$
20	V_{CC}

FIGURE 1. Terminal connections.

(each buffer)

Inputs		Output
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

H = High level voltage
L = Low level voltage
X = Irrelevant

FIGURE 2. Truth table.

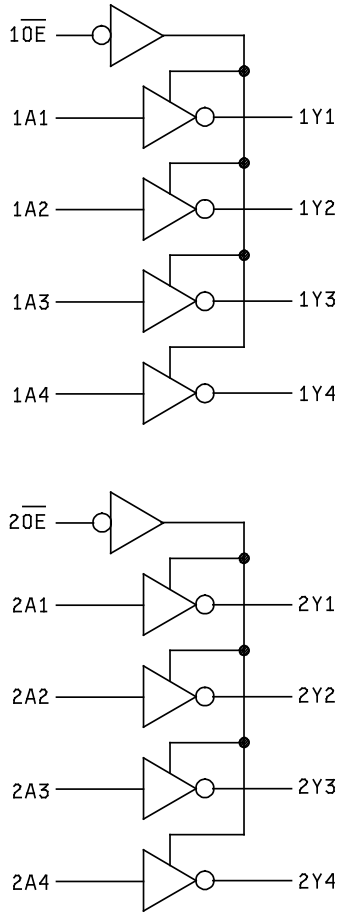
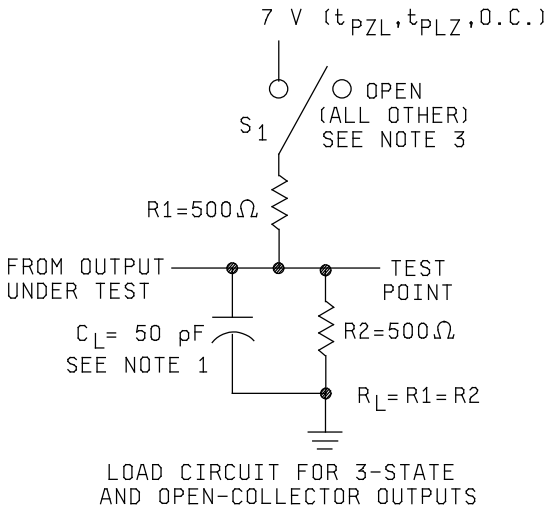


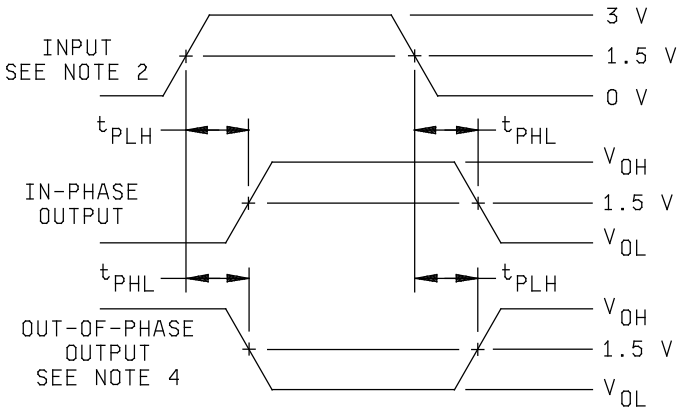
FIGURE 3. Logic diagram.



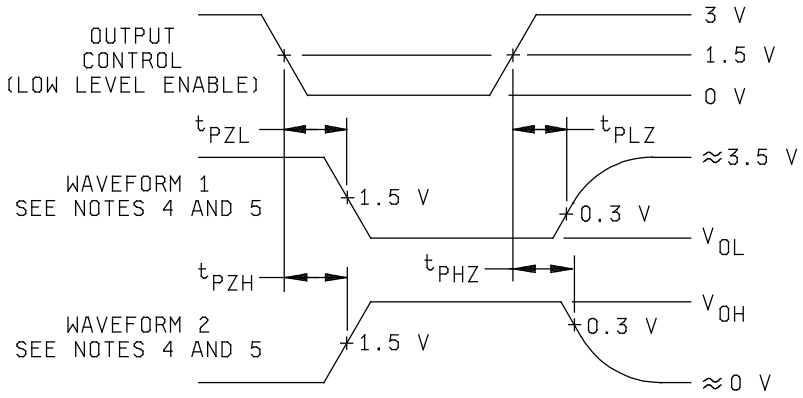
LOAD CIRCUIT FOR 3-STATE
AND OPEN-COLLECTOR OUTPUTS

See notes on next sheet.

FIGURE 4. Test circuit and timing waveforms.



PROPAGATION DELAY TIMES



3-STATE OUTPUT ENABLE TIMES

NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
3. When measuring propagation delay times of 3-state outputs, switch S1 is open.
4. The outputs are measured one at a time with one transition per measurement.
5. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 4. Test circuit and timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3,	1, 2, 3, 7, 8, 9
Group D end-point electrical parameters (see 4.4)	1, 2, 3,	1, 2, 3,
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-10-15

Approved sources of supply for SMD 5962-97585 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Military reference number
5962-9758501QRA	01295	SNJ54F240J	M38510/33201BRA
5962-9758501QSA	01295	SNJ54F240W	M38510/33201BSA
5962-9758501Q2A	01295	SNJ54F240FK	M38510/33201B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243