REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. – gt	03-02-06	R. Monnin
B	Update drawing as part of five year review. -rrp	12-04-23	C. SAFFLE

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								
REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

CHECKED BY
Raymond Monnin

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
97-08-13

MICROCIRCUIT, DIGITAL-LINEAR, DUAL, ASYNCHRONOUS COMMUNICATIONS ELEMENT WITH FIFO, MONOLITHIC SILICON

AMSC N/A

REVISION LEVEL
B

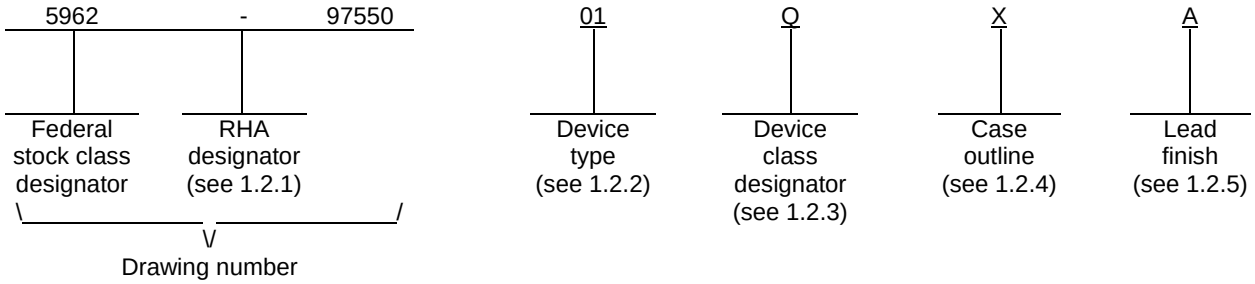
SIZE	CAGE CODE	
A	**67268**	**5962-97550**

SHEET 1 OF 26

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TL16C552AM	Dual asynchronous communications element with FIFO

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD})	-0.5 V dc to +7.0 V dc
Input voltage (V_{IN})	-0.5 V dc to +7.0 V dc
Continuous total power dissipation at 25°C	1689 mW 3/
Operating free air temperature range (T_A)	-55°C to +125°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	3°C/W
Thermal resistance, junction-to-air (θ_{JA})	74°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{DD})	4.75 V dc to 5.25 V dc
High-level input voltage range (V_{IH})	+2.0 V dc to V_{DD}
Low-level input voltage (V_{IL})	+0.0 V dc to +0.8 V
Clock frequency, (f_{clock})	16 MHz max
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ Above 25°C, derate at a factor of 13.5mW/°C.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime’s agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 10 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Types	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{DD} = 5.25 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -12 mA for PD0-PD7, I_{OH} = -4 mA for all other outputs 1/	1, 2, 3	All	2.4		V
Low-level output voltage	V_{OL}	V_{DD} = 5.25 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 12 mA for PD0-PD7, I_{OL} = 12 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$, I_{OL} = 4 mA for all other outputs	1, 2, 3	All		0.4	V
Input current	I_I	V_{DD} = 5.25 V, all other terminals floating 2/	1, 2, 3	All		±10	µA
High impedance output current	I_{OZ}	V_{DD} = 5.25 V, V_O = 0 V with chip de-selected or V_O = 5.25 V with chip and write-mode selected 1/	1, 2, 3	All		±20	µA
Dynamic supply current	I_{DD}	V_{DD} = 5.25 V, inputs at 0.8 V or 2.0 V, no loads on outputs, f_{CLK} = 8 MHz	1, 2, 3	All		50	mA
Clock Timing Requirements 3/							
Pulse duration, CLK↑	t_{w1}	see figure 3	9, 10, 11	All	31		ns
Pulse duration, CLK↓	t_{w2}	see figure 3	9, 10, 11	All	31		ns
Pulse duration, $\overline{RESET}$	t_{w3}	see figure 3	9, 10, 11	All	1000		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Read Cycle Timing Requirements 3/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Types	Limits		Unit
					Min	Max	
Pulse duration, $\overline{IOR}\downarrow$	t_{w4}	see figure 3	9, 10, 11	All	80		ns
Setup time, $\overline{CSx}$ valid before $\overline{IOR}\downarrow$ 4/	t_{su1}	see figure 3	9, 10, 11	All	15		ns
Setup time, A2-A0 valid before $\overline{IOR}\downarrow$ 4/	t_{su2}	see figure 3	9, 10, 11	All	15		ns
Hold time, A2-A0 valid after $\overline{IOR}\uparrow$ 4/	t_{h1}	see figure 3	9, 10, 11	All	20		ns
Hold time, $\overline{CSx}$ valid after $\overline{IOR}\uparrow$ 4/	t_{h2}	see figure 3	9, 10, 11	All	20		ns
Delay time, $t_{su2} + t_{w4} + t_{d2}$ 5/	t_{d1}	see figure 3	9, 10, 11	All	175		ns
Delay time, $\overline{IOR}\uparrow$ to $\overline{IOR}$ or $\overline{IOW}\downarrow$	t_{d2}	see figure 3	9, 10, 11	All	80		ns

Write Cycle Timing Requirements 3/

Pulse duration, $\overline{IOW}\downarrow$	t_{w5}	see figure 3	9, 10, 11	All	80		ns
Setup time, $\overline{CSx}$ valid before $\overline{IOW}\downarrow$ 4/	t_{su4}	see figure 3	9, 10, 11	All	15		ns
Setup time, A2-A0 valid before $\overline{IOW}\downarrow$ 4/	t_{su5}	see figure 3	9, 10, 11	All	15		ns
Setup time, DB0-DB7 valid before $\overline{IOW}\uparrow$	t_{su6}	see figure 3	9, 10, 11	All	15		ns
Hold time, A2-A0 valid after $\overline{IOW}\uparrow$ 4/	t_{h3}	see figure 3	9, 10, 11	All	20		ns
Hold time, $\overline{CSx}$ valid after $\overline{IOW}\uparrow$ 4/	t_{h4}	see figure 3	9, 10, 11	All	20		ns
Hold time, DB0-DB7 valid after $\overline{IOW}\uparrow$	t_{h5}	see figure 3	9, 10, 11	All	15		ns
Delay time, $t_{su5} + t_{w5} + t_{d4}$	t_{d3}	see figure 3	9, 10, 11	All	175		ns
Delay time, $\overline{IOW}\uparrow$ to $\overline{IOW}$ or $\overline{IOR}\downarrow$	t_{d4}	see figure 3	9, 10, 11	All	80		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.
Read Cycle Switching Characteristics 3/ 6/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Types	Limits		Unit
					Min	Max	
Propagation delay time, $\overline{IOR}$ ↓ to BDO↑ or $\overline{IOR}$ ↑ to BDO↓	t_{pd1}	C_L = 100 pF see figure 3	9, 10, 11	All		60	ns
Enable time, $\overline{IOR}$ ↓ to DB0-DB7 valid	t_{en}	C_L = 100 pF see figure 3	9, 10, 11	All		60	ns
Disable time, $\overline{IOR}$ ↑ to DB0-DB7 released	t_{dis}	C_L = 100 pF see figure 3	9, 10, 11	All		60	ns
Transmitter Switching Characteristics 3/							
Delay time, interrupt THRE↓ to SOUT↓ 7/	t_{d5}	see figure 3	9, 10, 11	All	8	24	RCLK cycles
Delay time, SOUT↓ at start to interrupt THRE↑ 8/	t_{d6}	see figure 3	9, 10, 11	All	8	9	RCLK cycles
Delay time, $\overline{IOW}$ (WR THR)↑ to interrupt THRE↑ 8/	t_{d7}	see figure 3	9, 10, 11	All	16	32	RCLK cycles
Delay time, SOUT↓ at start to $\overline{TXRDY}$ ↓	t_{d8}	C_L = 100 pF see figure 3	9, 10, 11	All		8	RCLK cycles
Propagation delay time, $\overline{IOW}$ (WR THR)↓ to interrupt THRE↓	t_{pd2}	C_L = 100 pF see figure 3	9, 10, 11	All		140	ns
Propagation delay time, $\overline{IOR}$ (RD IIR)↑ to interrupt THRE↓	t_{pd4}	C_L = 100 pF see figure 3	9, 10, 11	All		140	ns
Propagation delay time, $\overline{IOW}$ (WR THR)↑ to $\overline{TXRDY}$ ↑	t_{pd5}	C_L = 100 pF see figure 3	9, 10, 11	All		195	ns

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - Continued
Receiver Switching Characteristics 3/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Types	Limits		Unit
					Min	Max	
Delay time, from stop to INT↑ 9/	t_{d9}	see figure 3	9, 10, 11	All		1	RCLK cycles
Propagation delay time, RCLK↑ to sample CLK↑	t_{pd6}	see figure 3	9, 10, 11	All		100	ns
Propagation delay time, $\overline{IOR}$ (RD RBR / RD LSR)↓ to reset interrupt↓	t_{pd7}	C_L = 100 pF see figure 3	9, 10, 11	All		150	ns
Propagation delay time, $\overline{IOR}$ (RD RBR)↓ to $\overline{RXRDY}$ ↑	t_{pd8}	see figure 3	9, 10, 11	All		150	ns

Modem Control Switching Characteristics 3/

Propagation delay time, $\overline{IOW}$ (WR MCR)↑ to $\overline{RTS}$ or $\overline{DTR}$ ↓↑	t_{pd9}	C_L = 100 pF see figure 3	9, 10, 11	All		100	ns
Propagation delay time, modem input ($\overline{CTS}$, $\overline{DSR}$)↓↑ to interrupt↑	t_{pd10}	C_L = 100 pF see figure 3	9, 10, 11	All		170	ns
Propagation delay time, $\overline{IOR}$ (RD MSR)↑ to interrupt↓	t_{pd11}	C_L = 100 pF see figure 3	9, 10, 11	All		140	ns
Propagation delay time, RI↑ to interrupt↑	t_{pd12}	C_L = 100 pF see figure 3	9, 10, 11	All		170	ns

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - Continued
Parallel Port Timing Requirements 3/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Types	Limits		Unit
					Min	Max	
Setup time, data valid before $\overline{STB}$ ↓	t_{su7}	see figure 3	9, 10, 11	All	1		µs
Hold time, data valid after $\overline{STB}$ ↑	t_{h6}	see figure 3	9, 10, 11	All	1		µs
Pulse duration, $\overline{STB}$ ↓	t_{w6}	see figure 3	9, 10, 11	All	1		µs
Delay time, BUSY↑ to $\overline{ACK}$ ↓ 10/	t_{d10}	see figure 3	9, 10, 11	All			
Delay time, BUSY↓ to $\overline{ACK}$ ↓ 10/	t_{d11}	see figure 3	9, 10, 11	All			
Pulse duration, BUSY↑ 10/	t_{w7}	see figure 3	9, 10, 11	All			
Pulse duration, $\overline{ACK}$ ↓ 10/	t_{w8}	see figure 3	9, 10, 11	All			
Delay time, BUSY↑ after STB↑ 10/	t_{d12}	see figure 3	9, 10, 11	All			
Delay time, INT2↓ after $\overline{ACK}$ ↓	t_{d13}	C_L = 15 pF see figure 3	9, 10, 11	All		22	ns
Delay time, INT2↑ after $\overline{ACK}$ ↑	t_{d14}	C_L = 15 pF see figure 3	9, 10, 11	All		20	ns
Delay time, INT2↑ after $\overline{ACK}$ ↑	t_{d15}	C_L = 15 pF see figure 3	9, 10, 11	All		24	ns
Delay time, INT2↓ after $\overline{IOR}$ ↑	t_{d16}	C_L = 15 pF see figure 3	9, 10, 11	All		25	ns

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - Continued

1/ Excluding $\overline{STB}$, $\overline{INIT}$, $\overline{AFD}$, and $\overline{SLIN}$ pins because these terminals are open-drain pins with an internal pull-up resistor to V_{DD} of approximately 10 kΩ.

2/ Excluding the TRI pin because this input terminal contains an internal pull-down resistor that is approximately 5 kΩ.

3/ These parameters are guaranteed by design but not tested except for t_{pd1}, which is tested at 25°C, 125°C, and -55°C.

4/ The internal address strobe is always active during this test.

5/ In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (interrupt identification register and line status register).

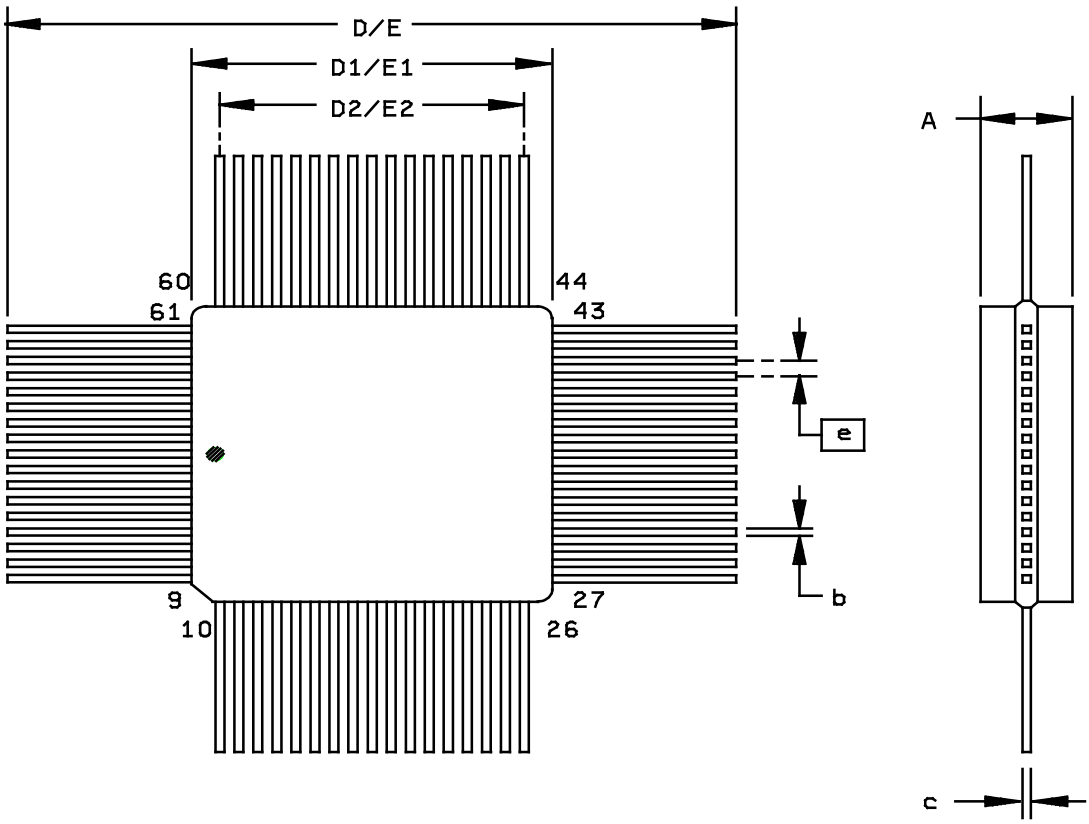
6/ V_{OL}, V_{OH}, and the external loading determine the charge and discharge time.

7/ The acronym THRE stands for transmitter holding register empty.

8/ When the transmitter interrupt delay is active, this delay is lengthened by one character time minus the last stop bit time.

9/ The receiver data available indicator, the overrun error indicator, the trigger level interrupts, and the active $\overline{RXRDY}$ indicator are delayed 3 RCLK cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) are delayed 3 RCLK cycles. These indicators are updated immediately for any further bytes received after RDRBR goes active. There are 8 RCLK cycle delays for trigger change level interrupts.

10/ Limits for these parameters are defined by the printer being used and are not part of this specification.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.134	0.154	3.404	3.912
b	0.008	0.013	0.203	0.330
c	0.005	0.007	0.127	0.178
D/E	1.300	1.500	33.02	38.10
D1/E1	0.485	0.500	12.32	12.70
D2/E2	0.400 TYP		10.16 TYP	
e	0.025 BSC		0.635 BSC	

FIGURE 1. Case outline.

Device Type 01			
Case Outline X			
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	PMED	35	A0
2	TRI	36	$\overline{IOW}$
3	$\overline{CS1}$	37	$\overline{IOR}$
4	CLK	38	$\overline{CS2}$
5	$\overline{DSR1}$	39	$\overline{RESET}$
6	$\overline{RI1}$	40	V_{DD}
7	GND	41	SIN0
8	$\overline{DCD1}$	42	$\overline{TXRDY1}$
9	$\overline{RXRDY0}$	43	$\overline{ENIRQ}$
10	SOUT1	44	BD0
11	$\overline{DTR1}$	45	INT0
12	$\overline{RTS1}$	46	PD7
13	$\overline{CTS1}$	47	PD6
14	DB0	48	PD5
15	DB1	49	PD4
16	DB2	50	PD3
17	DB3	51	PD2
18	DB4	52	PD1
19	DB5	53	PD0
20	DB6	54	GND
21	DB7	55	$\overline{STB}$
22	$\overline{TXRDY0}$	56	$\overline{AFD}$
23	V_{DD}	57	$\overline{INIT}$
24	$\overline{RTS0}$	58	$\overline{SLIN}$
25	$\overline{DTR0}$	59	INT2
26	SOUT0	60	INT1
27	GND	61	$\overline{RXRDY1}$
27	$\overline{CTS0}$	62	SIN1
29	$\overline{DCD0}$	63	$\overline{ERR}$
30	$\overline{RI0}$	64	V_{DD}
31	$\overline{DSR0}$	65	SLCT
32	$\overline{CS0}$	66	BUSY
33	A2	67	PE
34	A1	68	$\overline{ACK}$

FIGURE 2. Terminal connections.

Terminal Name	Terminal No.	I/O	Description
$\overline{ACK}$	68	I	Line printer acknowledge. $\overline{ACK}$ goes low to indicate a successful data transfer has taken place. $\overline{ACK}$ generates a printer port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Line printer autofeed. $\overline{AFD}$ is an open-drain line that provides the printer with an active-low signal when continuous form paper is to be autofed to the printer. $\overline{AFD}$ has an internal pull-up resistor to V_{DD} of approximately 10 kΩ.
An (n = 0 to 3)	35,34,33	I	Address. The address lines A0-A2 select the internal registers during CPU bus operations.
BDO	44	O	Bus buffer. BDO is an active-high output and is asserted when either serial channel or the parallel port is read. BDO controls the system bus driver.
BUSY	66	I	Line printer busy. BUSY is an input line from the printer that goes high when the printer is not ready to accept data.
CLK	4	I	Clock. CLK is the external clock input to the baud rate divisor of each ACE.
$\overline{CSn}$ (n = 0 to 2)	32,3,38	I	Chip select. Each $\overline{CSn}$ input acts as an enable for the write and read signals for serial channels 1 ($\overline{CS0}$) and 2 ($\overline{CS1}$). $\overline{CS2}$ enable the signals to the printer port.
$\overline{CTSn}$ (n = 0 and 1)	28,13	I	Clear to send. The logical state of each $\overline{CTSn}$ terminal is reflected in the CTS bit of the modem status register (CTS is bit 4 of the modem status register, written as MSR4) of each ACE. A change of state in either $\overline{CTS}$ terminal since the previous reading of the associated MSR causes the setting of Δ CTS (MSR0) of each modem status register.
DBn (n = 0 to 7)	14-21	I/O	Data bits DB0 - DB7. The data bus provides eight I/O lines with 3-state outputs for the transfer of data, control, and status information between the TL16C552A and the CPU. These lines are normally in the high-impedance state except during read operations. DB0 is the least significant bit (LSB) and is the first serial bit to be received or transmitted.
$\overline{DCDn}$ (n = 0 and 1)	29,8	I	Data carrier detect. $\overline{DCD}$ is a modem input. Its condition can be tested by the CPU by reading MSR7 (DCD) of the modem status registers. MSR3 (ΔDCD) of the modem status register indicates whether $\overline{DCD}$ has changed states since the previous reading of the MSR. $\overline{DCD}$ has no effect on the receiver.
$\overline{DSRn}$ (n = 0 and 1)	31,5	I	Data set ready. The logical state of the $\overline{DSRn}$ terminals is reflected in the MSR5 of its associated modem status register. ΔDSR (MSR1) indicates whether the associated $\overline{DSRn}$ terminal has changed states since the previous reading of the MSR.
$\overline{DTRn}$ (n = 0 and 1)	25,11	O	Data terminal ready. Each $\overline{DTRn}$ can be set low by setting MCR0, modem control register bit 0 of its associated ACE. $\overline{DTRn}$ is cleared (high) by clearing the DTR bit (MCR0) or whenever a reset occurs. When active (low), $\overline{DTRn}$ indicates that its ACE is ready to receive data.

FIGURE 2. Terminal connections - continued.

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{ENIRQ}}$	43	I	Parallel port interrupt source mode selection. When $\overline{\text{ENIRQ}}$ is low, the AT mode of interrupts is enabled. In AT mode, INT2 is intentionally connected to $\overline{\text{ACK}}$. When $\overline{\text{ENIRQ}}$ is tied high, the PS-2 mode of interrupt is enabled and INT2 is internally tied to the inverse of the $\overline{\text{PRINT}}$ bit in the line printer status register. INT2 is latched high on the rising edge of $\overline{\text{ACK}}$. INT2 is held until the status register is read, which then clears the $\overline{\text{PRINT}}$ status bit and INT2.
$\overline{\text{ERR}}$	63	I	Line printer error. $\overline{\text{ERR}}$ is an input line from the printer. The printer reports an error by holding $\overline{\text{ERR}}$ low during the error condition.
GND	1,27,54		Ground (0 V). All terminals must be tied to GND for proper operation.
$\overline{\text{INIT}}$	57	I/O	Line printer initialize. $\overline{\text{INIT}}$ is an open-drain that provides the printer with an active-low signal that allows the printer initialization routine to be started. $\overline{\text{INIT}}$ has an internal pull-up resistor to V_{DD} of approximately 10 kΩ.
INTn (n = 0 and 1)	45,60	O	External serial channel interrupt. Each serial channel interrupt 3-state output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the interrupt enable register of its associated channel: receiver error flag, received data available, transmitter holding register empty, and modem status. The interrupt is cleared on appropriate service. Upon reset, the interrupt output is in the high-impedance state.
INT2	59	O	Printer port interrupt. INT2 is an active-high, 3-state output generated by the positive transition of $\overline{\text{ACK}}$. INT2 is enabled by bit 4 of the write control register. Upon reset, INT2 is in the high-impedance state. Its mode is also controlled by $\overline{\text{ENIRQ}}$.
$\overline{\text{IOR}}$	37	I	Input/output read strobe. $\overline{\text{IOR}}$ is an active-low input that enables the selected channel to output data to the data bus (DB0-DB7). The data output depends on the register selected by the address inputs A0, A1, A2, and chip select. Chip select 0 ($\overline{\text{CS0}}$) selects ACE #1, chip select 1 ($\overline{\text{CS1}}$) selects ACE #2, and chip select 2 ($\overline{\text{CS2}}$) selects the printer port.
$\overline{\text{IOW}}$	36	I	Input/output write strobe. $\overline{\text{IOW}}$ is an active-low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends on the register selected by the address inputs A0, A1, A2, and chip selects $\overline{\text{CS0}}$, $\overline{\text{CS1}}$, and $\overline{\text{CS2}}$.
PDn (n = 0 to 7)	53-46	I/O	Parallel data bits (0-7). PD0-PD7 provide a byte wide input or output port to the system.
PE	67	I	Line printer paper empty. PE is an input line from the printer that goes high when the printer runs out of paper.
PEMD	1	I	Printer enhancement mode. When low, PEMD enables the write data register to the PD0 - PD7 lines. A high on PEMD allows direction control of the PD0 - PD7 port by the DIR bit in the control register. PEMD is usually tied low for the printer operation.

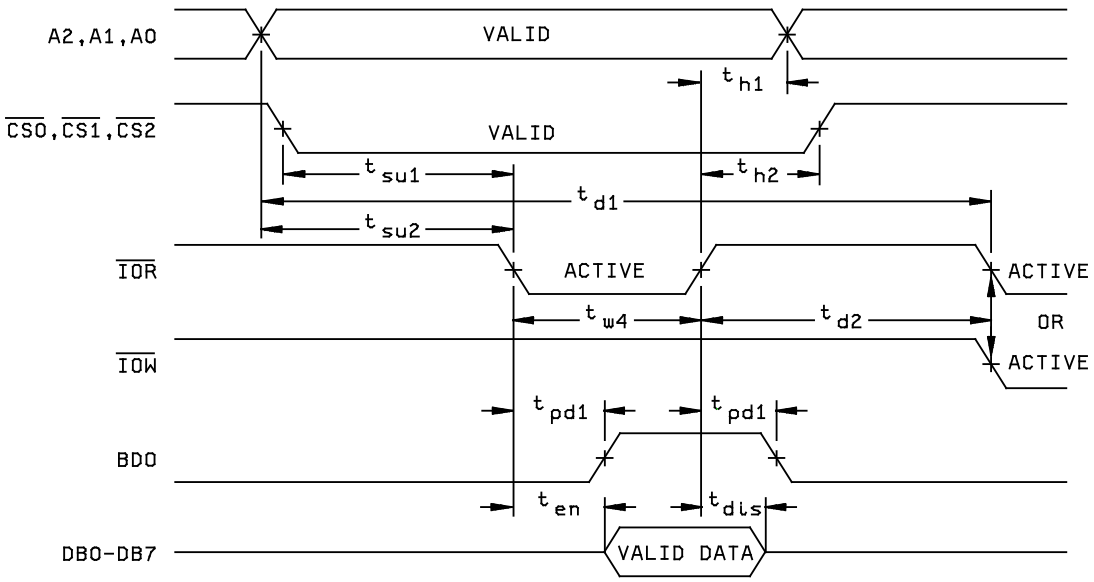
FIGURE 2. Terminal connections - continued.

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{RESET}}$	39	I	$\overline{\text{RESET}}$. When low, $\overline{\text{RESET}}$ forces the TL16C552A into an idle mode in which all serial data activities are suspended. The modem control register along with its associated outputs are cleared. The line status register is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in the idle state until programmed to resume serial data activities. $\overline{\text{RESET}}$ has a hysteresis level of typically 400 mV.
$\overline{\text{RTS}}$n (n = 0 and 1)	24,12	O	Request to send. The $\overline{\text{RTS}}$ outputs are set low by setting MCR1 of its UARTs modem control register. Both $\overline{\text{RTS}}$ terminals are reset high by $\overline{\text{RESET}}$. A low on $\overline{\text{RTS}}$ indicates that its ACE has data ready to transmit. In half-duplex operations, $\overline{\text{RTS}}$ controls the direction of the line.
$\overline{\text{RXRDY}}$n (n = 0 and 1)	9,61	O	Receiver ready. Receiver direct memory access (DMA) signaling is also available through this output. One of two types of DMA signaling can be selected using FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. For signal transfer DMA (a transfer is made between CPU bus cycles), Mode 0 is used. Multiple transfers are made continuously until the receiver FIFO has been emptied are supported by mode 1. Mode 0. $\overline{\text{RXRDY}}$ is active (low) when in the FIFO mode (FCR0=1, FCR3 = 0) or when in the TL16C450 mode (FCR0 = 0) and the receiver FIFO or receiver holding register contain at least one character. When there are no more characters in the FIFO or holding registers, $\overline{\text{RXRDY}}$ goes inactive (high). Mode 1. $\overline{\text{RXRDY}}$ goes active (low) in the FIFO mode (FCR0 = 1) when FCR3 = 1 and the time-out or trigger levels have been reached. $\overline{\text{RXRDY}}$ goes inactive (high) when the FIFO or holding register is empty.
$\overline{\text{RI}}$n (n = 0 and 1)	30,6	I	Ring indicator. The $\overline{\text{RI}}$ signal is a modem control input. Its condition is tested by reading MSR6 (RI) of each ACE. The modem status register output TERI (MSR2) indicates whether $\overline{\text{RI}}$ has changed from high to low since the previous reading of the modem status register.
SINn (n = 0 and 1)	41,62	I	Serial data. SIN0 and SIN1 move information from the communication line or modem to the receiver circuits. Mark is a high state and space is a low state. Data on serial data inputs is disabled when operating in the loop mode.
SLCT	65	I	Line printer select. SLCT is an input line from the printer that goes high when the printer is selected.
$\overline{\text{SLIN}}$	58	I/O	Line printer select. $\overline{\text{SLIN}}$ is an open-drain I/O that selects the printer when active (low). $\overline{\text{SLIN}}$ has an internal pull-up resistor to V_{DD} of approximately 10 kΩ.
SOUTn (n = 0 and 1)	26,10	O	Serial data outputs. SOUT0 and SOUT1 are the serial data outputs from the ACE transmitter circuitry. A mark is a high state and a space is a low state. Each SOUT is held in the mark condition when the transmitter is disabled ($\overline{\text{RESET}}$ is asserted low) the transmitter register is empty, or when in the loop mode.

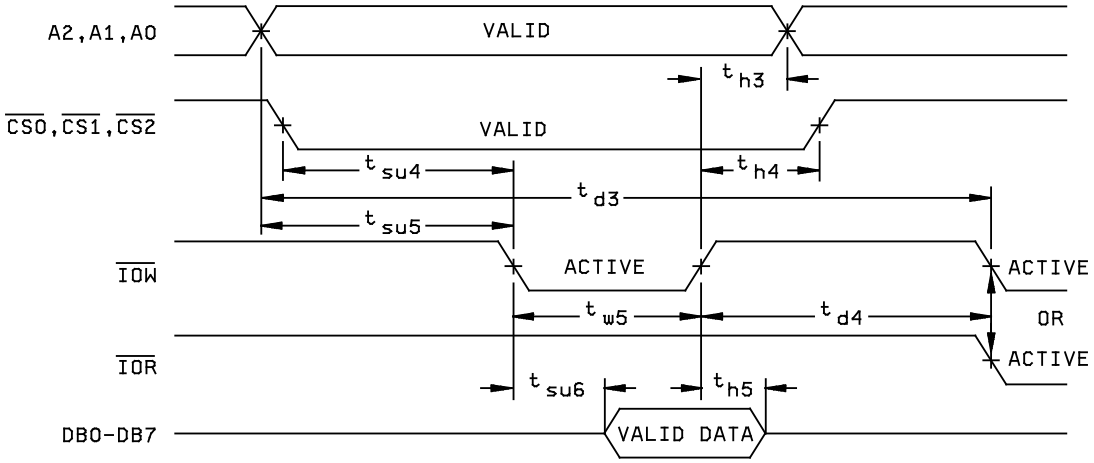
FIGURE 2. Terminal connections - continued.

$\overline{STB}$	55	I/O	Line printer strobe. STB provides communication between the TL16C552A and the printer. When $\overline{STB}$ is active (low), it provides the printer with a signal to latch the data currently on the printer port. $\overline{STB}$ has an internal pull-up resistor to V_{DD} of approximately 10 kΩ.
TRI	2	I	3-state output control input. TRI controls the 3-state control of all I/O and output terminals. When TRI is asserted, all I/Os and outputs are in the high-impedance state allowing board level testers to drive the outputs without overdriving internal buffers. TRI is level sensitive and is pulled down with an internal resistor that is approximately 5 kΩ.
$\overline{TXRDYn}$ (n=0 or 1)	22, 42	O	Transmitter ready. Two types of DMA signaling are available. Either can be selected using FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. Single-transfer DMA a transfer is made between CPU bus cycles) is supported by mode 0. Multiple transfers that are made continuously until the transmitter FIFO has been filled are supported by mode 1. Mode 0. When in the FIFO mode (FCR= 1, FCR3 = 0) or in the TL16C450 mode (FCR = 0) and there are no characters in the transmitter holding register or transmitter FIFO, $\overline{TXRDYn}$ is active (low). Once $\overline{TXRDYn}$ is activated (low), it goes inactive after the first character is loaded into the holding register of the transmitter FIFO. Mode 1. $\overline{TXRDY}$ goes active (low) when in the FIFO mode (FCR0 = 1) when FCR3 = 1 and there are no characters in the transmitter FIFO. When the transmitter FIFO is completely full, $\overline{TXRDY}$ goes inactive (high).
V_{DD}	23,40,64		Power supply. The V_{DD} requirement is 5 V ± 5%.

FIGURE 2. Terminal connections - continued.

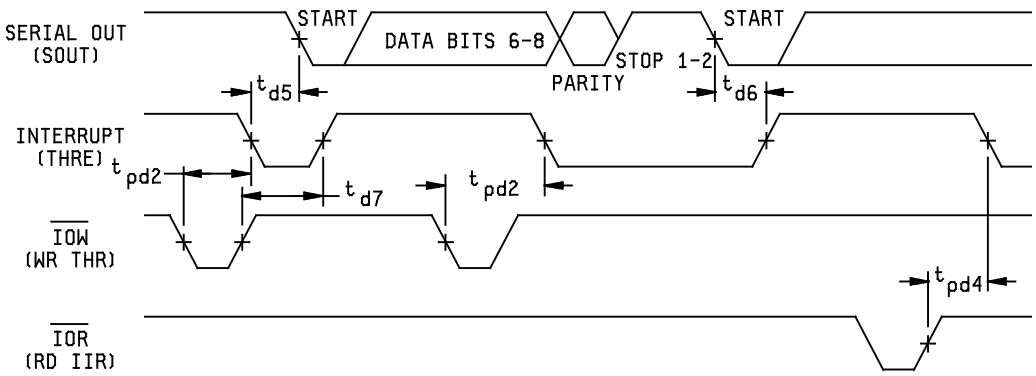


READ CYCLE TIMING WAVEFORM

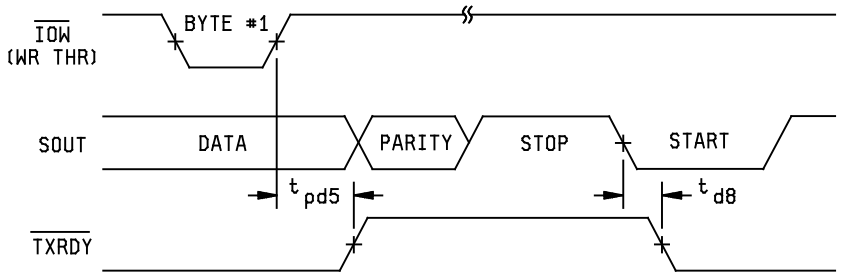


WRITE CYCLE TIMING WAVEFORM

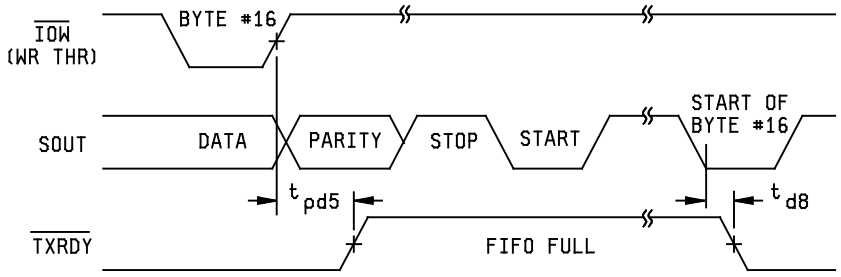
FIGURE 3. Timing waveforms.



TRANSMITTER TIMING WAVEFORM

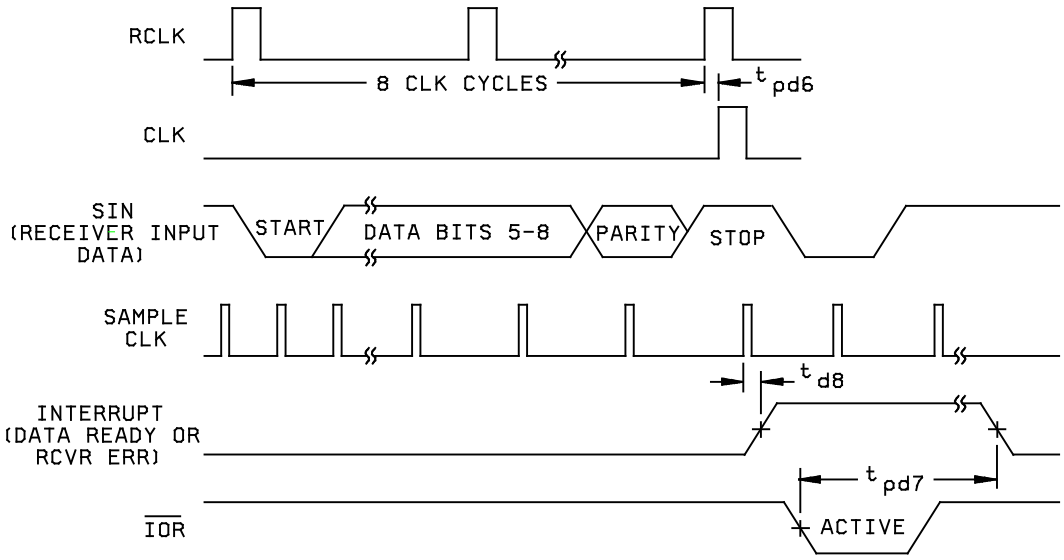


TRANSMITTER READY MODE 0 TIMING WAVEFORM

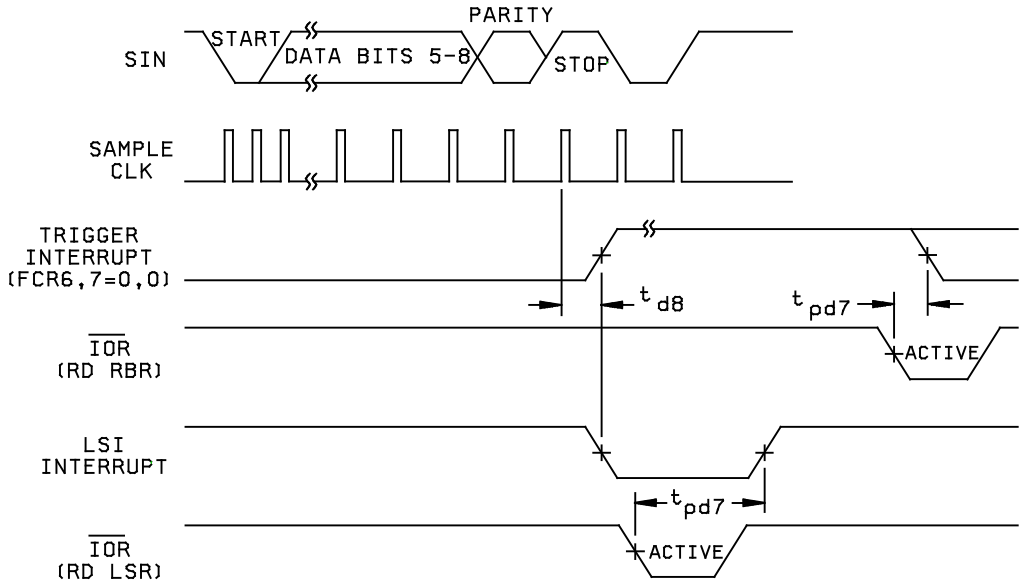


TRANSMITTER READY MODE 1 TIMING WAVEFORM

FIGURE 3. Timing waveforms - continued.

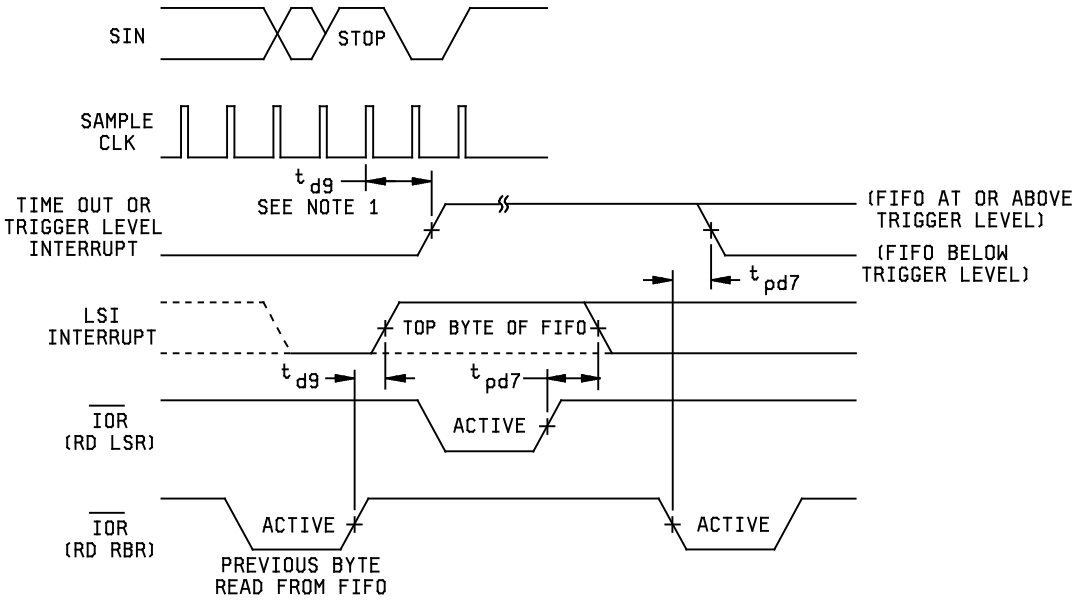


RECEIVER TIMING WAVEFORM

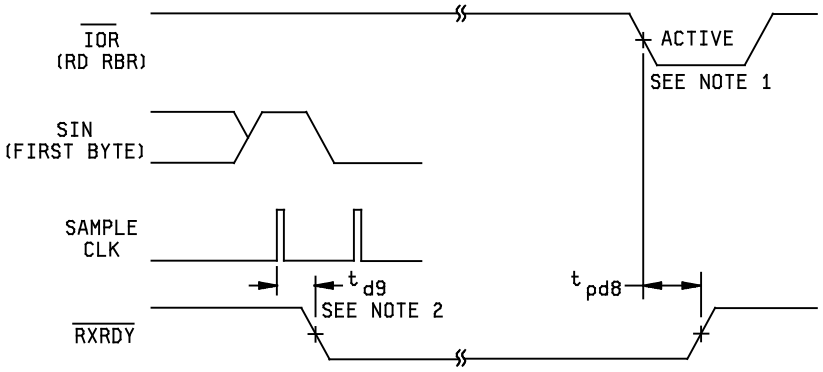


RECEIVER FIFO FIRST BYTE (SETS RDR) WAVEFORMS

FIGURE 3. Timing waveforms - continued.



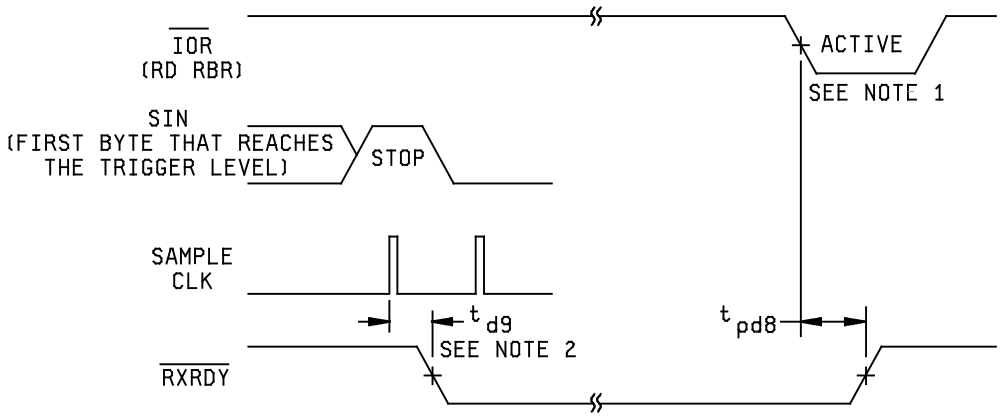
RECEIVER FIFO AFTER FIRST BYTE (AFTER RDR SET) WAVEFORM



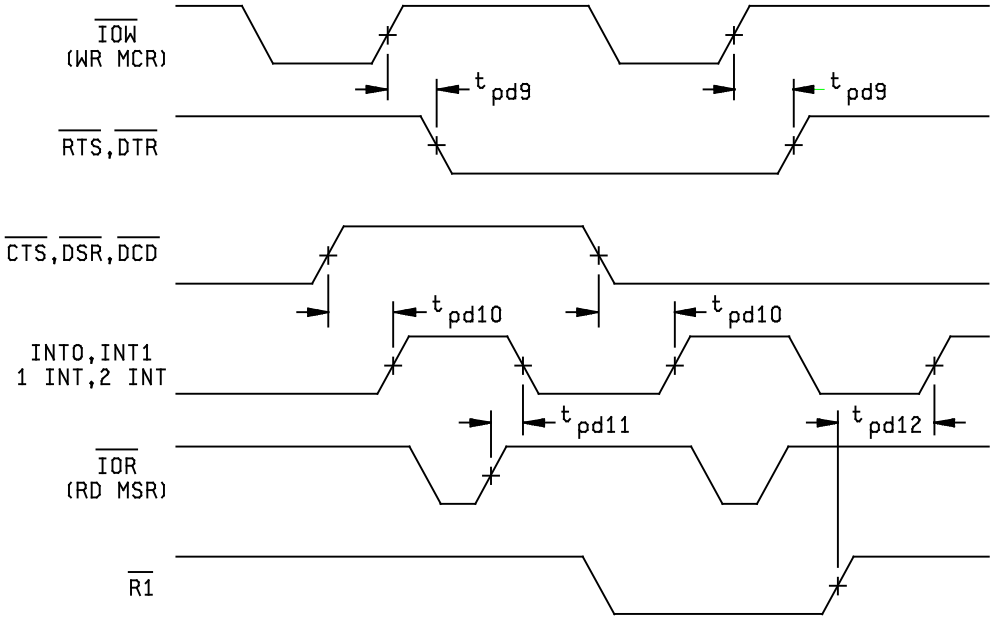
RECEIVER READY MODE 0 WAVEFORM

NOTES: 1. This is the reading of the last byte in the FIFO.
2. If FCRO = 1, t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

FIGURE 3. Timing waveforms - continued.



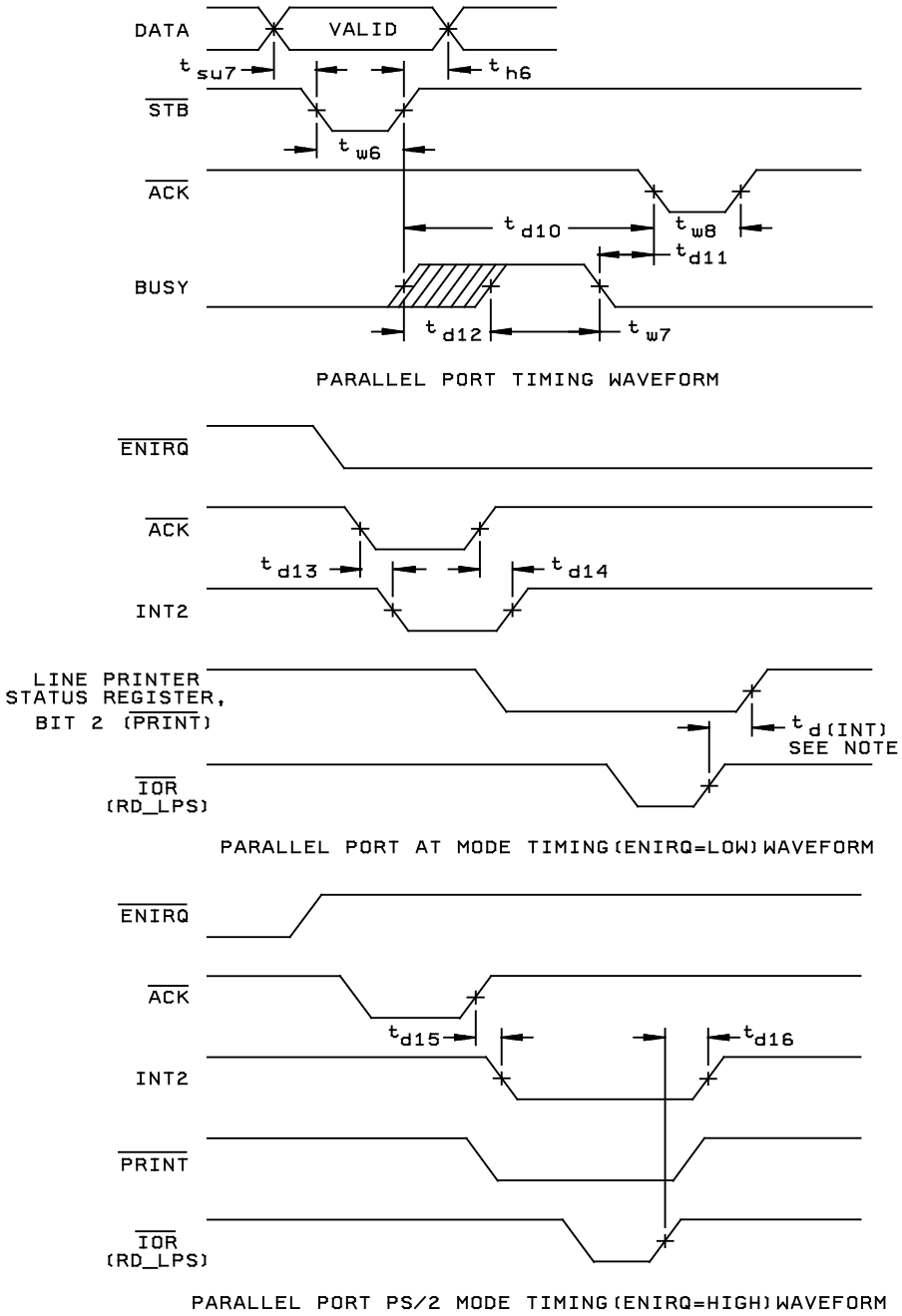
RECEIVER READY MODE 1 WAVEFORM



MODEM CONTROL TIMING WAVEFORM

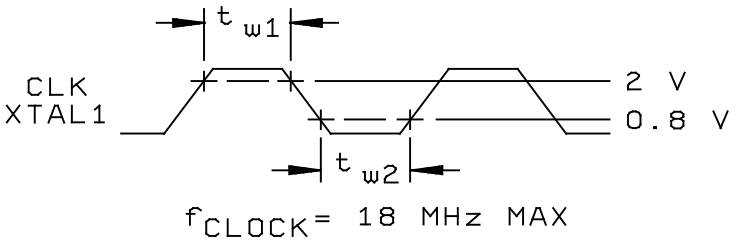
NOTES: 1. This is the reading of the last byte in the FIFO.
2. If FCRO = 1, t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

FIGURE 3. Timing waveforms - continued.



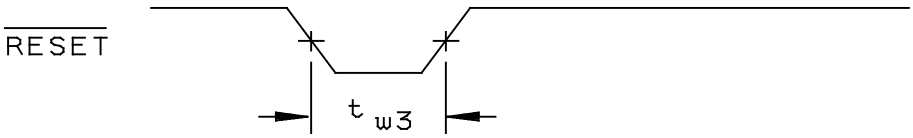
NOTES: A timing value is not provided for $t_{d(int)}$ since the line printer status register, bit 2 ($\overline{\text{PRINT}}$) is an internal signal.

FIGURE 3. Timing waveforms - continued.



f_{CLOCK} = 18 MHz MAX

CLK VOLTAGE WAVEFORM



$\overline{\text{RESET}}$ VOLTAGE WAVEFORM

FIGURE 3. Timing waveforms – continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3, 1/ 9,10,11	1,2,3, 1/ 9,10,11	1,2,3, 1/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,9,10,11	1,2,3, 9,10,11	1,2,3,9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-04-23

Approved sources of supply for SMD 5962-97550 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9755001QXA	01295	TLC16C552AMHVB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.