REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add truth table and delete 1.5. Make changes to 4.4.1b and 4.4.1c. Replace reference to MIL-STD-973 with reference to MIL-PRF-38535. - ro	06-05-01	R. Monnin
B	Remove class M references. Update drawing to current MIL-PRF-38535 requirements. - jt	16-02-05	Charles F. Saffle
C	Update drawing to latest MIL-PRF-38535 requirements. - jt	20-12-02	James R. Eschmeyer

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
97-05-30

REVISION LEVEL
C

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, BIPOLAR, SYNCHRONOUS 4-BIT COUNTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-97548**

SHEET 1 OF 14

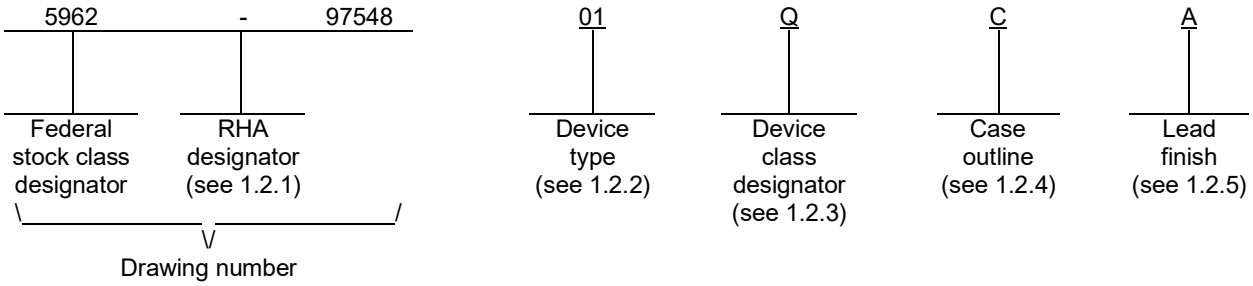
DSCC FORM 2233
APR 97

5962-E038-21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54163	Synchronous 4-bit counter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Leadless square chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage (V_{IN})	-0.5 V dc to +5.5 V dc
Interemitter voltage 2/	5.5 V
Operating free air temperature range	-55°C to +125°C
Maximum power dissipation (P_D)	500 mW
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175 °C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High-level output current (I_{OH})	-800 μA max
Low-level output current (I_{OL})	16 mA max
Clock frequency, (f_{clock})	25 MHz max
Width of clock pulse, t_w(clock)	25 ns min
Width of clear pulse, t_w(clear)	20 ns min
Setup time, t_{su}, from data inputs A, B, C, D to CLK input 3/	20 ns min
Setup time, t_{su}, from $\overline{ENP}$ to CLK input 3/	20 ns min
Setup time, t_{su}, from $\overline{LOAD}$ to CLK input 3/	25 ns min
Setup time, t_{su}, from $\overline{CLR}$ to CLK input 3/	20 ns min
Hold time at any input, t_h	0 ns min
Operating free-air temperature range (T_A)	-55 °C to +125 °C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ This is the voltage between two emitters of a multiple-emitter transistor.
3/ The waveforms on t_{su} are on figure 3.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein .

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level input voltage	V_{IH}			1, 2, 3	01	2		V
Low-level input voltage	V_{IL}			1, 2, 3	01		0.8	V
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_I = -12 mA		1, 2, 3	01		-1.5	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = -800 µA		1, 2, 3	01	2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		1, 2, 3	01		0.4	V
Input current at maximum input voltage	I_I	V_{CC} = 5.5 V, V_I = 5.5 V		1, 2, 3	01		1	mA
High-level input current	I_{IH}	V_{CC} = 5.5 V,	CLK or ENT	1, 2, 3	01		80	µA
		V_I = 2.4 V	Other inputs	1, 2, 3			40	
Low-level input current	I_{IL}	V_{CC} = 5.5 V,	CLK or ENT	1, 2, 3	01		-3.2	mA
		V_I = 0.4 V	Other inputs	1, 2, 3			-1.6	
Short-circuit output current	I_{OS} 1/	V_{CC} = 5.5 V		1, 2, 3	01	-20	-57	mA
Supply current, all outputs high	I_{CCH} 2/	V_{CC} = 5.5 V		1, 2, 3	01		85	mA
Supply current, all outputs low	I_{CCL} 3/	V_{CC} = 5.5 V		1, 2, 3	01		91	mA
Functional test	4/	V_{IN} = V_{IH} min or V_{IL} max verify output V_O, see 4.4.1b		7, 8	01			
Maximum clock frequency	f_{max}	C_L = 15 pF, R_L = 400 Ω, see figure 3 5/		9	01	25		MHz
Propagation delay time from CLK to RCO	t_{PLH}			9	01		35	ns
	t_{PHL}			9			35	
Propagation delay time from CLK ($\overline{LOAD}$ input high) to any Q	t_{PLH}			9	01		20	ns
	t_{PHL}			9			23	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time from CLK ($\overline{LOAD}$ input low) to any Q	t_{PLH}	C_L = 15 pF, R_L = 400 Ω, see figure 3 5/	9	01		25	ns
	t_{PHL}		9			29	
Propagation delay time from ENT to RCO	t_{PLH}		9	01		16	ns
	t_{PHL}		9			16	
Propagation delay time from $\overline{CLR}$ to any Q	t_{PHL}		9	01		38	ns

1/ Not more than one output should be shorted at a time.

2/ I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

3/ I_{CCL} is measure with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

4/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances per MIL-STD-883 may be incorporated. For outputs, $L \le 0.8$ V, $H \ge 2.0$ V.

5/ Propagation delay for clearing is measured from the clock input transition.

Device type	01	
Case outlines	E, F	2
Terminal number	Terminal symbol	
1	$\overline{CLR}$	NC
2	CLK	$\overline{CLR}$
3	A	CLK
4	B	A
5	C	B
6	D	NC
7	ENP	C
8	GND	D
9	$\overline{LOAD}$	ENP
10	ENT	GND
11	Q_D	NC
12	Q_C	$\overline{LOAD}$
13	Q_B	ENT
14	Q_A	Q_D
15	RCO	Q_C
16	V_{CC}	NC
17	- - -	Q_B
18	- - -	Q_A
19	- - -	RCO
20	- - -	V_{CC}

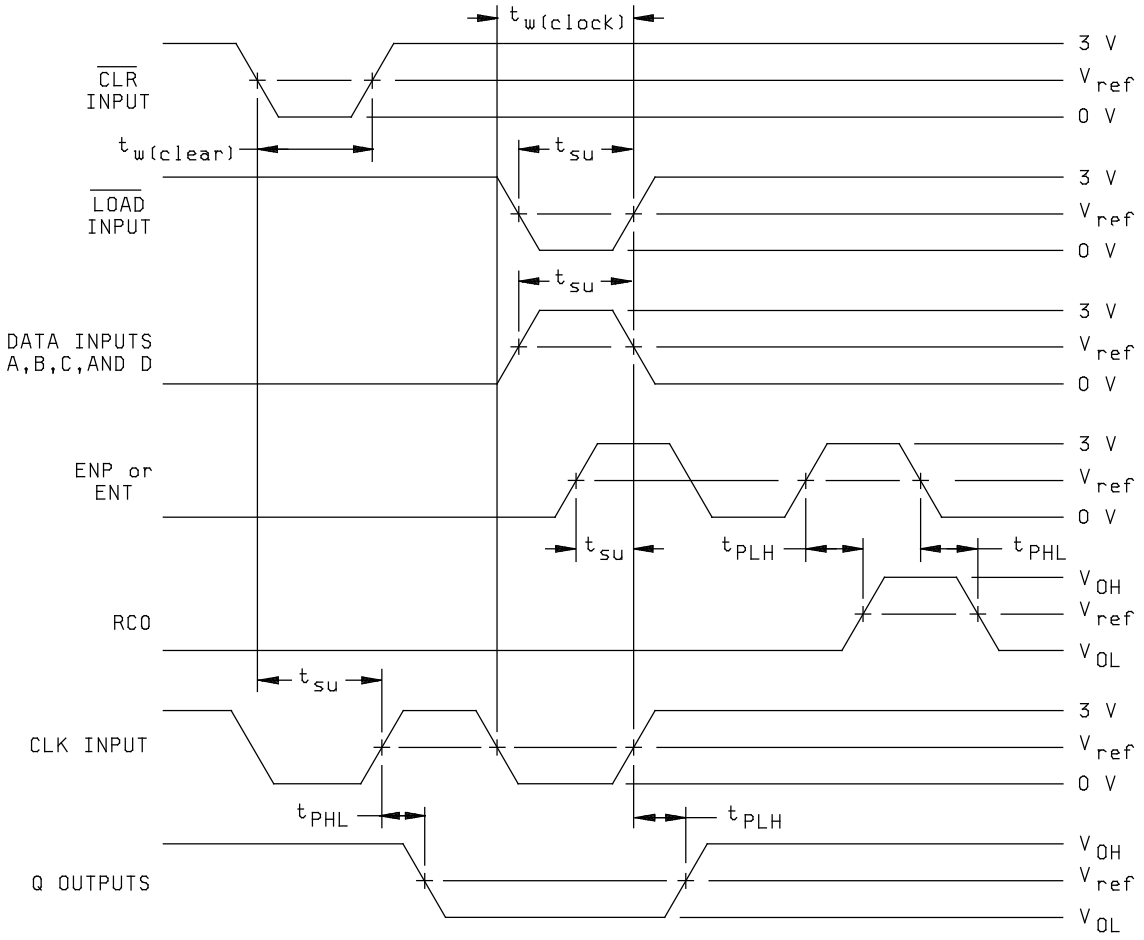
FIGURE 1. Terminal connections.

INPUTS						OUTPUTS		Function
CLR	CLK	ENP	ENT	LOAD	A,B,C,D	Qn	RCO	
L	↑	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	L	L	L	L	Parallel load
H	↑	X	X	L	H	H	See note	Parallel load
H	↑	H	H	H	X	Count	See note	Count
H	X	L	X	H	X	Qn	See note	Inhibit
H	X	X	L	H	X	Qn	L	Inhibit

H = High level.
L = Low level.
X = Don't care.
H = High level one step time prior to the CLK low-to-high transition.
L = Low level one setup time prior to the CLK low-to-high transition.
Qn = The state of the referenced output prior to the CLK low-to-high transition.
↑ = CLK low-to-high transition.

NOTE: The RCO output is high when ENT is high and the counter is at terminal count (HHHH).

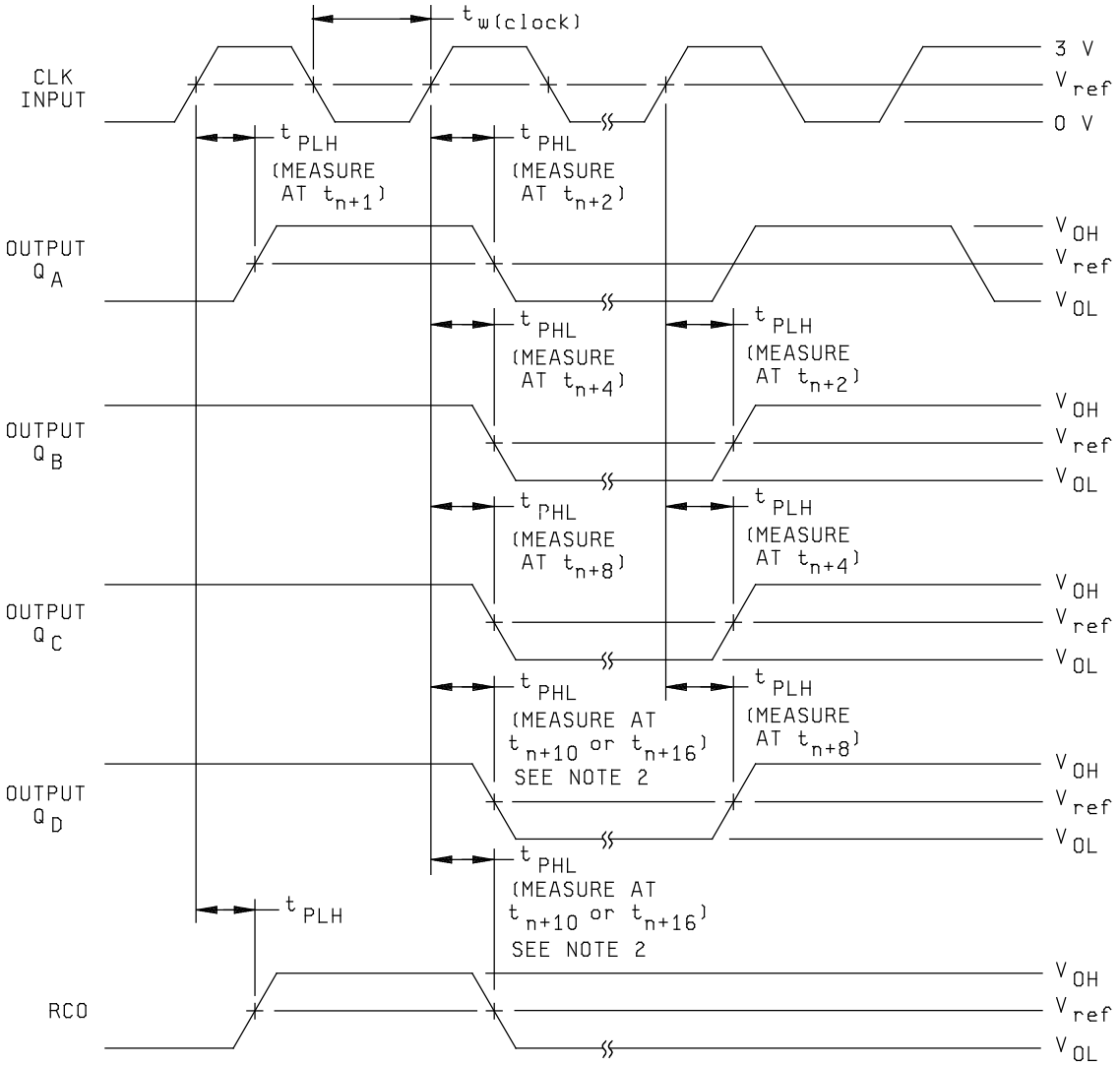
FIGURE 2. Truth table .



NOTES:

1. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \cong 50\ \Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
2. Enable P and enable T setup times are measured at t_{n+0}.
3. $V_{ref} = 1.5$ V

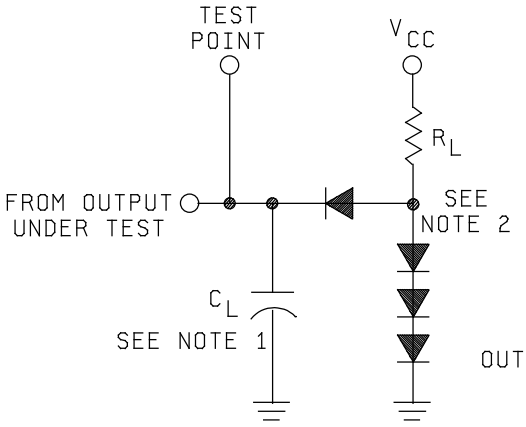
FIGURE 3. Test circuit and switching waveforms.



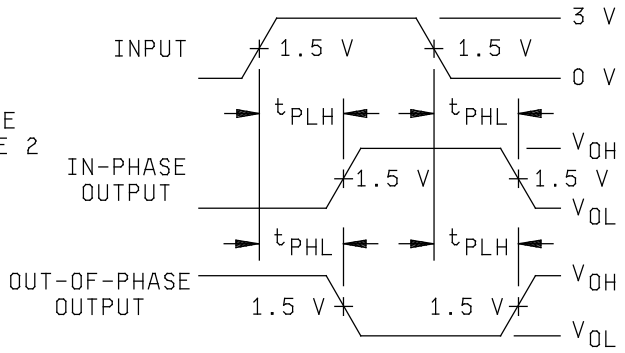
NOTES:

1. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \cong 50\ \Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{max}.
2. Outputs Q_D and carry are tested at t_{n+16}, where t_n is the bit time when all outputs are low.
3. V_{ref} = 1.5 V.

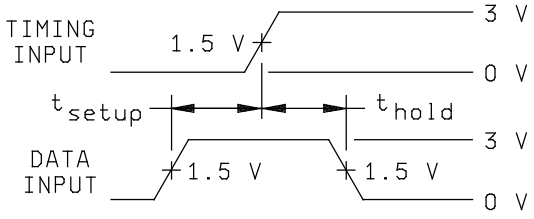
FIGURE 3. Test circuit and switching waveforms – Continued.



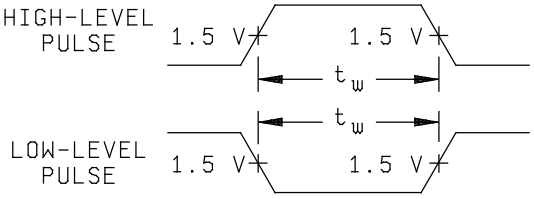
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS

NOTES:

1. C_L includes probe and jig capacitance. C_L = 15 pF, R_L = 400 Ω.
2. All diodes are 1N3064 or equivalent.

FIGURE 3. Test circuit and switching waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 4, 5, 6, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---
Final electrical parameters (see 4.2)	1,2,3,7,8,9 1/	1,2,3 2/ 7,8,9
Group A test requirements (see 4.4)	1,2,3,7,8,9	1,2,3,7,8,9
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3,7,8,9
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-12-02

Approved sources of supply for SMD 5962-97548 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9754801QEA	01295	SNJ54163J
5962-9754801QFA	01295	SNJ54163W
5962-9754801Q2A	3/	

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ This device is not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243