REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Y. Update boilerplate to add device class N. Editorial changes throughout. - ro	98-10-28	R. MONNIN
B	Drawing updated to reflect current requirements. – gt	03-04-11	R. MONNIN
C	Update drawing to current MIL-PRF-38535 requirements. Remove class M references. -rrp	14-03-12	C. SAFFLE

REV																				
SHEET																				
REV	C	C	C	C	C	C														
SHEET	15	16	17	18	19	20														
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

CHECKED BY
RAY MONNIN

APPROVED BY
RAY MONNIN

DRAWING APPROVAL DATE
96-10-15

MICROCIRCUIT, LINEAR, 9-CHANNEL DIFFERENTIAL TRANSCEIVER, MONOLITHIC SILICON

AMSC N/A

REVISION LEVEL
C

SIZE	CAGE CODE	
A	**67268**	**5962-96893**

SHEET 1 OF 20

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device class Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:

5962	-	96893	01	Q	X	A
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

_____ _____/
\V
Drawing number

1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Slew limit Driver	Slew limit Receiver	Circuit function
01	55976A1	8	9	9 Channel Differential Transceiver
02	55976A2	4	5	9 Channel Differential Transceiver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment (encapsulated in plastic)
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Document
X	GDFP1-F56	56	Dual flat pack	MIL-STD-1835
Y	MO-153	56	Plastic small outline package	JEP 95

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}) ..... -0.3 V dc to +6.0 V dc
Voltage range at any bus terminal ..... -10 V dc to +15 V dc
Data I/O and control (A-side) voltage range..... -0.3 V dc to V_{CC} + 0.5 V dc
Electrostatic discharge: B side and GND, Class 3: ..... 12 kV (Human Body Model)
B side and GND: ..... 400 V (Machine Model)
All terminals, Class 3:..... 4 kV (Human Body Model) 3/
All terminals:..... 400 V (Machine Model)
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature, soldering 1.6 mm (1/16 inch) from
case for 10 seconds..... +260°C
Junction-to-ambient thermal resistance, (θ_{JA}) ..... 95.4 °C/W
Junction-to-case thermal resistance, (θ_{JC}) ..... 5.67°C/W
Thermal-shutdown junction temperature, (T_{JS}) ..... 165°C
Maximum power dissipation at T_A = 125°C (in still air) (P_D) ..... 260 mW

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.75 V dc to +5.25 V dc
Minimum high level input voltage (V_{IH}) (except nB+, nB-)..... +2.0 V
Maximum low level input voltage (V_{IL}) (except nB+, nB-)..... +0.8 V
Voltage at any bus terminal (separately or common mode):
(V_O, V_I or V_{IC}) (nB+ or nB-)..... -7 V dc min, 12 V dc max
High level output current (I_{OH}) (Driver) ..... -60 mA
(Receiver)..... -8 mA
Low level output current (I_{OL}) (Driver) ..... +60 mA
(Receiver)..... +8 mA
Ambient operating temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ This absolute maximum rating is tested in accordance with MIL-STD-883C, Method 3015.7.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of this document are available online at www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions for device classes N, Q, and V shall be as specified in MIL-PRF-38535 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. A certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime - VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_A \le +125°C$ $+4.75\ V \le V_{CC} \le +5.25\ V$ unless otherwise specified		V_{CC}	Device type	Group A subgroups	Limits 3/		Unit
							Min	Max	
Driver differential high-level output voltage	V_{ODH}	S1 to A, see figure 3	V_T = 5 V	4.75 V to 5.25 V	All	1	1.0		V
						2, 3	0.7		
		S1 to B, see figure 3				1	0.8		
						2, 3	0.7		
Driver differential low-level output voltage	V_{ODL}	S1 to B, see figure 3	V_T = 5 V	4.75 V to 5.25 V	All	1		-1.0	V
						2, 3		-0.7	
		S1 to A, see figure 3				1		-0.8	
						2, 3		-0.7	
High level output voltage	V_{OH}	A side, V_{ID} = 200 mV see figure 4	I_{OH} = -8 mA	4.75 V to 5.25 V	All	1, 2, 3	4.0		V
Low level output voltage	V_{OL}	A side, V_{ID} = -200 mV see figure 4	I_{OL} = 8 mA	4.75 V to 5.25 V	All	1, 2, 3		0.8	V
Receiver positive differential input threshold voltage	V_{IT+}	I_{OH} = -8 mA, see figure 4		4.75 V to 5.25 V	All	1, 2, 3		0.2	V
Receiver negative differential input threshold voltage	V_{IT-}	I_{OL} = 8 mA, see figure 4		4.75 V to 5.25 V	All	1, 2, 3		-0.2	V
Receiver input hysteresis (V_{IT+} - V_{IT-})	V_{hys}	T_A = 25°C		5.0 V	All	1	24.0		mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T_A ≤ +125°C +4.75 V ≤ V_{CC} ≤ +5.25 V unless otherwise specified		V_{CC}	Device type	Group A subgroups	Limits 3/		Unit
							Min	Max	
Bus input current	I_I	V_{IH} = 12 V, Other input at 0 V		5.0 V	All	1, 2, 3		1.0	mA
				0.0 V				1.0	
		V_{IH} = -7 V, Other input at 0 V		5.0 V				-0.8	
				0.0 V				-0.8	
High-level input current	I_{IH}	A, BSR, CRE, and DE/RE	V_{IH} = 2.0 V	4.75 V to 5.25 V	All	1, 2, 3		-100	µA
		CDE0, CDE1 and CDE2						+100	
Low-level input current	I_{IL}	A, BSR, CRE, and DE/RE	V_{IH} = 0.8 V	4.75 V to 5.25 V	All	1, 2, 3		-100	µA
		CDE1, CDE1 and CDE2						+100	
Short circuit output current	I_{OS}	nB+ or nB-		4.75 V to 5.25 V	All	1, 2, 3		±260	mA
Supply current	I_{CC}	Disabled		4.75 V to 5.25 V	All	1, 2, 3		10.0	mA
		All drivers enabled, no load						60.0	
		All receivers enabled, no load						45.0	
Driver switching characteristics									
Functional test 3014	4/	V_{IH} = 2.0 V, V_{IL} = 0.8 V Verify output V_O see 4.4.1b		4.75 V to 5.25 V	All	7, 8	L	H	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_A \le +125°C$ $+4.75\ V \le V_{CC} \le +5.25\ V$ unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits 3/		Unit
						Min	Max	
Driver switching characteristics - continued								
Propagation delay time, t_{PHL} or t_{PLH}	t_{pd}	See figure 3	5.0 V	01	9	3.0	11.0	ns
					10, 11		15.0	
				02	9	5.0	9.0	
					10, 11		13.5	
Skew limit, maximum t_{pd} - minimum t_{pd}	$t_{sk(lim)}$		4.75 V to	01	9, 10, 11		8.0	ns
	5/		5.25 V	02			4.0	
Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	$t_{sk(p)}$		4.75 V to 5.25 V	All	9, 10, 11		4.0	ns
Enable time, control inputs to active output	t_{en}		4.75 V to	All	9		50.0	ns
			5.25 V		10, 11		60.0	
Disable time, control inputs to high impedance output	t_{dis}		4.75 V to	All	9		100	ns
			5.25 V		10, 11		140	
Propagation delay time, high-level to high impedance output	t_{PHZ}	see figure 5	4.75 V to	All	9		100	ns
			5.25 V		10, 11		120	
Propagation delay time, low-level to high impedance output	t_{PLZ}	see figure 5	4.75 V to	All	9		100	ns
			5.25 V		10, 11		120	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T_A ≤ +125°C +4.75 V ≤ V_{CC} ≤ +5.25 V unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits 3/		Unit
						Min	Max	
Driver switching characteristics - continued								
Propagation delay time, high impedance to high- level output	t_{PZH}	see figure 5	4.75 V to 5.25 V	All	9		50.0	ns
					10, 11		60.0	
Propagation delay time, high impedance to low-level output	t_{PZL}		4.75 V to 5.25 V		9		50.0	
					10, 11		60.0	
Receiver switching characteristics								
Functional test 3014	4/	V_{IH} = 2.0 V, V_{IL} = 0.8 V Verify output V_O see 4.4.1b	4.75 V to 5.25 V	All	7, 8	L	H	
Propagation delay time, t_{PHL} or t_{PLH}	t_{pd}	see figure 4	5.0 V	01	9	7.5	16.5	ns
					10, 11		19.0	
				02	9	8.6	13.6	
					10, 11		16.0	
Skew limit, maximum t_{pd} - minimum t_{pd}	$t_{sk(lim)}$		4.75 V to 5.25 V	01	9, 10, 11		9.0	ns
	5/			02			5.0	
Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	$t_{sk(p)}$		4.75 V to 5.25 V	All	9, 10, 11		4.0	ns
Enable time, control inputs to active output	t_{en}		4.75 V to 5.25 V	All	9		50.0	ns
					10, 11		70.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T_A ≤ +125°C +4.75 V ≤ V_{CC} ≤ +5.25 V unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits 3/		Unit
						Min	Max	
Receiver switching characteristics - continued								
Disable time, control inputs to high impedance output	t_{dis}		4.75 V to 5.25 V	All	9		60.0	ns
					10, 11		80.0	
Propagation delay time, high-level to high impedance output	t_{PHZ}	See figure 6	4.75 V to 5.25 V	All	9		60.0	ns
					10, 11		80.0	
Propagation delay time, low-level to high impedance output	t_{PLZ}		4.75 V to 5.25 V		9		50.0	
					10, 11		70.0	
Propagation delay time, high impedance to high-level output	t_{PZH}	See figure 6	4.75 V to 5.25 V	All	9		50.0	ns
					10, 11		70.0	
Propagation delay time, high impedance to low-level output	t_{PZL}		4.75 V to 5.25 V		9		50.0	
					10, 11		70.0	

1/ For tests not listed in the referenced MIL-STD-883, utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

5/ This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions and to any two devices.

Case Y

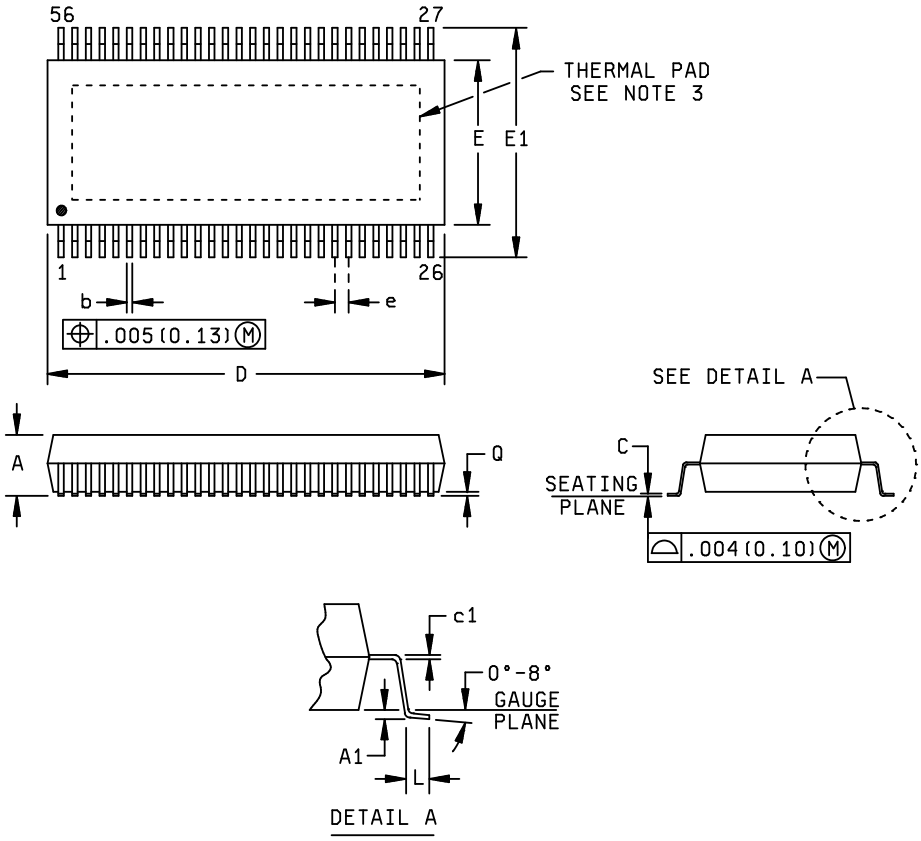


FIGURE 1. Case outline.

Case Y

Symbol	Millimeters		Notes
	Min	Max	
A	---	1.20	
A1	0.25	---	
b	0.170	0.270	
C	0.10	---	
c1	0.15	---	
D	13.90	14.10	
E	6.00	6.20	
E1	7.90	8.30	
e	0.500	---	
L	0.500	0.750	
Q	0.50	0.150	

NOTES:

1. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm.
2. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die possibly selected leads.
3. Falls within JEDEC MO-153.

FIGURE 1. Case outline - Continued.

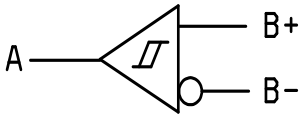
Device types	01 and 02		
Case outlines	X and Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	29	1B-
2	BSR	30	1B+
3	$\overline{CRE}$	31	2B-
4	1A	32	2B+
5	1DE/$\overline{RE}$	33	3B-
6	2A	34	3B+
7	2DE/$\overline{RE}$	35	4B-
8	3A	36	4B+
9	3DE/$\overline{RE}$	37	5B-
10	4A	38	5B+
11	4DE/$\overline{RE}$	39	V_{CC}
12	V_{CC}	40	GND
13	GND	41	GND
14	GND	42	GND
15	GND	43	GND
16	GND	44	GND
17	GND	45	V_{CC}
18	V_{CC}	46	6B-
19	5A	47	6B+
20	5DE/$\overline{RE}$	48	7B-
21	6A	49	7B+
22	6DE/$\overline{RE}$	50	8B-
23	7A	51	8B+
24	7DE/$\overline{RE}$	52	9B-
25	8A	53	9B+
26	8DE/$\overline{RE}$	54	CDE0
27	9A	55	CDE1
28	9DE/$\overline{RE}$	56	CDE2

FIGURE 2. Terminal connections.

Terminal Functions				
Terminal	Logic level	I/O	Termination	Description
mA (m = 1 to 9)	TTL	I/O	Pullup	1A to 9A carry data to and from the communication controller.
mB- (m = 1 to 9)	RS-485	I/O	Pulldown	1B- to 9B- are the inverted data signals of the balanced pair to/from the bus.
mB+ (m = 1 to 9)	RS-485	I/O	Pullup	1B+ to 9B+ are the noninverted data signals of the balanced pair to/from the bus.
BSR	TTL	Input	Pullup	BSR is the bit significant response. BSR disables receivers 1 through 8 and enables wired-OR drivers when BSR and DE/$\overline{RE}$ and CDE1 or CDE2 are high. Channel 9 is placed in a high-impedance state with BSR high.
CDE0	TTL	Input	Pulldown	CDE0 is the common driver enable 0. Its input signal enables all drivers when CDE0 and 1DE/$\overline{RE}$ - 9DE/$\overline{RE}$ are high.
CDE1	TTL	Input	Pulldown	CDE1 is the common driver enable 1. Its input signal enables drivers 1 to 4 when CDE1 is high and BSR is low.
CDE2	TTL	Input	Pulldown	CDE2 is the common driver enable 2. When CDE2 is high and BSR is low, drivers 5 to 8 are enabled.
$\overline{CRE}$	TTL	Input	Pullup	$\overline{CRE}$ is the common receiver enable. When high, $\overline{CRE}$ disables receiver channels 5 to 9.
mDE/$\overline{RE}$ (m = 1 to 9)	TTL	Input	Pullup	1DE/$\overline{RE}$ - 9DE/$\overline{RE}$ are direction controls that transmit data to the bus when it and CDE0 are high. Data is received from the bus when 1DE/$\overline{RE}$ - 9DE/$\overline{RE}$ and $\overline{CRE}$ and BSR are low and CDE1 and CDE2 are low.

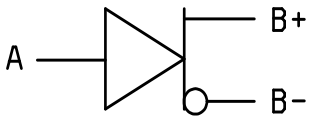
FIGURE 2. Terminal connections - Continued.

RECEIVER



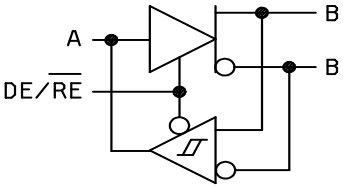
INPUTS		OUTPUT
B+1/	B-1/	A
L	H	L
H	L	H

DRIVER



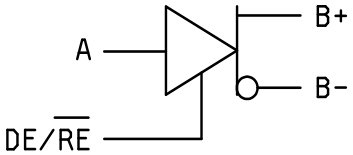
INPUT	OUTPUTS	
A	B+	B-
L	L	H
H	H	L

TRANSCEIVER



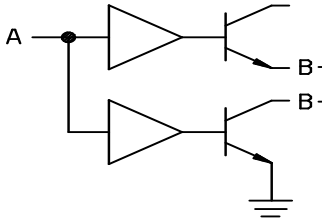
INPUTS				OUTPUTS		
DE/$\overline{RE}$	A	B+1/	B-1/	A	B+	B-
L	-	L	H	L	-	-
L	-	H	L	H	-	-
H	L	-	-	-	L	H
H	H	-	-	-	H	L

DRIVER WITH ENABLE



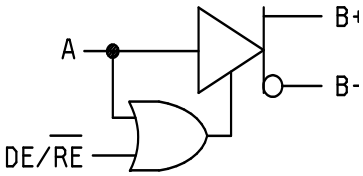
INPUTS		OUTPUTS	
DE/$\overline{RE}$	A	B+	B-
L	L	Z	Z
L	H	Z	Z
H	L	L	H
H	H	H	L

WIRED-OR DRIVER



INPUT	OUTPUTS	
A	B+	B-
L	Z	Z
H	H	L

TWO-ENABLE INPUT DRIVE

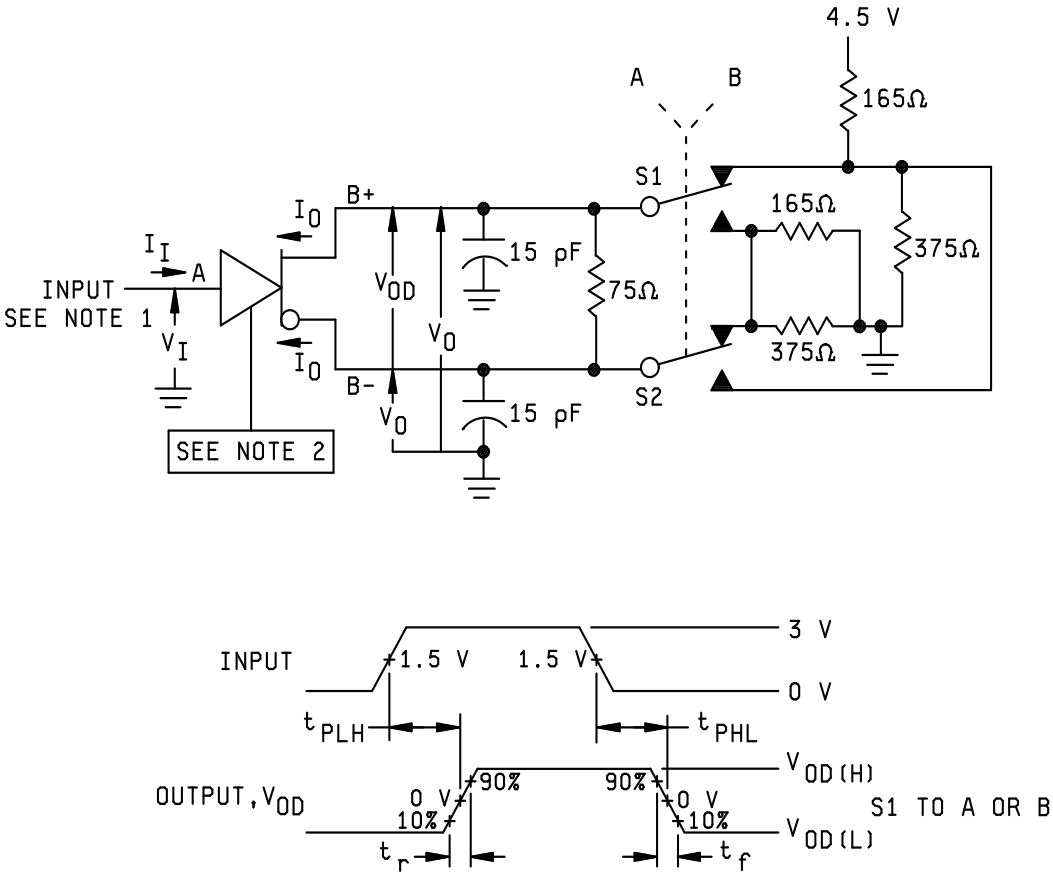


INPUTS		OUTPUTS	
DE/$\overline{RE}$	A	B+	B-
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	H	L

NOTES: H = high level, L = low level, Z = high impedance (off).

1/ "H" in this column represents a voltage of 200 mV or higher than the other bus input. "L" represents a voltage of 200 mV or lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

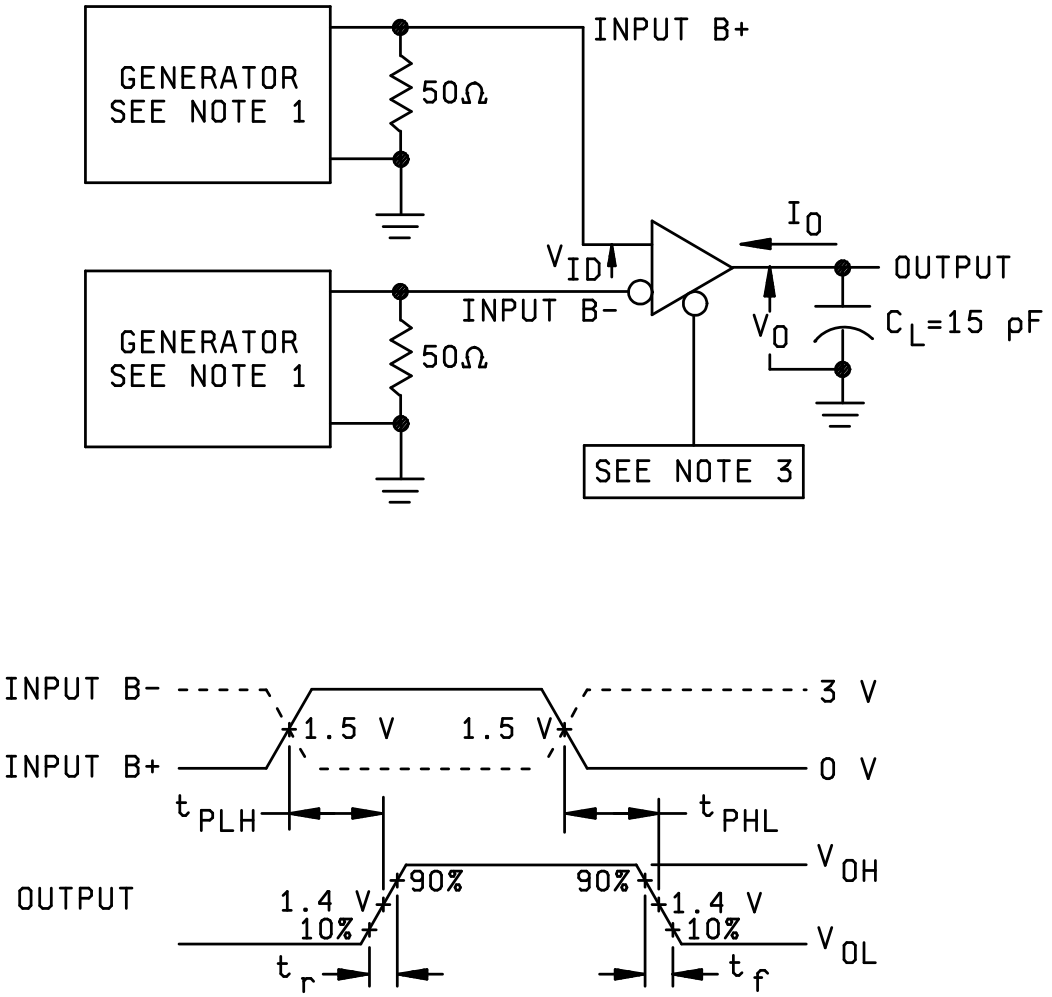
FIGURE 3. Truth table.



NOTES:

1. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR $\leq$ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
2. CDE0 and DE/$\overline{RE}$ are at 2 V, BSR is at 0.8 V.
3. All resistances are ±5%, unless otherwise indicated.
4. All capacitances are ±10%, unless otherwise indicated.
5. All indicated voltages are ±10 mV.

FIGURE 4. Driver delay and transition test circuit and timing waveforms.



NOTES:

1. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\Omega$.
2. All indicated voltages are ±10 mV.
3. CDE0, CDE1, CDE2, BSR, CRE, and DE/$\overline{RE}$ at 0.8 V.
4. All resistances are ±5%, unless otherwise indicated.
5. All capacitances are ±10%, unless otherwise indicated.

FIGURE 5. Receiver delay and transition test circuit and timing waveforms.

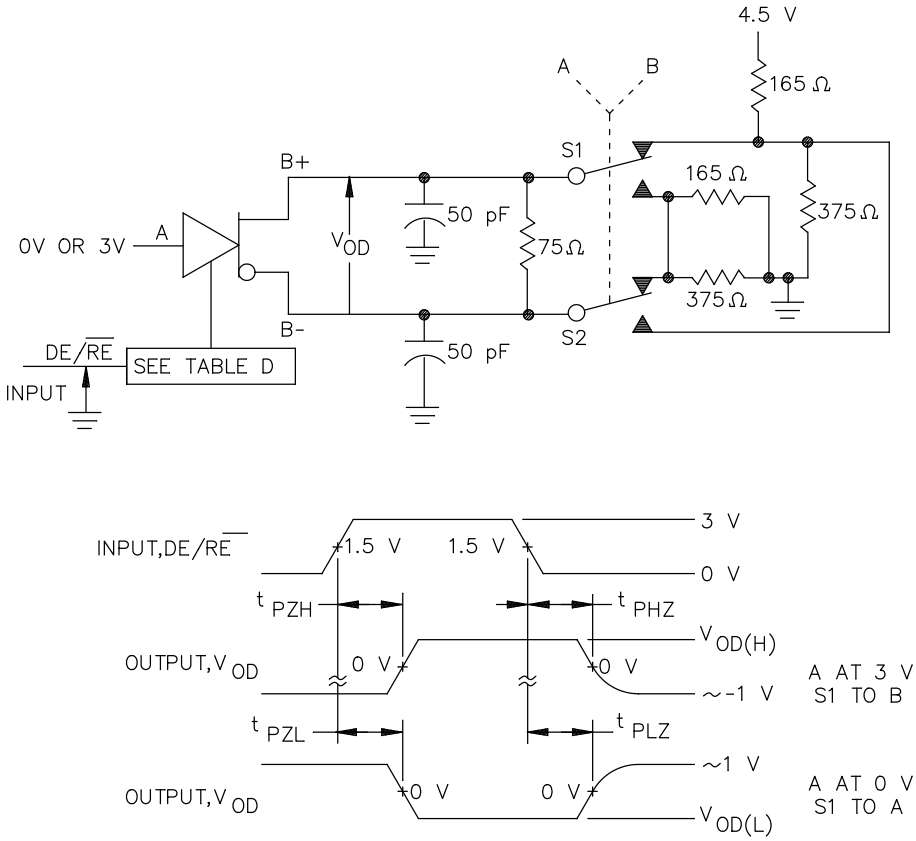


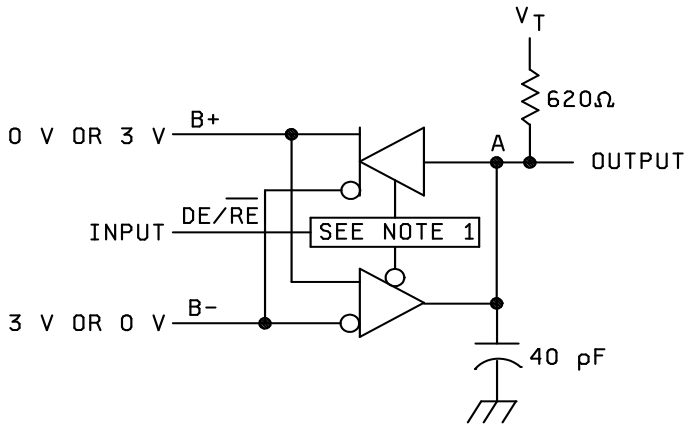
TABLE D. Enabling for driver enable and disable time.

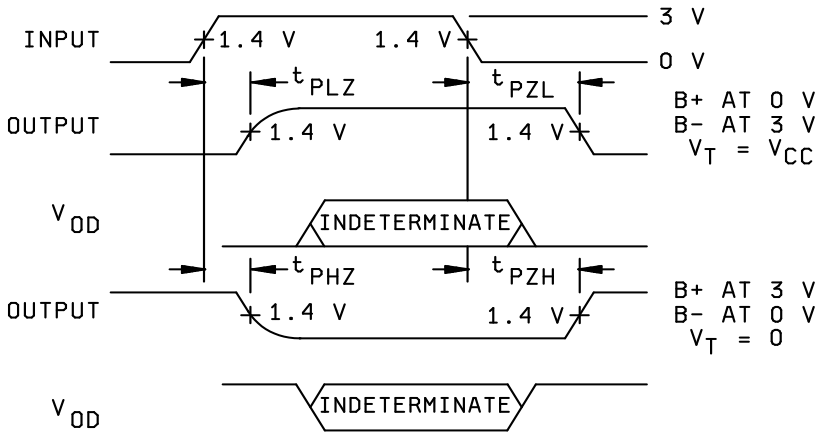
DRIVER	BSR	CDE0	CDE1	CDE2	$\overline{CRE}$
1 – 8	H	H	L	L	X
9	L	H	H	H	H

NOTES:

1. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR $\leq$ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
2. All indicated voltages are ±10 mV.
3. All resistances are ±5%, unless otherwise indicated.
4. All capacitances are ±10%, unless otherwise indicated.

FIGURE 6. Driver enable and disable time test circuit and timing waveforms.





NOTES:

1. CDE0 is high, CDE1, CDE2, BSR, and $\overline{\text{CRE}}$ are low.
2. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR $\leq$ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
3. All indicated voltages are ±10 mV.
4. All resistances are ±5%, unless otherwise indicated.
5. All capacitances are ±10%, unless otherwise indicated.

FIGURE 6. Receiver enable and disable time test circuit and timing waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,8, 2/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes N, Q, and V, subgroups 7 and 8 shall be sufficient to verify the truth table.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. The devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply. Sources of supply for device classes N, Q, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-03-12

Approved sources of supply for SMD 5962-96893 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9689301NYD	3/	SNJ55976A1DCA
5962-9689301QXA	01295	SNJ55976A1WD
5962-9689302NYD	3/	SNJ55976A2DCA
5962-9689302QXA	01295	SNJ55976A2WD

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.