REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R339-97.	97-05-20	R. Monnin
B	Updated drawing to reflect current requirements. Redrawn. -rrp	02-11-18	R. Monnin
C	Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw	15-04-24	Charles F. Saffle
D	Update paragraphs to current MIL-PRF-38535 requirements. - drw	20-11-13	James R. Eschmeyer

REV																				
SHEET																				
REV	D	D	D	D																
SHEET	15	16	17	18																
REV STATUS			REV			D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
96-10-14

REVISION LEVEL
D

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL-LINEAR, CMOS, 12-BIT ANALOG TO DIGITAL CONVERTER WITH SERIAL CONTROL AND 11 ANALOG INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96886**

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	96886	01	Q	R	A
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

__________ __________/
V
Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	TLC2543	12-bit analog to digital converter with serial control and 11 analog inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat package
2	CQCC1-N20	20	Leadless chip carrier package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC})	-0.5 V dc to +6.5 V dc 2/
Input voltage range (V_{IN})(any input)	-0.3 V dc to V_{CC} +0.3 V dc
Output voltage (V_{OUT})	-0.3 V dc to V_{CC} +0.3 V dc
Positive reference voltage, V_{ref+}	V_{CC} +0.1 V dc
Negative reference voltage, V_{ref-}	-0.1 V dc
Peak input current (any input)	±20 mA
Peak total input current (all inputs)	±30 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Positive reference voltage, (V_{ref+})	V_{CC} 3/
Negative reference voltage, (V_{ref-})	0.0 V 3/
Differential reference voltage, V_{ref+} - V_{ref-}	+2.5 V dc to V_{CC} +0.1 V dc 3/
Analog input voltage	0.0 V to V_{CC} 3/
High-level control input voltage, V_{IH} (V_{CC} =3.0 V to 3.6 V)	2.0 V dc
Low-level control input voltage, V_{IL} (V_{CC} = 3.0 V to 3.6 V)	0.8 V dc
Clock frequency at I/O CLOCK	0.0 MHz to 4.1 MHz
Setup time, Address bits at data input before I/O CLOCK↑, $t_{su(A)}$	100 ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$	0.0 ns (min)
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$	0.0 ns (min)
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$	1.425 µs 4/
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$	120 ns (min)
Pulse duration I/O CLOCK Low, $t_{wL(I/O)}$	120 ns (min)
Transition time, I/O CLOCK, $t_{t(I/O)}$	1 µs (min) 5/
Transition time, DATA INPUT and $\overline{CS}$, $t_{t(CS)}$	10 µs (min)
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise noted).

3/ Anaolg input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to V(V_{ref+} - V_{ref-}); However, the electrical specifications are no longer applicable.

4/ To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

5/ This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Load circuit. The load circuit shall be as specified on figure 4.

3.2.6 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

TABLE I. Electrical performance characteristics.

Test 1/	Symbol	Conditions -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level output voltage	V_{OH}	I_{OH} = -1.6 mA, V_{CC} = 4.5 V	1, 2, 3	01	2.4		V
		I_{OH} = -20 μA, V_{CC} = 4.5 V to 5.5 V			VCC - 0.1		
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA, V_{CC} = 4.5 V	1, 2, 3	01		0.4	V
		I_{OL} = 20 μA, V_{CC} = 4.5 V to 5.5 V				0.1	
Off-state (high-impedance state) output current	I_{OZH}	$\overline{CS}$ at V_{CC}, V_{OUT} = V_{CC} = 4.5 V to 5.5 V	1, 2, 3	01		2.5	μA
	I_{OZL}	$\overline{CS}$ at V_{CC}, V_{OUT} = 0, V_{CC} = 4.5 V to 5.5 V				-2.5	
Input current high	I_{IH}	V_I = V_{CC}, V_{CC} = 4.5 V to 5.5 V	1, 2, 3	01		10.0	μA
Input current low	I_{IL}	V_I = 0, V_{CC} = 4.5 V to 5.5 V	1, 2, 3	01		-10.0	μA
Operating supply current	I_{CC}	$\overline{CS}$ at 0 V, V_{CC} = 4.5 V to 5.5 V	1, 2, 3	01		10.0	mA
Power-down current	$I_{CC(PD)}$	For all digital inputs, 0 ≤ V_I ≤ 0.5 V or V_I ≥ V_{CC} – 0.5 V	1, 2, 3	01		25	μA
Selected channel leakage current	----	Selected channel at V_{CC}, Unselected channel at 0 V, V_{CC} = 4.5 V to 5.5 V	1, 2, 3	01		10	μA
		Selected channel at 0 V, Unselected channel at V_{CC}, V_{CC} = 4.5 V to 5.5 V				-10	
Maximum static analog reference current into REF+	----	V_{REF+} = V_{CC}, V_{REF-} = GND, V_{CC} = 4.5 V to 5.5 V	1, 2, 3	01		10.0	μA
Input capacitance	C_I	Analog inputs, V_{CC} = 4.5 V to 5.5 V, See 4.4.1c	4	01		60	pF
		Control inputs, V_{CC} = 4.5 V to 5.5 V, See 4.4.1c				15	
Functional test		See 4.4.1b	7, 8	01			
Linearity error 2/	E_L	See figure 5, 3/ V_{CC} = 4.5 V to 5.5 V	4, 5, 6	01		±1	LSB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test 1/	Symbol	Conditions -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Differential linearity error	E_D	See figure 5, 3/ V_{CC} = 4.5 V to 5.5 V	4, 5, 6	01		±1	LSB
Offset error 4/	E_O	See figure 5, 3/ V_{CC} = 4.5 V to 5.5 V	4, 5, 6	01		±1.5	LSB
Gain error 4/	E_G	See figure 5, 3/ V_{CC} = 4.5 V to 5.5 V	4, 5, 6	01		±1	LSB
Total adjusted error 5/	E_T		4, 5, 6	01		±1.75	LSB
Conversion time	t_{CONV}	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		10	µs
Total cycle time (access, sample, and conversion)	t_C	See figure 5, 6/ V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		10 + total I/O CLOCK periods + $t_{d(I/O-EOC)}$	µs
Channel acquisition time (sample)	t_{acq}	See figure 5, 6/ V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01	4	12	I/O CLOCK periods
Valid time, DATA OUT remains valid after I/O CLOCK↓	t_V	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01	10		ns
Delay time, I/O CLOCK↓ to DATAOUT valid	$t_{d(I/O-DATA}$	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		150	ns
Delay time, last I/O CLOCK↓ to EOC↓	$t_{d(I/O-EOC)}$	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		2.2	ns
Delay time, EOC↑ to DATA OUT (MSB)	$t_{d(EOC-DATA}$	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		100	ns
Enable time, $\overline{CS}$↓ to DATA OUT (MSB/LSB driven)	t_{PZH}, t_{PZL}	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		1.3	µs
Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	t_{PHZ}, t_{PLZ}	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		150	ns
Rise time, EOC	$t_{r(EOC)}$	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		50	ns
Fall time, EOC	$t_{f(EOC)}$	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		50	ns
Rise time, data bus	$t_{r(bus)}$	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		50	ns
Fall time, data bus	$t_{f(bus)}$	See figure 5, V_{CC} = 4.5 V to 5.5 V	9, 10, 11	01		50	ns
Delay time, last I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion	$t_{d(I/O-CS)}$	V_{CC} = 4.5 V to 5.5 V 7/	9, 10, 11	01		5	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

1/ All voltage values are with respect to GND with REF- and GND wired together (unless otherwise noted).

2/ Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristic.

3/ Analog input voltages greater than applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000).

4/ Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep at the offset point.

5/ Total unadjusted error comprises linearity, zero-scale, and full-scale errors.

6/ I/O CLOCK period = 1/(I/O CLOCK frequency).

7/ Any transitions of $\overline{CS}$ are recognized as valid only if the levels is maintained for a setup time. $\overline{CS}$ must be taken low at ≤ 5 μs of the tenth I/O CLOCK falling edge to ensure a conversion is aborted. Between 5 μs and 10 μs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

Device type	01
Case outline	R, S, and 2
Terminal number	Terminal symbol
1	ANI0
2	ANI1
3	ANI2
4	ANI3
5	ANI4
6	ANI5
7	ANI6
8	ANI7
9	ANI8
10	GND
11	ANI9
12	ANI10
13	REF-
14	REF+
15	$\overline{\text{CS}}$
16	DATA OUT
17	DATA INPUT
18	I/O CLOCK
19	EOC
20	V_{CC}

Pin description	
Terminal symbol	Description
AINn (n = 0 to 10)	Analog signal inputs
REF-	Lower reference voltage
REF+	Upper reference voltage
$\overline{\text{CS}}$	Chip select
DATA OUT	Serial data input
DATA INPUT	Serial data input
I/O CLOCK	Input-Output clock
EOC	End of conversion

FIGURE 1. Terminal connections.

Analog-Channel-Select Address

Analog Input Selected	Value Shifted Into Address	
	Binary	Hex
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED 1/	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX) 2/
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	00
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

1/ V_{ref+} is the voltage supplied to REF+, and V_{ref-} is the voltage applied to REF-.
2/ The output results shown are the ideal values and may vary with the reference stability and with internal offsets.

Power-Down-Select Address

INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \leq 25\ \mu A$

FIGURE 2. Truth tables.

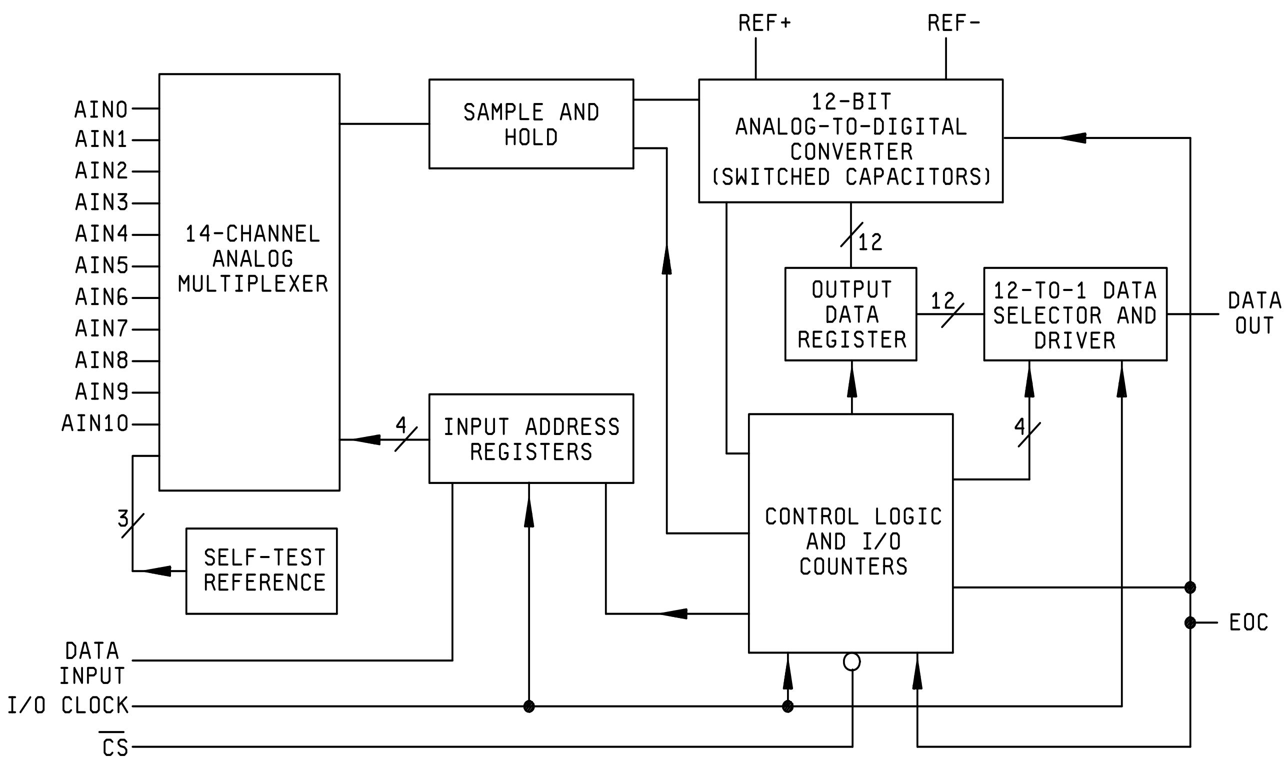


FIGURE 3. Block diagram.

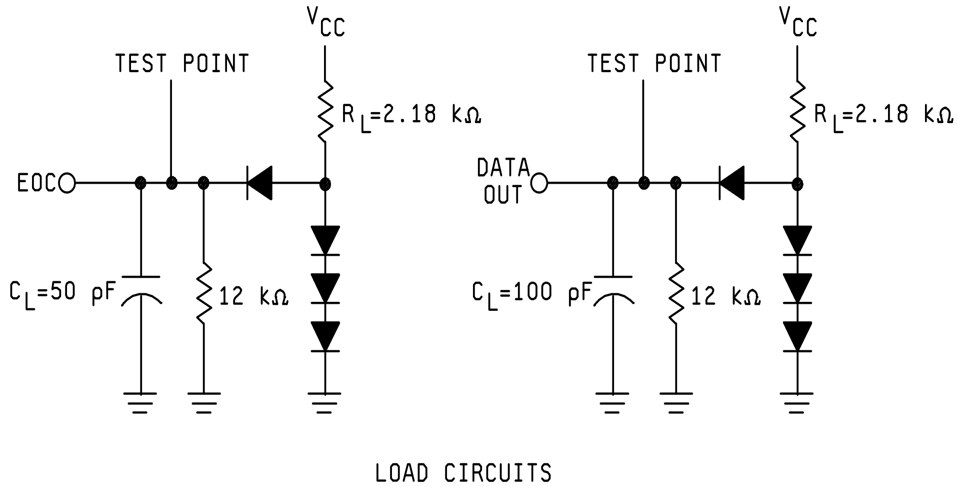
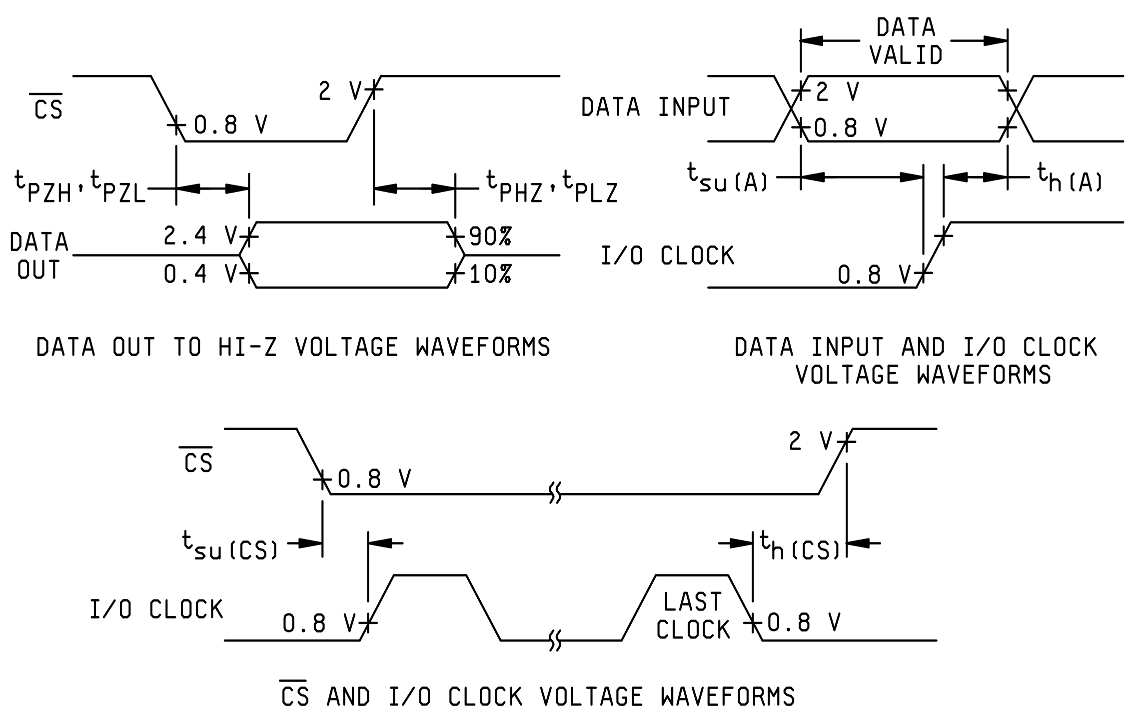


FIGURE 4. Load circuit.



NOTE: To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

FIGURE 5. Timing waveforms.

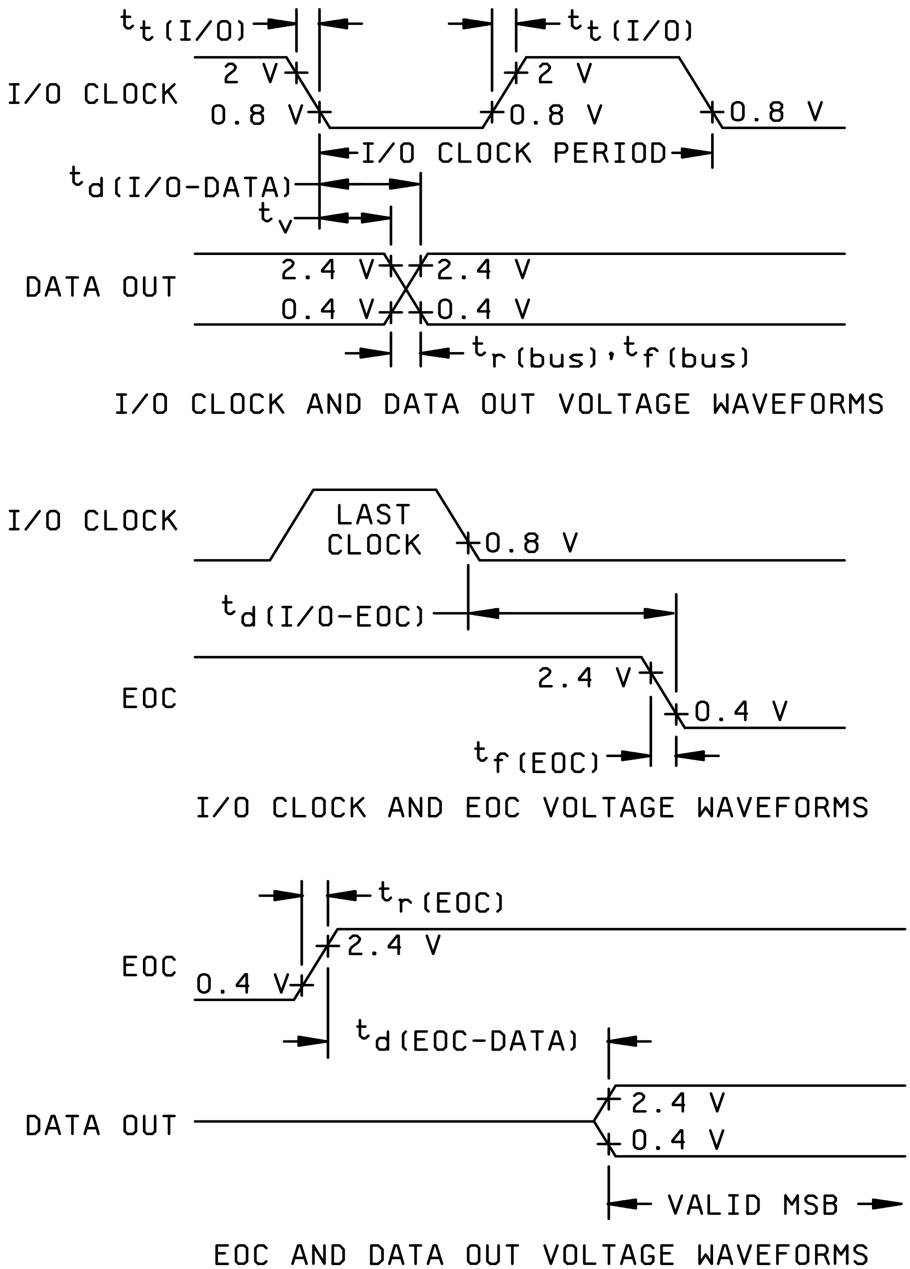
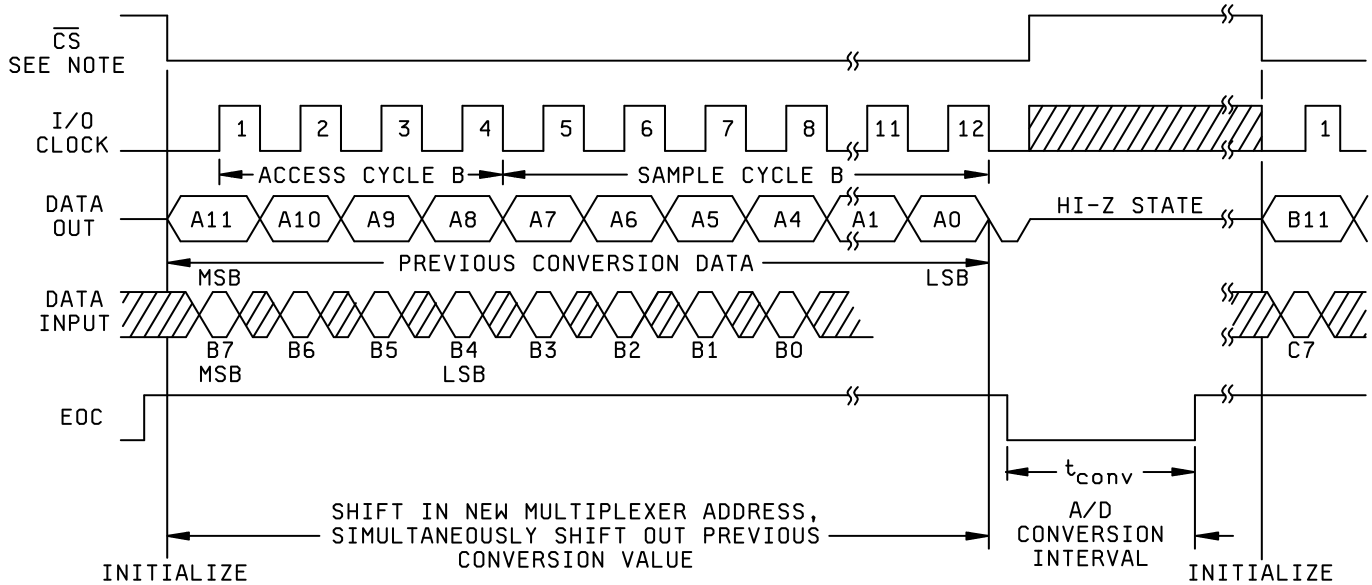
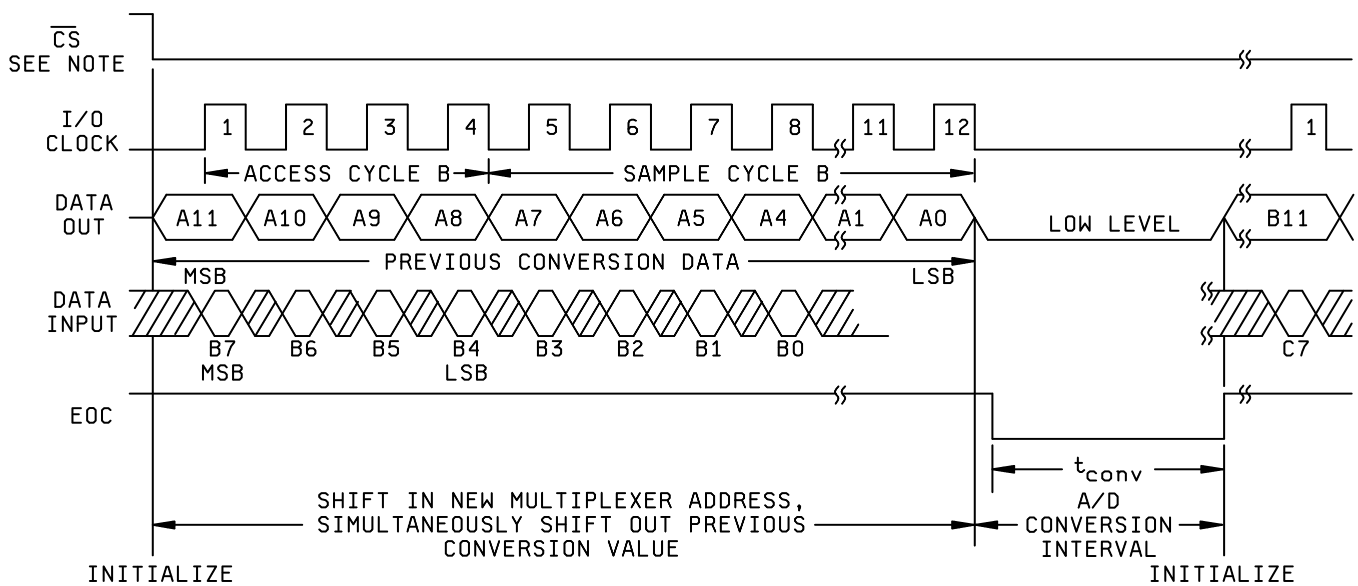


FIGURE 5. Timing waveforms - continued.



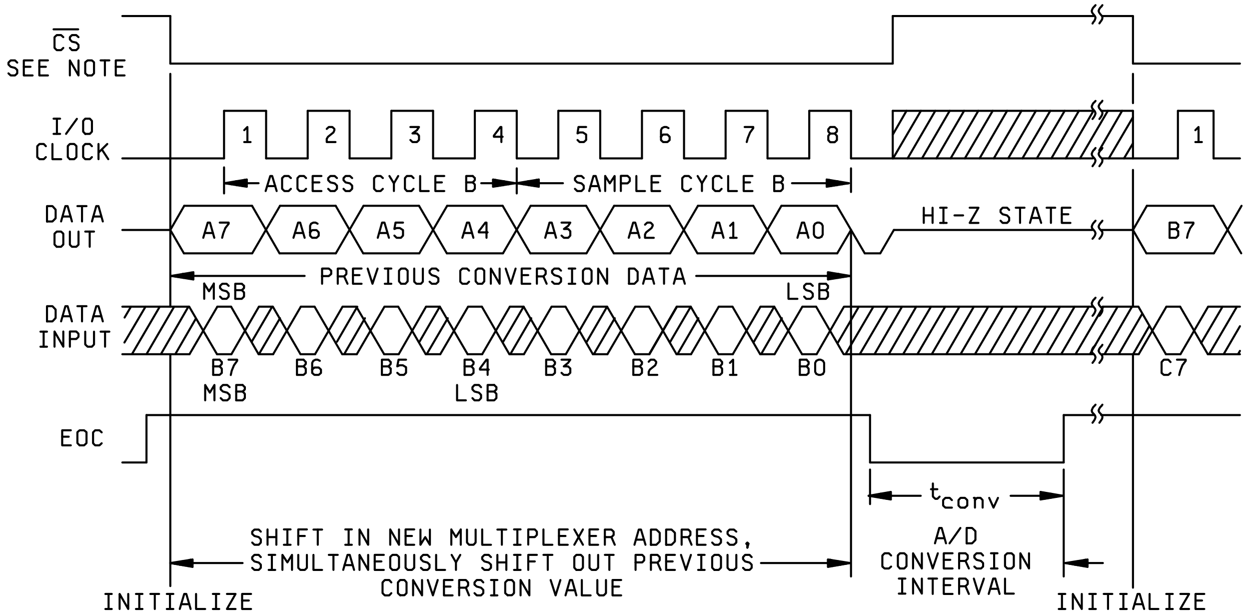
TIMING FOR 12-CLOCK TRANSFER USING $\overline{CS}$ WITH MSB FIRST



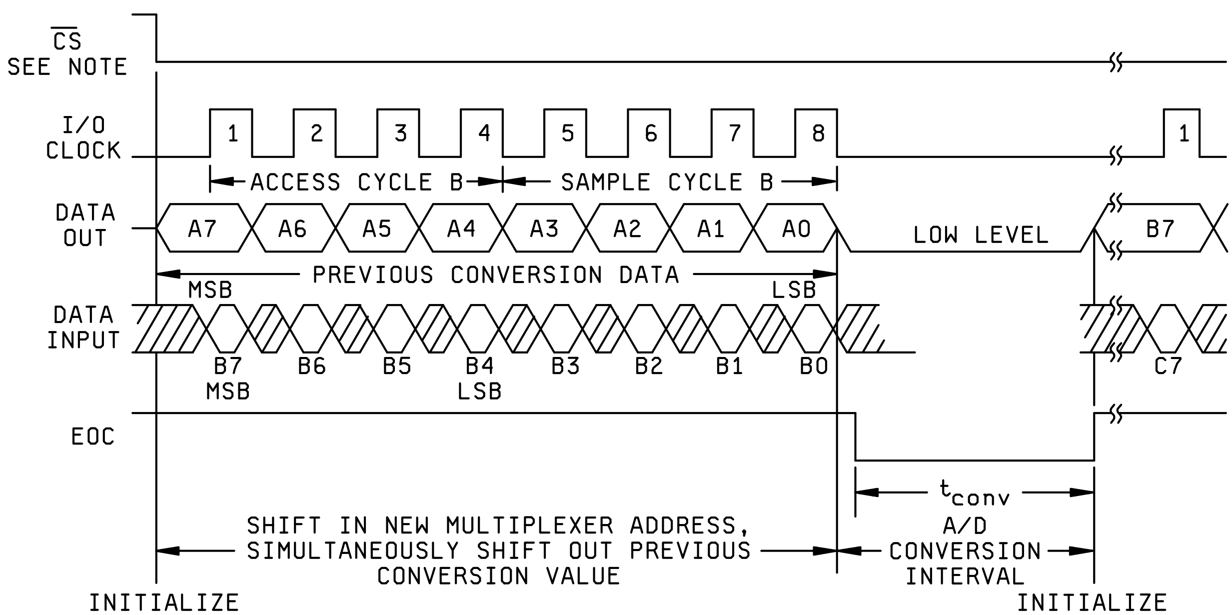
TIMING FOR 12-CLOCK TRANSFER NOT USING $\overline{CS}$ WITH MSB FIRST

NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

FIGURE 5. Timing waveforms - continued.



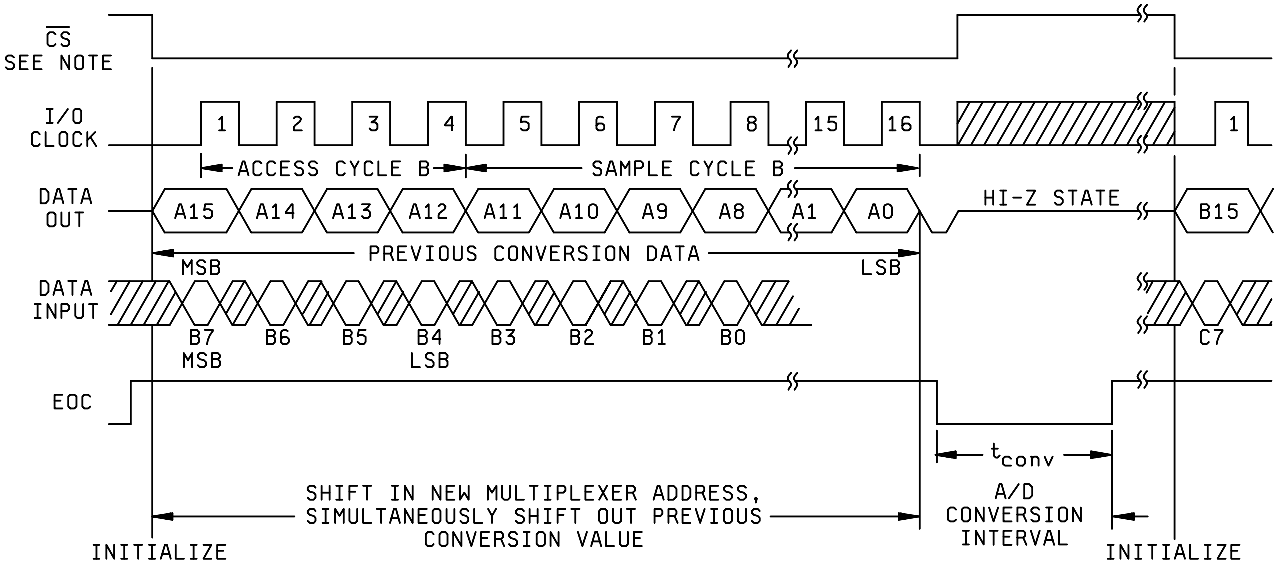
TIMING FOR 8-CLOCK TRANSFER USING $\overline{CS}$ WITH MSB FIRST



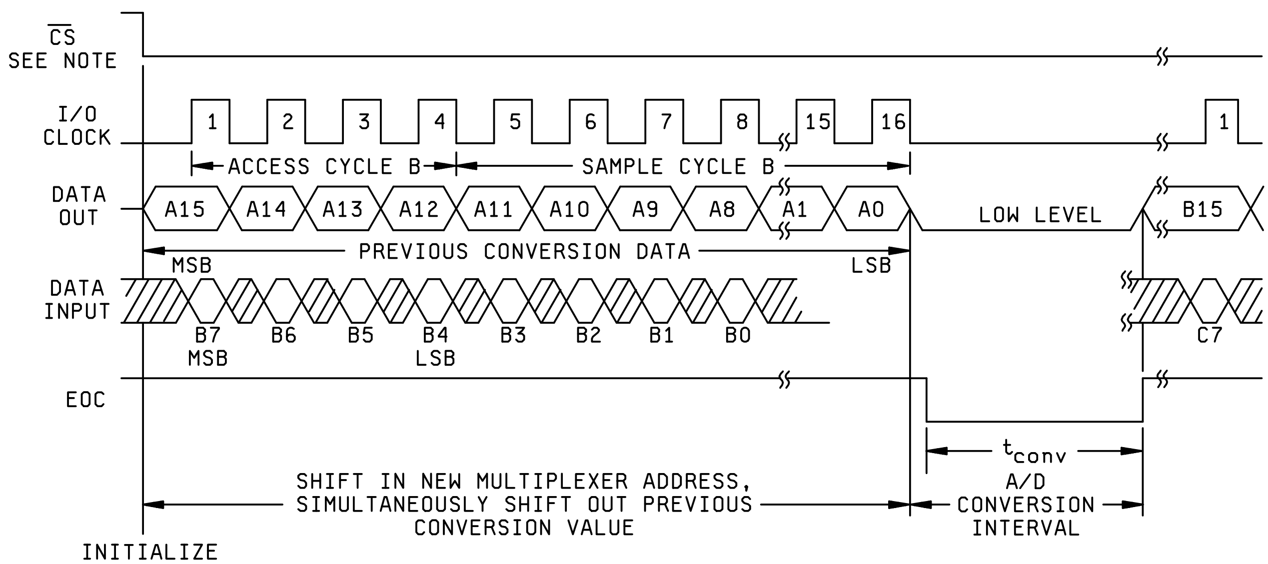
TIMING FOR 8-CLOCK TRANSFER NOT USING $\overline{CS}$ WITH MSB FIRST

NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

FIGURE 5. Timing waveforms - continued.



TIMING FOR 16-CLOCK TRANSFER USING $\overline{CS}$ WITH MSB FIRST



TIMING FOR 16-CLOCK TRANSFER NOT USING $\overline{CS}$ WITH MSB FIRST

NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

FIGURE 5. Timing waveforms - continued.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_I measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 1/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1	1
Group D end-point electrical parameters (see 4.4)	1	1
Group E end-point electrical parameters (see 4.4)	- - -	- - -

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-11-13

Approved sources of supply for SMD 5962-96886 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9688601QRA	01295	TLC2543MJB
5962-9688601QSA	3/	TLC2543MWB
5962-9688601Q2A	3/	TLC2543MFKB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243