

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – LTG	03-02-11	Thomas M. Hess
B	Add footnote <u>15</u> / for test condition of total power supply current (I_{CCT}) to table I. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. – LTG	10-05-14	Thomas M. Hess
C	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. Delete class M requirement throughout. - LTG	16-09-21	Thomas M. Hess



REV																				
SHEET																				
REV	C	C	C	C																
SHEET	15	16	17	18																
REV STATUS OF SHEETS	REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Thanh V. Nguyen	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Thanh V. Nguyen																		
	APPROVED BY Monica L. Poelking	<p align="center">MICROCIRCUIT, DIGITAL, FAST CMOS, 8-BIT DIAGNOSTIC SCAN REGISTER, TTL COMPATIBLE INPUTS AND LIMITED OUTPUT VOLTAGE SWING, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 96-03-22																		
	REVISION LEVEL C	<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-96827</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-96827														
SIZE A	CAGE CODE 67268	5962-96827																	
		SHEET 1 OF 18																	

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}).....	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}).....	-0.5 V dc to $V_{CC} + 0.5$ V dc 4/
DC output voltage range (V_{OUT}).....	-0.5 V dc to $V_{CC} + 0.5$ V dc 4/
DC input clamp current (I_{IK}) ($V_{IN} = -0.5$ V).....	-20 mA
DC output clamp current (I_{OK}) ($V_{OUT} = -0.5$ V and +7.0 V).....	± 20 mA
DC output source current (I_{OH}) (per output).....	-30 mA
DC output sink current (I_{OL}) (per output).....	+70 mA
DC V_{CC} current (I_{CC}).....	± 268 mA
Ground current (I_{GND}).....	+588 mA
Storage temperature range (T_{STG}).....	-65°C to +150°C
Case temperature under bias (T_{BIAS}).....	-65°C to +135°C
Lead temperature (soldering, 10 seconds).....	+300°C
Thermal resistance, junction-to-case (θ_{JC}).....	See MIL-STD-1835
Junction temperature (T_J).....	+175°C
Maximum power dissipation (P_D).....	500 mW

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC}).....	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}).....	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT}).....	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}).....	0.8 V
Minimum high level input voltage (V_{IH}).....	2.0 V
Case operating temperature range (T_C).....	-55°C to +125°C
Maximum input rise or fall rate ($\Delta t/\Delta V$):	
(from $V_{IN} = 0.3$ V to 2.7 V, 2.7 V to 0.3 V).....	5 ns/V
Maximum high level output current (I_{OH}).....	-3 mA
Maximum low level output current (I_{OL}).....	20 mA

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
- 4/ For $V_{CC} \geq 6.5$ V, the upper limit on the range is limited to 7.0 V.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 3

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 4

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 5

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit	
						Min	Max		
High level output voltage 3006	V _{OH1} <u>4/</u>	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND	I _{OH} = -300 μA	All	4.5 V	1, 2, 3	3.0	V _{CC} -0.5	V
	V _{OH2}		I _{OH} = -3 mA				2.4		
Low level output voltage 3007	V _{OL1} <u>4/</u>	For all inputs affecting output under test V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND	I _{OL} = +300 μA	All	4.5 V	1, 2, 3		0.2	V
	V _{OL2}		I _{OL} = +20 mA					0.55	
Negative input clamp voltage 3022	V _{IC}	For input under test, I _{IN} = -18 mA		All	4.5 V	1, 2, 3		-1.2	V
Three-state output leakage current high 3021	I _{OZH} <u>5/ 6/</u>	$\overline{OEY} = 2.0 V$ or 0.8 V For all other inputs V _{IN} = V _{CC} or GND	V _{OUT} = 2.7 V	All	5.5 V	1, 2, 3		10.0	μA
Three-state output leakage current low 3020	I _{OZL} <u>5/ 6/</u>		V _{OUT} = 0.5 V	All	5.5 V	1, 2, 3		-10.0	μA
Input current high 3010	I _{IH1}	For input under test V _{IN} = V _{CC} For all other inputs V _{IN} = V _{CC} or GND		All	5.5 V	1, 2, 3		5.0	μA
	I _{IH2}	For input under test V _{IN} = 2.7 V For all other inputs V _{IN} = V _{CC} or GND		All	5.5 V	1, 2, 3		±1.0	μA
Input current low 3009	I _{IL}	For input under test V _{IN} = 0.5 V For all other inputs V _{IN} = V _{CC} or GND		All	5.5 V	1, 2, 3		±1.0	μA
Power-off leakage current	I _{OFF}	V _{OUT} = 4.5 V		All	0.0 V	1, 2, 3		±1.0	μA
Output short circuit current 3011	I _{OS} <u>7/</u>	For all inputs V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V V _{OUT} = 0.0 V		All	5.5 V	1, 2, 3	-60	-225	mA
Dynamic power supply current	I _{CCD} <u>4/ 8/</u>	Outputs open		All	5.5 V	4, 5, 6		250	μA/ MHz•Bit
Quiescent supply current delta, TTL input level 3005	ΔI _{CC} <u>9/</u>	For input under test V _{IN} = 3.4 V For all other inputs V _{IN} = V _{CC} or GND		All	5.5 V	1, 2, 3		2.0	mA

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
C

5962-96827

SHEET
6

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified		Device type	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
							Min	Max	
Quiescent supply current, outputs high 3005	I _{CCH}	$\overline{OEY} = \text{GND}$ For all other inputs V _{IN} = V _{CC} or GND		All	5.5 V	1, 2, 3		1.5	mA
Quiescent supply current, outputs low 3005	I _{CCL}			All	5.5 V	1, 2, 3		1.5	mA
Quiescent supply current, outputs disabled 3005	I _{CCZ} <u>5/</u>	$\overline{OEY} = V_{CC}$ For all other inputs V _{IN} = V _{CC} or GND		All	5.5 V	1, 2, 3		1.5	mA
Total supply current	I _{CC1} <u>10/ 15/</u>	Outputs open f _{CP} = 10 MHz $\overline{OEY} = \text{GND}$ One bit toggling f _i = 5 MHz 50% duty cycle For nonswitching input V _{IN} = V _{CC} or GND	For switching Inputs V _{IN} = V _{CC} or GND	All	5.5 V	4, 5, 6		5.3	mA
			For switching Inputs V _{IN} = 3.4 V or GND			4, 5, 6		7.3	
	I _{CC2} <u>4/ 10/ 15/</u>	Outputs open f _{CP} = 10 MHz $\overline{OEY} = \text{GND}$ Eight bits and four controls toggling f _i = 5 MHz 50% duty cycle For nonswitching input V _{IN} = V _{CC} or GND	For switching Inputs V _{IN} = V _{CC} or GND	All	5.5 V	4, 5, 6		17.8	
			For switching Inputs V _{IN} = 3.4 V or GND			4, 5, 6		30.8	
Input capacitance 3012	C _{IN} <u>11/</u>	T _C = +25°C See 4.4.1b		All	GND	4		10.0	pF
Output capacitance 3012	C _{OUT} <u>11/</u>			All	GND	4		12.0	pF
Low level ground bounce noise	V _{OLP} <u>11/ 12/</u>	V _{IH} = 3.0 V, V _{IL} = 0.0 V T _A = +25°C See 4.4.1d See figure 4		All	5.0 V	4		1750	mV
	V _{OLV} <u>11/ 12/</u>					4		-1100	
High level V _{CC} bounce noise	V _{OHP} <u>11/ 12/</u>			All	5.0 V	4		800	mV
	V _{OHV} <u>11/ 12/</u>					4		-1200	
Functional test 3014	<u>13/</u>	V _{IH} = 2.0 V, V _{IL} = 0.8 V Verify output V _O See 4.4.1c		All	4.5 V	7, 8	L	H	
					5.5 V	7, 8	L	H	

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
C

5962-96827

SHEET
7

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _c ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Propagation delay time, PCLK to Y _n 3003	t _{PLH1} , t _{PHL1} <u>14/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	All	4.5 V	9, 10, 11	2.0	12.0	ns
Propagation delay time, MODE to SDO 3003	t _{PLH2} , t _{PHL2} <u>14/</u>		All	4.5 V	9, 10, 11	2.0	18.0	ns
Propagation delay time, SDI to SDO 3003	t _{PLH3} , t _{PHL3} <u>14/</u>		All	4.5 V	9, 10, 11	2.0	18.0	ns
Propagation delay time, DCLK to SDO 3003	t _{PLH4} , t _{PHL4} <u>14/</u>		All	4.5 V	9, 10, 11	2.0	30.0	ns
Propagation delay time, output enable, \overline{OEY} to Y _n 3003	t _{PZH1} <u>14/</u>		All	4.5 V	9, 10, 11	3.0	20.0	ns
	t _{PZL1} <u>14/</u>					9, 10, 11	3.0	
Propagation delay time, output enable, DCLK to D _n 3003	t _{PZH2} <u>14/</u>		All	4.5 V	9, 10, 11	3.0	30.0	ns
	t _{PZL2} <u>14/</u>					9, 10, 11	3.0	
Propagation delay time, output disable, \overline{OEY} to Y _n 3003	t _{PHZ1} <u>14/</u>		All	4.5 V	9, 10, 11	3.0	30.0	ns
	t _{PLZ1} <u>14/</u>					9, 10, 11	3.0	
Propagation delay time, output disable, DCLK to D _n 3003	t _{PHZ2} <u>14/</u>		All	4.5 V	9, 10, 11	3.0	90.0	ns
	t _{PLZ2} <u>14/</u>					9, 10, 11	3.0	
Setup time, high or low, D _n to PCLK	t _{s1} <u>14/</u>		All	4.5 V	9, 10, 11	6.0		ns
Setup time, high or low MODE to PCLK	t _{s2} <u>14/</u>		All	4.5 V	9, 10, 11	15.0		ns
Setup time, high or low, Y _n to DCLK	t _{s3} <u>14/</u>		All	4.5 V	9, 10, 11	5.0		ns
Setup time, high or low, MODE to DCLK	t _{s4} <u>14/</u>	All	4.5 V	9, 10, 11	12.0		ns	
Setup time, high or low, SDI to DCLK	t _{s5} <u>14/</u>	All	4.5 V	9, 10, 11	10.0		ns	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 8

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _c ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Setup time, high or low, DCLK to PCLK	t _{s6} <u>14/</u>	C _L = 50 pF minimum R _L = 500Ω See figure 5	All	4.5 V	9, 10, 11	15.0		ns
Setup time, high or low, PCLK to DCLK	t _{s7} <u>14/</u>		All	4.5 V	9, 10, 11	45.0		ns
Hold time, high or low, D _n to PCLK	t _{h1} <u>14/</u>		All	4.5 V	9, 10, 11	2.0		ns
Hold time, high or low, MODE to PCLK	t _{h2} <u>14/</u>		All	4.5 V	9, 10, 11	0.0		ns
Hold time, high or low, Y _n to DCLK	t _{h3} <u>14/</u>		All	4.5 V	9, 10, 11	5.0		ns
Hold time, high or low, MODE to DCLK	t _{h4} <u>14/</u>		All	4.5 V	9, 10, 11	5.0		ns
Hold time, high or low, SDI to DCLK	t _{h5} <u>14/</u>		All	4.5 V	9, 10, 11	0.0		ns
PCLK pulse width, high or low	t _{w1} <u>14/</u>		All	4.5 V	9, 10, 11	15.0		ns
DCLK pulse width, high or low	t _{w2} <u>14/</u>		All	4.5 V	9, 10, 11	25.0		ns

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at 4.5 V ≤ V_{CC} ≤ 5.5 V.

4/ This parameter is guaranteed, if not tested, to the limits specified in table I herein.

5/ Three-state output conditions are required.

6/ This test may be performed using V_{IH} = 3.0 V. When V_{IH} = 3.0 V is used, the test is guaranteed for V_{IH} = 2.0 V.

7/ Not more than one output should be tested at a time. The duration of the test should not exceed one second.

8/ I_{CCD} may be verified by the following equation:

$$I_{CCD} = \frac{I_{CCT} - I_{CC} - D_H N_T \Delta I_{CC}}{f_{CP}/2 + f_i N_i}$$

where I_{CCT}, I_{CC} (I_{CL} or I_{CH} in table I), and ΔI_{CC} shall be the measured values of these parameters, for the device under test, when tested as described in table I, herein. The values for D_H, N_T, f_{CP}, f_i, and N_i shall be as listed in the test conditions column for I_{CCT} in table I, herein.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 9

TABLE I. Electrical performance characteristics - Continued.

9/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1 \text{ V}$ (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 2.0 mA; and the preferred method and limits are guaranteed.

10/ I_{CCT} is calculated as follows:

$$I_{CCT} = I_{CC} + D_H N_T \Delta I_{CC} + I_{CCD}(f_{CP}/2 + f_i N_i)$$

where

I_{CC} = Quiescent supply current (any I_{CCL} or I_{CCH})

D_H = Duty cycle for TTL inputs at 3.4 V

N_T = Number of TTL inputs at 3.4 V

ΔI_{CC} = Quiescent supply current delta, TTL inputs at 3.4 V

I_{CCD} = Dynamic power supply current caused by an input transition pair (HLH or LHL)

f_{CP} = Clock frequency for registered devices ($f_{CP} = 0$ for nonregistered devices)

f_i = Input frequency

N_i = Number of inputs at f_i

11/ This test is required only for group A testing; see 4.4.1 herein.

12/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL} . V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH} .

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH} . V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL} .

13/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. For outputs, $L < 1.5 \text{ V}$, $H \geq 1.5 \text{ V}$.

14/ AC limits at $V_{CC} = 5.5 \text{ V}$ are equal to the limits at $V_{CC} = 4.5 \text{ V}$ and guaranteed by testing at $V_{CC} = 4.5 \text{ V}$. Minimum propagation delay time limits for $V_{CC} = 4.5 \text{ V}$ and 5.5 V are guaranteed, if not tested, to the limits specified in table I, herein. For propagation delay tests, all paths must be tested.

15/ For I_{CC} test in an ATE environment, the effect of parasitic output capacitive loading from the test environment must be taken into account, as its effect is not intended to be included in the test results. The impact must be characterized and appropriate offset factors must be applied to the test result.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 10

Device type	All				
Case outlines	L	3	Case outlines	L	3
Terminal number	Terminal symbol	Terminal symbol	Terminal number	Terminal symbol	Terminal symbol
1	\overline{OEY}	NC	15	Y ₇	NC
2	DCLK	\overline{OEY}	16	Y ₆	PCLK
3	D ₀	DCLK	17	Y ₅	SDO
4	D ₁	D ₀	18	Y ₄	Y ₇
5	D ₂	D ₁	19	Y ₃	Y ₆
6	D ₃	D ₂	20	Y ₂	Y ₅
7	D ₄	D ₃	21	Y ₁	Y ₄
8	D ₅	NC	22	Y ₀	NC
9	D ₆	D ₄	23	MODE	Y ₃
10	D ₇	D ₅	24	V _{CC}	Y ₂
11	SDI	D ₆	25	---	Y ₁
12	GND	D ₇	26	---	Y ₀
13	PCLK	SDI	27	---	MODE
14	SDO	GND	28	---	V _{CC}

NC = No internal connection.

Terminal descriptions	
Terminal symbol	Description
D _n (n = 0 to 7)	Parallel data inputs to the pipeline register or parallel data outputs from the shadow register
DCLK	Diagnostics clock input for loading shadow register
PCLK	Pipeline register clock input loads D-port or shadow register contents on low-to-high transition
MODE	Control input for pipeline register multiplexer and shadow register control
\overline{OEY}	Output enable control input for Y-port (active low)
SDI	Serial data input to shadow register
SDO	Serial data output from shadow register
Y _n (n = 0 to 7)	Data outputs from the pipeline register or parallel inputs to the shadow register

FIGURE 1. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 11

Inputs				Outputs			Operation
MODE	SDI	DCLK	PCLK	SDO	Shadow register	Pipeline register	
L	X	↑	X	S ₇	S ₀ ← SDI S _n ← S _{n-1}	NA	Serial shift; D ₇ -D ₀ outputs disabled
L	X	X	↑	S ₇	NA	P _n ← D _n	Load pipeline register from data inputs
H	L	↑	X	L	S _n ← Y _n	NA	Load shadow register from Y _n outputs
H	H	↑	X	H	Hold	NA	Hold shadow register; D ₇ -D ₀ outputs enabled
H	X	X	↑	SDI	NA	P _n ← S _n	Load pipeline register from shadow register

H = High voltage level

L = Low voltage level

X = Irrelevant

↑ = Low-to-high clock transition

S_n (n = 7 to 0) = Shadow register outputs

P_n (n = 7 to 0) = Pipeline register outputs

NA = Not applicable; output is not a function of the specified input combinations

FIGURE 2. Truth table.

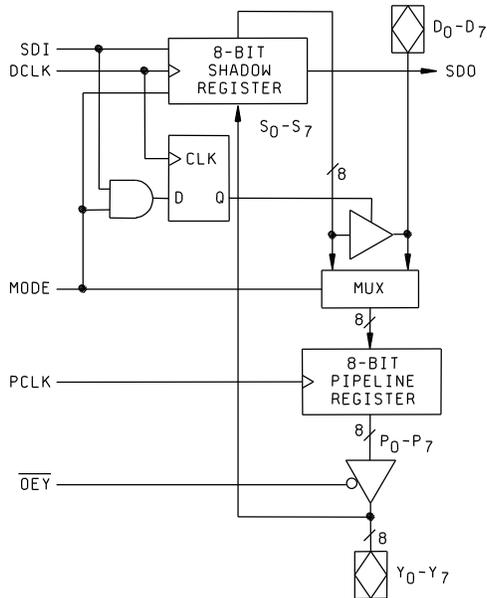


FIGURE 3. Logic diagram.

**STANDARD
MICROCIRCUIT DRAWING**

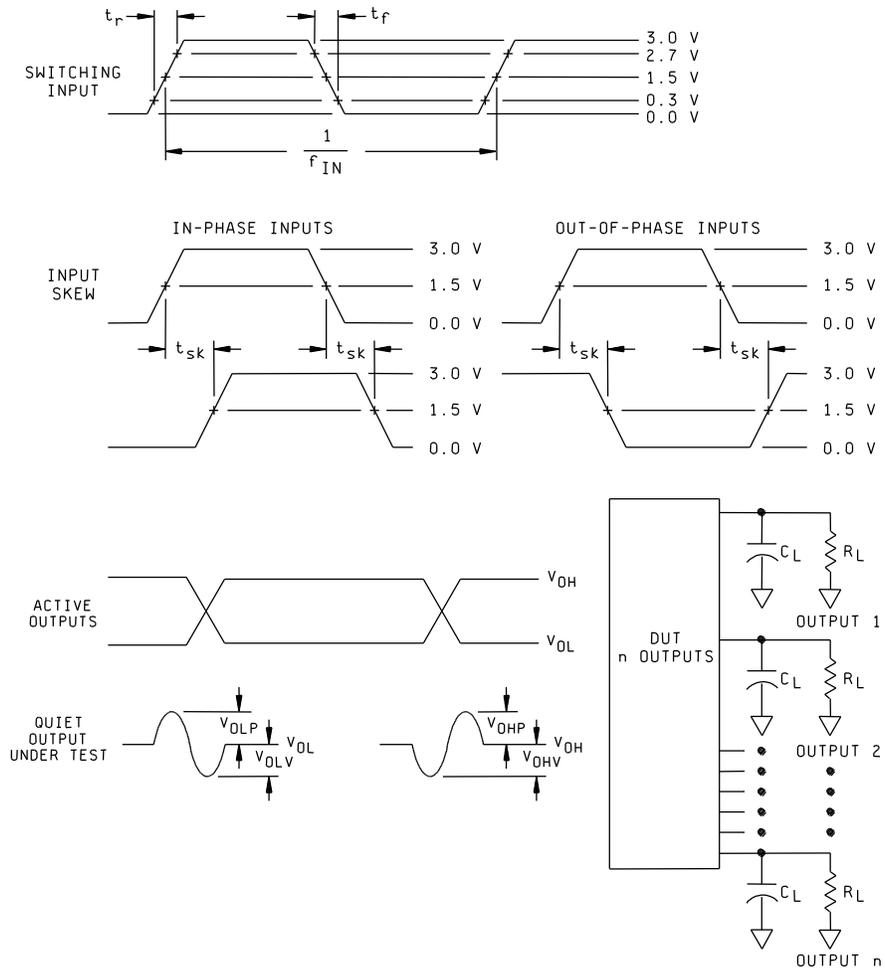
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-96827

REVISION LEVEL
C

SHEET
12



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. $R_L = 450\Omega \pm 1$ percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
 - a. $V_{IN} = 0.0$ V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
 - b. $t_r, t_f = 3$ ns ± 1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f , the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ± 1.0 ns tolerance and guaranteeing the results at 3.0 ns ± 1.0 ns; skew between any two switching inputs signals (t_{sk}) ≤ 250 ps.

FIGURE 4. Ground bounce load circuit and waveforms.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 13

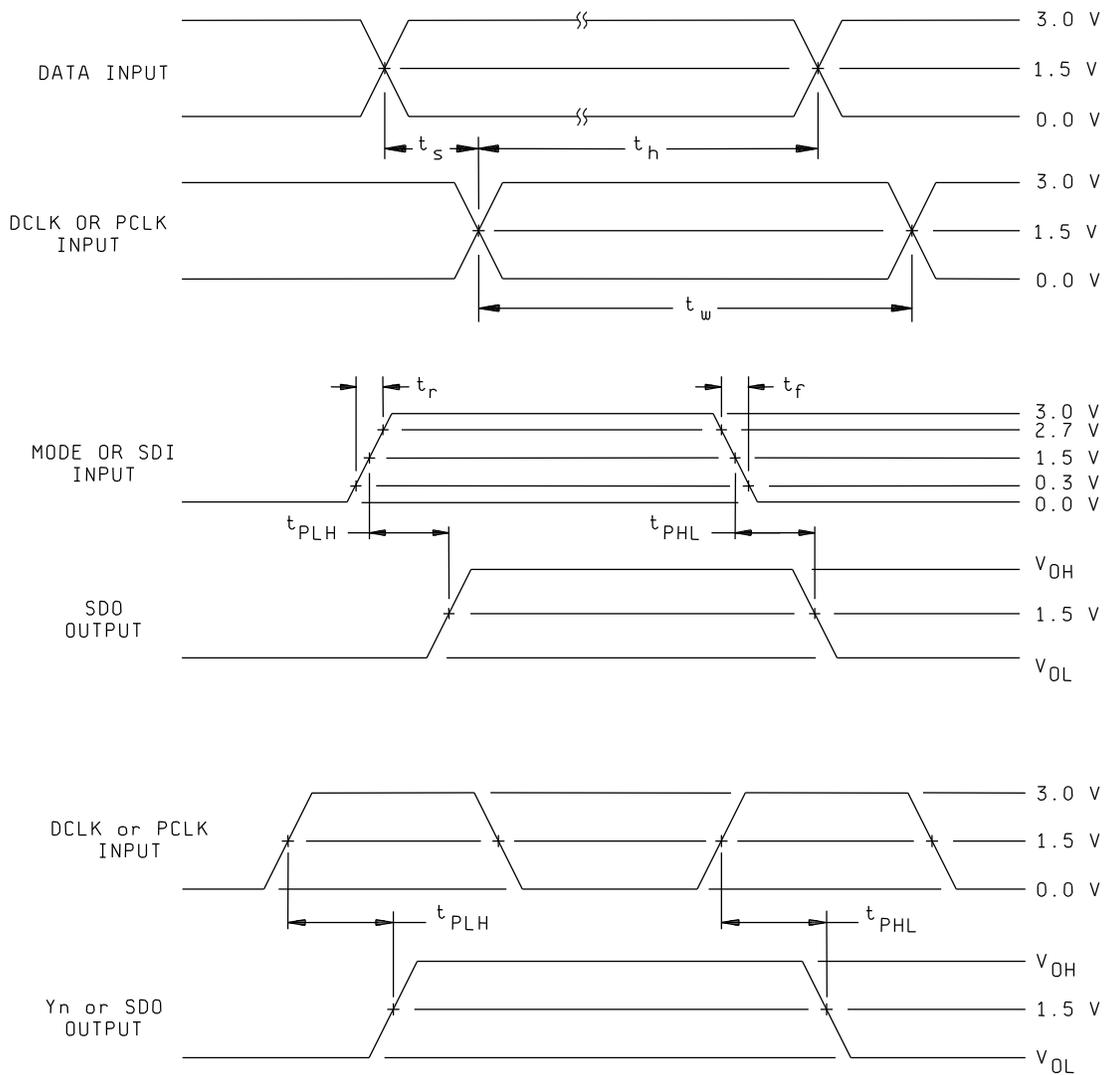


FIGURE 5. Switching waveforms and test circuit.

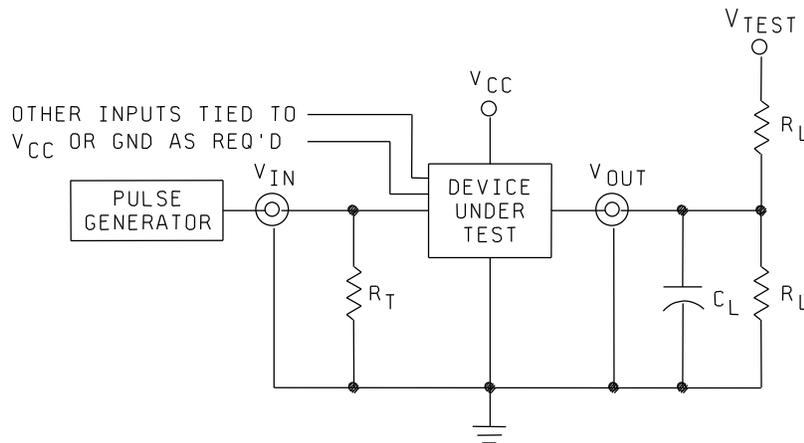
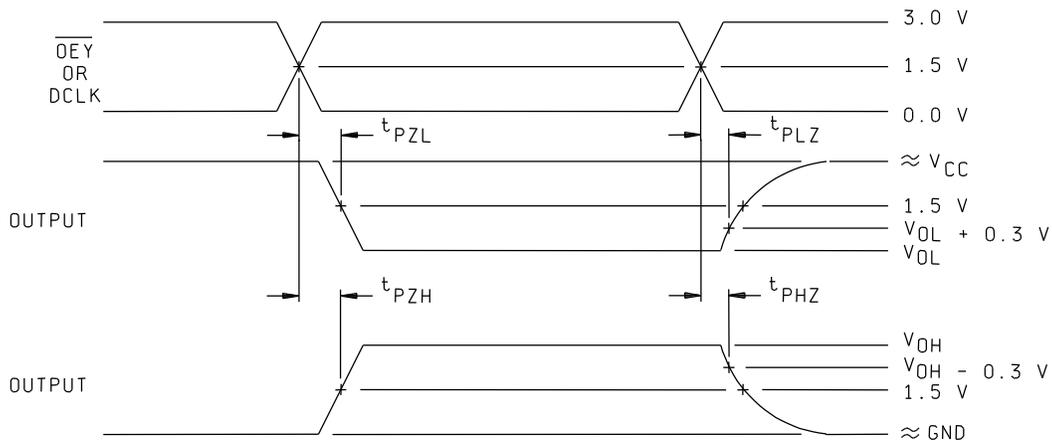
**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-96827

REVISION LEVEL
C

SHEET
14



NOTES:

1. When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 7.0 \text{ V}$.
2. When measuring t_{PHZ} , t_{PZH} , t_{PLH} , and t_{PHL} : $V_{TEST} = \text{open}$.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is low at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is high at V_{OH} except when disabled by the output enable control.
4. $C_L = 50 \text{ pF}$ minimum or equivalent (includes test jig and probe capacitance).
5. $R_L = 500\Omega$ or equivalent.
6. $R_T = 50\Omega$ or equivalent.
7. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $PRR \leq 10 \text{ MHz}$; $t_r \leq 2.5 \text{ ns}$; $t_f \leq 2.5 \text{ ns}$; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V , respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 15

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{OUT} , test all applicable pins on five devices with zero failures.

For C_{IN} and C_{OUT} , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types that by design will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the C_{IN} and C_{OUT} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results for each device tested.

- c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 16

d. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP} , V_{OLV} , V_{OHP} , and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DLA Land and Maritime-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP} , V_{OLV} , V_{OHP} , and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DLA Land and Maritime-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DLA Land and Maritime-VA data from testing on both fixtures that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP} , V_{OLV} , V_{OHP} , and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For V_{OLP} , V_{OLV} , V_{OHP} , and V_{OHV} , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types that by design will yield the same test values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the V_{OLP} , V_{OLV} , V_{OHP} , and V_{OHV} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results, along with the oscilloscope plots, for each device tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 4, 7, 9	1, 4, 7, 9

1/ PDA applies to subgroups 1 and 4 (i.e., I_{CCT} only).

2/ PDA applies to subgroups 1, 4, and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 17

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-96827
		REVISION LEVEL C	SHEET 18

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-09-21

Approved sources of supply for SMD 5962-96827 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply a <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9682701QLA	01295	CY29FCT818ATDMB
5962-9682701Q3A	<u>3/</u>	CY29FCT818ATLMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE
number

Vendor name
and address

01295

Texas Instruments Incorporated
Semiconductor Group
8505 Forest Ln.
P.O. Box 660199
Dallas, TX 75243

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