| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Change in accordance with the notice of revision 5962-R349-97. - jak | 97-06-27 | Monica L. Poelking |
| B | Incorporate previous Notice Of Revision (NOR). Update the boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - jak | 09-01-21 | Charles F. Saffle |
| C | Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. Delete class M requirement throughout. - LTG | 15-03-25 | Thomas M. Hess |

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | |
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| SHEET | | | | | | | | | | | | | | | | | | | |
| REV STATUS | REV | C | C | C | C | C | C | C | C | C | C | C | C | C | C |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
Joseph A. Kerby

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
96-03-13

REVISION LEVEL
C

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**http://www.landandmaritime.dla.mil**

MICROCIRCUIT, DIGITAL, ADVANCED HIGH-SPEED CMOS, QUADRUPLE 2-INPUT POSITIVE-NAND GATE, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

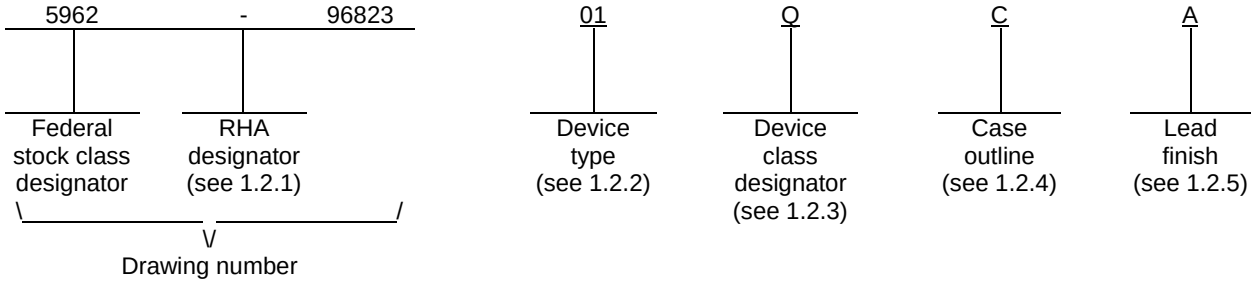
| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-96823** |

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54AHCT00 | Quadruple 2-input positive-NAND gate, TTL compatible inputs |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| C | GDIP1-T14 or CDIP2-T14 | 14 | Dual-in-line |
| D | GDFP1-F14 or CDFP2-F14 | 14 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range ($V_{CC}$) ..... -0.5 V dc to +7.0 V dc
DC input voltage range ($V_{IN}$) ..... -0.5 V dc to +7.0 V dc 4/
DC output voltage range ($V_{OUT}$) ..... -0.5 V dc to $V_{CC}$ +0.5 V dc 4/
DC input clamp current ($I_{IK}$) ($V_{IN}$ < 0.0 V) ..... -20 mA
DC output clamp current ($I_{OK}$) ($V_{OUT}$ < 0.0 V or $V_{OUT}$ > $V_{CC}$) ..... ±20 mA
Continuous output current ($I_O$) ($V_{OUT}$ = 0 V to $V_{CC}$) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Maximum power dissipation at $T_A$ = +55°C (instill air) ($P_D$) ..... 500 mW
Storage temperature range ($T_{STG}$) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case ($\Theta_{JC}$) ..... See MIL-STD-1835
Junction temperature ($T_J$) ..... +175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range ($V_{CC}$) ..... +4.5 V dc to +5.5 V dc
Minimum high level input voltage ($V_{IH}$) ..... +2.0 V
Maximum low level input voltage ($V_{IL}$) ..... +0.8 V
Input voltage range ($V_{IN}$) ..... +0.0 V dc to +5.5 V dc
Output voltage range ($V_{OUT}$) ..... +0.0 V dc to $V_{CC}$
Maximum high level output current ($I_{OH}$) ..... -8 mA
Maximum low level output current ($I_{OL}$) ..... +8 mA
Minimum input rise or fall rate ($\Delta t/\Delta V$) ..... +20 ns/V
Case operating temperature range ($T_C$) ..... -55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device, Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of -55°C to +125°C.

4/ The input and output voltage ratings may be exceeded providing that the input and output current ratings are observed.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD7 - Standard for Description of 54/74HCXXXXX and 54/74HCTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S Arlington, VA 22201-2107).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ -55°C ≤ $T_C$ ≤ +125°C +4.5 V ≤ $V_{CC}$ ≤ +5.5 V unless otherwise specified | | $V_{CC}$ | Group A subgroups | Limits 3/ Min | Limits 3/ Max | Unit |
|---|---|---|---|---|---|---|---|---|
| High level output voltage 3006 | $V_{OH}$ | For all inputs affecting outputs under test, $V_{IN}$ = $V_{IH}$ = 2.0 V or $V_{IL}$ = 0.8 V For all other inputs, $V_{IN}$ = $V_{CC}$ or GND | $I_{OH}$ = -50 μA | 4.5 V | 1, 2, 3 | 4.4 | | V |
| | | | $I_{OH}$ = -8 mA | | 1 | 3.94 | | |
| | | | | | 2, 3 | 3.8 | | |
| Low level output voltage 3007 | $V_{OL}$ | For all inputs affecting outputs under test, $V_{IN}$ = $V_{IH}$ = 2.0 V or $V_{IL}$ = 0.8 V For all other inputs, $V_{IN}$ = $V_{CC}$ or GND | $I_{OL}$ = +50 μA | 4.5 V | 1, 2, 3 | | 0.1 | V |
| | | | $I_{OL}$ = +8 mA | | 1 | | 0.36 | |
| | | | | | 2, 3 | | 0.44 | |
| Input current high 3010 | $I_{IH}$ | For input under test, $V_{IN}$ = $V_{CC}$ For all other inputs, $V_{IN}$ = $V_{CC}$ or GND | | 5.5 V | 1 | | +0.1 | μA |
| | | | | | 2, 3 | | +1.0 | |
| Input current low 3009 | $I_{IL}$ | For input under test, $V_{IN}$ = GND For all other inputs, $V_{IN}$ = $V_{CC}$ or GND | | 5.5 V | 1 | | -0.1 | μA |
| | | | | | 2, 3 | | -1.0 | |
| Quiescent supply current, 3005 | $I_{CC}$ | For all inputs, $V_{IN}$ = $V_{CC}$ or GND $I_{OUT}$ = 0.0 A | | 5.5 V | 1 | | 2.0 | μA |
| | | | | | 2, 3 | | 20.0 | |
| Quiescent supply current delta, TTL input levels | $\Delta I_{CC}$ 4/ | One input at 3.4 V Other inputs $V_{CC}$ or GND | | 5.5 V | 1 | | 1.35 | mA |
| | | | | | 2, 3 | | 1.5 | |
| Input capacitance 3012 | $C_{IN}$ | $T_C$ = +25°C, $V_{IN}$ = $V_{CC}$ or GND See 4.4.1c | | 5.0 V | 4 | | 8.0 | pF |
| Power dissipation capacitance | $C_{PD}$ 5/ | $C_L$ = 50 pF minimum f = 1 MHz, See 4.4.1c | | 5.0 V | 4 | | 11.5 | pF |
| Low level ground bounce noise | $V_{OLP}$ 6/ | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0.0 V $T_A$ = +25°C See 4.4.1d See figure 4 | | 5.0 V | 4 | | 1750 | mV |
| | $V_{OLV}$ 6/ | | | 5.0 V | 4 | | -1750 | |
| High level $V_{CC}$ bounce noise | $V_{OHP}$ 6/ | | | 5.0 V | 4 | | 750 | mV |
| | $V_{OHV}$ 6/ | | | 5.0 V | 4 | | -750 | |
| Functional tests 3014 | 7/ | $V_{IH}$ = 2.0 V or $V_{IL}$ = 0.8 V Verify output $V_O$ See 4.4.1b | | 4.5 V and 5.5 V | 7, 8 | L | H | |
| Propagation delay time, mA or mB to mY 3003 | $t_{PLH}$ 9/ | $C_L$ = 15 pF minimum See figure 5 8/ | | 4.5 V and 5.5 V | 9 | | 6.9 | ns |
| | | | | | 10, 11 | 1.0 | 8.0 | |
| | | $C_L$ = 50 pF minimum See figure 5 | | 4.5 V and 5.5 V | 9 | | 7.9 | ns |
| | | | | | 10, 11 | 1.0 | 9.0 | |
| | $t_{PHL}$ 9/ | $C_L$ = 15 pF minimum See figure 5 8/ | | 4.5 V and 5.5 V | 9 | | 6.9 | ns |
| | | | | | 10, 11 | 1.0 | 8.0 | |
| | | $C_L$ = 50 pF minimum See figure 5 | | 4.5 V and 5.5 V | 9 | | 7.9 | ns |
| | | | | | 10, 11 | 1.0 | 9.0 | |

See footnotes on next sheet.

TABLE I. Electrical performance characteristics – Continued.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. $\Delta I_{CC}$) utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all $I_{CC}$ tests, the output terminals shall be open. When performing the $I_{CC}$ tests, the current meter shall be placed in the circuit such that all current flows through the meter

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). Classes Q and V shall use the or preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times the $\Delta I_{CC}$ maximum; and the preferred method and limits are guaranteed.

5/ Power dissipation capacitance ($C_{PD}$) determines the power consumption ($P_D$) and the current consumption ($I_S$).
Where:

$P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n x d x \Delta I_{CC} x V_{CC})$

$I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + (n x d x \Delta I_{CC})$

f is the frequency of the input signal; n is the number of device inputs at TTL levels; and d is the duty cycle of the signal, and $C_L$ is the external output load capacitance.

6/ This test is for qualification only. Ground and $V_{CC}$ bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested that, whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from $V_{CC}$ to ground. The device manufacturer shall determine the values of these decoupling capacitors. The low and high level ground and $V_{CC}$ bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal $V_{OH}$ level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at $V_{OH}$ as all other outputs possible are switched from $V_{OH}$ to $V_{OL}$. $V_{OHV}$ and $V_{OHP}$ are then measured from the nominal $V_{OH}$ level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from $V_{OL}$ to $V_{OH}$.

The device inputs shall be conditioned such that all outputs are at a low nominal $V_{OL}$ level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at $V_{OL}$ as all other outputs possible are switched from $V_{OL}$ to $V_{OH}$. $V_{OLP}$ and $V_{OLV}$ are then measured from the nominal $V_{OL}$ level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from $V_{OH}$ to $V_{OL}$.

7/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances per MIL-STD-883 may be incorporated. For outputs, $L \leq 0.8$ V, $H \geq 2.0$ V.

8/ This parameter shall be guaranteed, if not tested, to the limits in table I, herein.

9/ For propagation delay tests, all paths must be tested.

| Device type | 01 | |
|---|---|---|
| Case outlines | C, D | 2 |
| Terminal number | Terminal symbol | Terminal symbol |
| 1 | 1A | NC |
| 2 | 1B | 1A |
| 3 | 1Y | 1B |
| 4 | 2A | 1Y |
| 5 | 2B | NC |
| 6 | 2Y | 2A |
| 7 | GND | NC |
| 8 | 3Y | 2B |
| 9 | 3A | 2Y |
| 10 | 3B | GND |
| 11 | 4Y | NC |
| 12 | 4A | 3Y |
| 13 | 4B | 3A |
| 14 | $V_{CC}$ | 3B |
| 15 | | NC |
| 16 | | 4Y |
| 17 | | NC |
| 18 | | 4A |
| 19 | | 4B |
| 20 | | $V_{CC}$ |

NC = No internal connection

| Terminal descriptions | |
|---|---|
| Terminal symbol | Description |
| mA (m = 1 to 4) | Data inputs, A |
| mB (m = 1 to 4) | Data inputs, B |
| mY (m = 1 to 4) | Data outputs |

FIGURE 1. Terminal connections.

(Each gate)

| Input | | Output |
|---|---|---|
| mA | mB | mY |
| H | H | L |
| L | X | H |
| X | L | H |

H = High voltage level
L = Low voltage level
X = Irrelevant

FIGURE 2. Truth table.

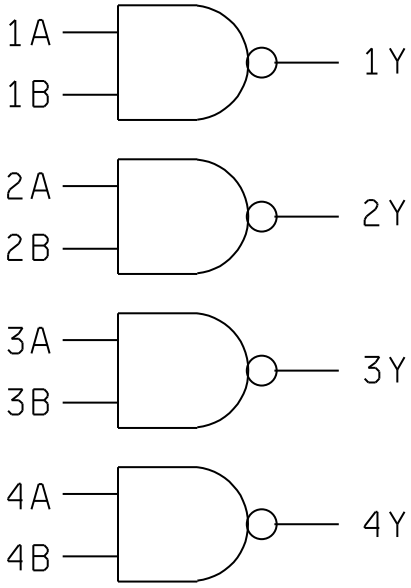
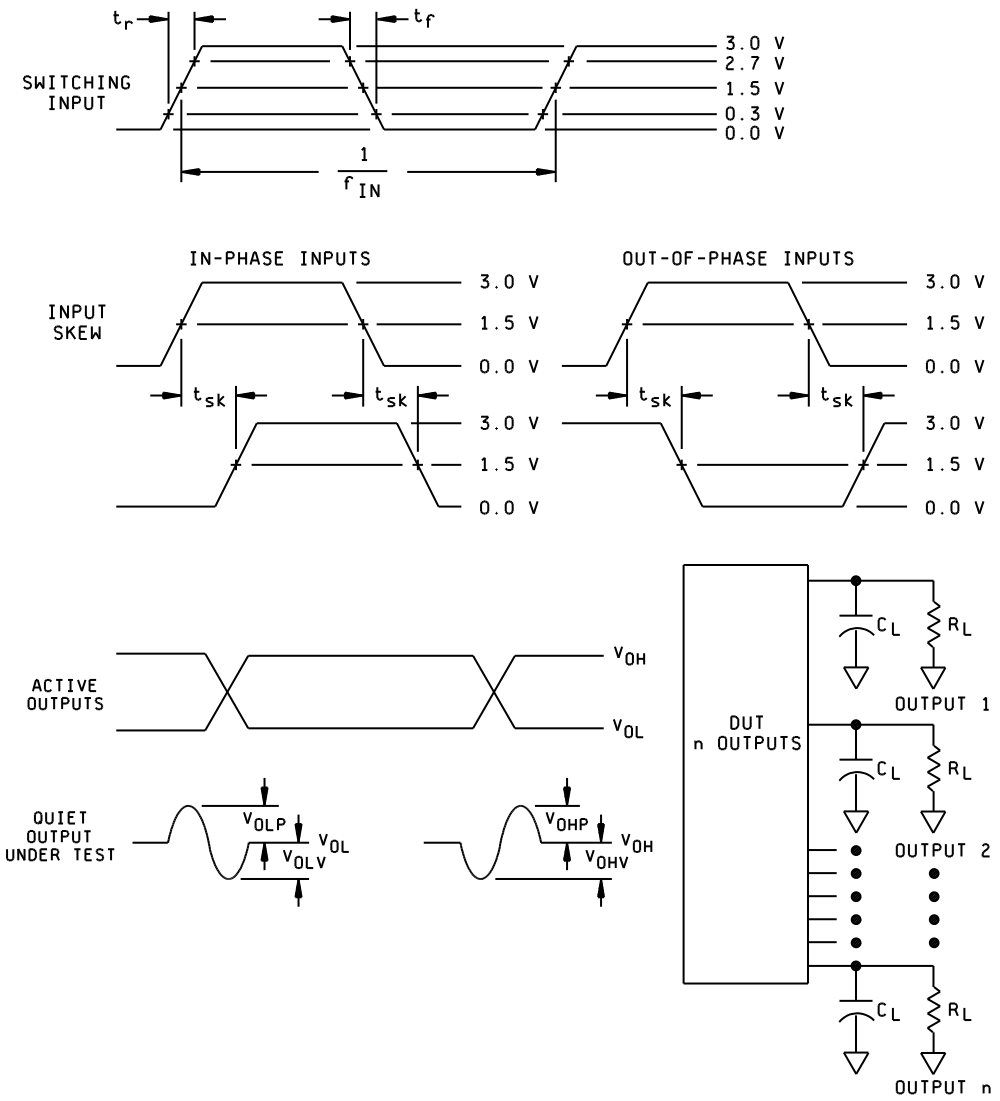


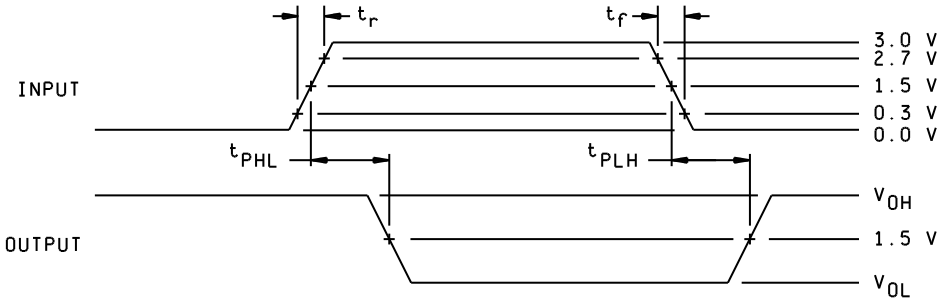

FIGURE 3. Logic diagram.

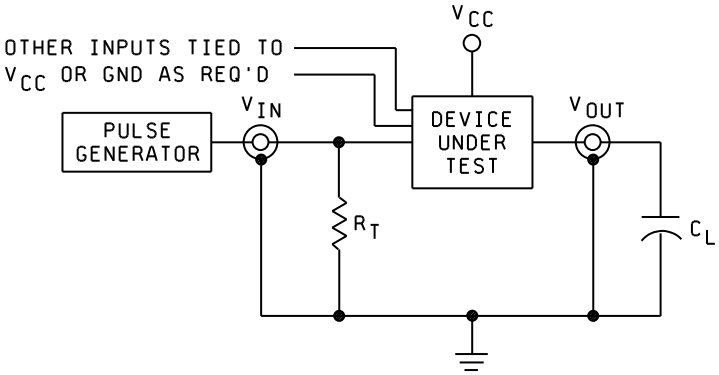



NOTES:

1. $C_L$ includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. $R_L$ = 5.0 kΩ ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. $V_{IN}$ = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq$ 1 MHz.
   b. $t_r$, $t_f$ = 3.0 ns ±1.0 ns. For input signal generators incapable of maintaining these values of $t_r$ and $t_f$, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching input signals ($t_{sk}$) ≤ 250 ps.

FIGURE 4. Ground bounce waveforms and test circuit.




NOTES:

1. $C_L$ per table I (includes test jig and probe capacitance).
2. $R_T$ = 50Ω or equivalent.
3. Input signal from pulse generator: $V_{IN}$ = 0.0 V to 3.0 V; PRR ≤ 1 MHz; $t_r$ = 3.0 ns; $t_f$ = 3.0 ns; $t_r$ and $t_f$ shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. $C_{IN,}$ and $C_{PD}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. $C_{IN}$ and $C_{OUT}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. The DC bias for the pin under test ($V_{BIAS}$) = 2.5 V or 3.0 V. For $C_{IN}$ and $C_{PD}$, test all applicable pins on five devices with zero failures.

For $C_{IN}$ a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the $C_{IN}$ test. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturer shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results for each device tested.

d. Ground and $V_{CC}$ bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DLA Land and Maritime-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DLA Land and Maritime-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DLA Land and Maritime-VA data from testing on both fixtures that shall include all measured peak values for each device tested and detailed oscilloscope plots for each $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For $V_{OHP}$, $V_{OHV}$, $V_{OLP}$, and $V_{OLV}$, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the $V_{OHP}$, $V_{OHV}$, $V_{OLP}$, and $V_{OLV}$ tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturer shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results, along with the oscilloscope plots, for each device tested.

TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|
| | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | 1 |
| Final electrical parameters (see 4.2) | 1/ 1, 2, 3, 7, 8, 9, 10, 11 | 2/ 1, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3, 7, 8, 9, 10, 11 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-03-25

Approved sources of supply for SMD 5962-96823 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9682301QCA | 01295 | SNJ54AHCT00J |
| 5962-9682301QDA | 01295 | SNJ54AHCT00W |
| 5962-9682301Q2A | 01295 | SNJ54AHCT00FK |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments Inc.<br>Semiconductor Group<br>8505 Forest Ln.<br>P.O. Box 660199<br>Dallas, TX 75243<br>Point of contact: U.S. Highway 75 South<br>P.O. Box 84, M/S 853<br>Sherman, TX 75090-9493 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.