REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change the device name to reflect the Bus Hold feature, and adjust limits to characterize the performance of the optimized die. Editorial changes throughout. - CFS	99-03-12	Monica L. Poelking
B	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	09-05-01	Thomas M. Hess
C	Update high and low voltage (V_{OH} and V_{OL}) test condition V_{IH} and V_{IL} limits to table I. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. Delete class M requirement throughout. - LTG	15-09-23	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29					

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
96-02-01

REVISION LEVEL
C

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, 3.3-VOLT SCAN TEST DEVICE WITH 18-BIT UNIVERSAL BUS TRANSCEIVER, WITH BUS HOLD, THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

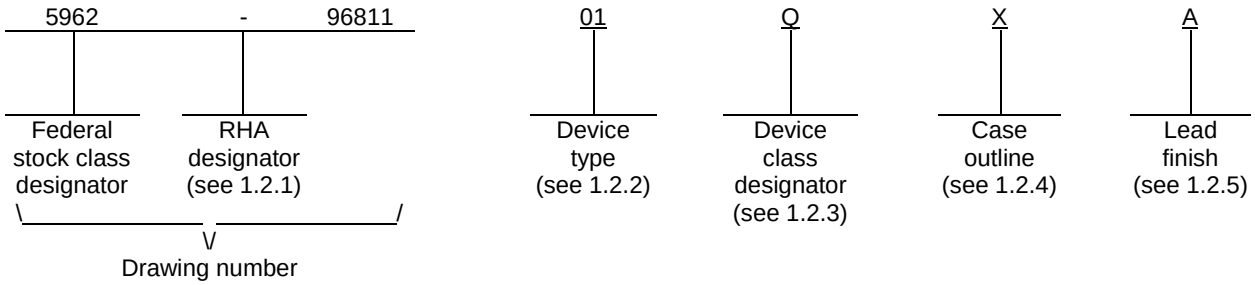
SIZE	CAGE CODE	
A	**67268**	**5962-96811**

SHEET 1 OF 29

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54LVTH18502A	3.3-volt scan test device with 18-bit universal bus transceiver, with bus hold, three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See Figure 1	68	Ceramic quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +4.6 V dc
DC input voltage range (V_{IN})	-0.5 V dc to +7.0 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to +7.0 V dc 4/
DC output current (I_{OL}) (per output)	+96 mA
DC output current (I_{OH}) (per output)	+48 mA 5/
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V)	-50 mA
DC output clamp current (I_{OK}) (V_{OUT} < 0.0 V)	-50 mA
Maximum Power Dissipation (P_D)	346 mW 6/
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	1.9°C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/ 7/

Supply voltage range (V_{CC})	+2.7 V dc to +3.6 V dc
Input voltage range (V_{IN})	0.0 V dc to +5.5 V dc
Output voltage range (V_{OUT})	0.0 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	+2.0 V dc
Maximum low level input voltage (V_{IL})	+0.8 V dc
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+48 mA
Maximum input rise or fall rate (outputs enabled) ($\Delta t/\Delta v$)	10 ns/V
Case operating temperature range (T_C)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ The input and output negative voltage ratings may be exceeded provided that the input and output clamp current ratings are observed.

5/ This current flows only when the output is in the high state and $V_{OUT} > V_{CC}$.

6/ Power dissipation values are derived using the formula $P_D = V_{CC}I_{CC} + nV_{OL}I_{OL}$, where V_{CC} and I_{OL} are as specified in 1.4 above, I_{CC} and V_{OL} are as specified in table I herein, and n represents the total number of outputs.

7/ Unused inputs must be held high or low to prevent them from floating.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The block or logic diagram shall be as specified on figure 4.

3.2.5 Test access port controller and scan test registers. The test access port (TAP) controller and scan registers shall be as specified on figure 5.

3.2.6 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 6.

3.2.7 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+2.7\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified		Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
							Min	Max	
Negative input clamp voltage 3022	V_{IK}	For input under test, I_{IN} = -18 mA		All	2.7 V	1,2,3		-1.2	V
High level output voltage 3006	V_{OH1}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ I_{OH} = -100 µA		All	2.7 V and 3.6 V	1,2,3	V_{CC} - 0.2		V
	V_{OH2}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ I_{OH} = -3 mA		All	2.7 V	1,2,3	2.4		
	V_{OH3}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ I_{OH} = -8 mA		All	3.0 V	1,2,3	2.4		
	V_{OH4}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ I_{OH} = -24 mA		All	3.0 V	1,2,3	2.0		
Low level output voltage 3007	V_{OL1}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ I_{OL} = +100 µA		All	2.7 V	1,2,3		0.2	V
	V_{OL2}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ I_{OL} = +24 mA		All	2.7 V	1,2,3		0.5	
	V_{OL3}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ I_{OL} = +16 mA		All	3.0 V	1,2,3		0.4	
	V_{OL4}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ I_{OL} = +32 mA		All	3.0 V	1,2,3		0.5	
	V_{OL5}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ I_{OL} = +48 mA		All	3.0 V	1,2,3		0.55	
Input current high 3010	I_{IH} 4/	For input under test, V_{IN} = 5.5 V	m$\overline{OEAB}$, m$\overline{OEBA}$, TDI, TMS	All	3.6 V	1,2,3		5.0	µA
			mAn or mBn ports		3.6 V			20.0	
			mCLKAB, Mclkba mLEAB, mLEBA, TCK		0.0 V and 3.6 V			10.0	
		For input under test, $V_{IN} = V_{CC}$	mCLKAB, mCLKBA mLEAB, mLEBA, TCK		3.6 V	1,2,3		+1.0	
			mAn or mBn ports		3.6 V	1,2,3		+1.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+2.7\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified		Device type	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Input current low 3009	I_{IL} 4/	For input under test V_{IN} = GND	m$\overline{OEAB}$, m$\overline{OEBA}$, TDI, TMS	All	3.6 V	1,2,3		-100.0	µA
			mAn or mBn ports		3.6 V			-5.0	
			mCLKAB, mCLKBA, mLEAB, mLEBA, TCK		3.6 V			-1.0	
Input bus hold current	I_{HOLD} 4/	A or B ports	V_{IN} = 0.8 V	All	3.0 V	1,2,3	75.0	500.0	µA
			V_{IN} = 2.0 V				-75.0	-500.0	
Three-state output leakage current high 3021	I_{OZH} 5/ 6/	V_{OUT} = 3.0 V		All	3.6 V	1,2,3		1.0	µA
Three-state output leakage current low 3020	I_{OZL} 5/ 6/	V_{OUT} = 0.5 V		All	3.6 V	1,2,3		-1.0	µA
Three-state output current, power-up	I_{OZPU} 5/ 6/	V_{OUT} = 0.5 V to 3.0 V		All	0.0 V to 1.5 V	1,2,3		±50.0	µA
Three-state output current, power-down	I_{OZPD} 5/ 6/	V_{OUT} = 0.5 V to 3.0 V		All	1.5 V to 0.0 V	1,2,3		±50.0	µA
Quiescent supply current 3005	I_{CC}	For all inputs $V_{IN} = V_{CC}$ or GND I_{OUT} = 0.0 A	Outputs high	All	3.6 V	1,2,3		3.0	mA
			Outputs low					30.0	
			Outputs disabled					3.0	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 7/	For input under test $V_{IN} = V_{CC}$ - 0.6 V For all other inputs $V_{IN} = V_{CC}$ or GND		All	3.0 V and 3.6 V	1,2,3		0.5	mA
Low level ground bounce noise	V_{OLP} 8/	V_{IH} = 2.7 V, V_{IL} = 0.0 V T_A = +25°C See figure 6 See 4.4.1d		All	3.0 V	4		650	mV
Low level ground bounce noise	V_{OLV} 8/			All	3.0 V	4		-900	
High level V_{CC} bounce noise	V_{OHP} 8/			All	3.0 V	4		1350	
High level V_{CC} bounce noise	V_{OHV} 8/			All	3.0 V	4		-1450	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+2.7\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Input capacitance 3012	C_{IN}	T_C = +25°C, See 4.4.1c V_{IN} = 3.0 V or 0.0 V	All	3.0 V	4		11.0	pF
I/O capacitance	$C_{I/O}$	T_C = +25°C, See 4.4.1c V_{OUT} = 3.0 V or 0.0 V	All	3.0 V	4		23.0	
Output capacitance	C_{OUT}	T_C = +25°C, See 4.4.1c V_{OUT} = 3.0 V or 0.0 V	All	3.0 V	4		9.0	
Functional test 3014	9/	V_{IN} = 0.8 V or 2.0 V Verify output V_O See 4.4.1b	All	2.7 V and 3.6 V	7,8	L	H	
NORMAL MODE								
Clock frequency, mCLKAB or mCLKBA	f_{CLK1}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	0	80	MHz
				3.0 V and 3.6 V		0	90	
Pulse width, mCLKAB or mCLKBA high or low	t_{w1}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	5.8		ns
				3.0 V and 3.6 V		4.6		
Pulse width, mLEAB or mLEBA high	t_{w2}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	3.2		ns
				3.0 V and 3.6 V		3.2		
Setup time, high or low, mAn before mCLKAB↑ or mBn before mCLKBA↑	t_{s1}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	3.2		ns
				3.0 V and 3.6 V		3.0		
Setup time, high or low mAn before mLEAB↓ or mBn before mLEBA↓, CLK high	t_{s2}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	1.1		ns
				3.0 V and 3.6 V		1.6		
Setup time, high or low, mAn before mLEAB↓ or mBn before mLEBA↓, CLK low	t_{s3}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	1.8		ns
				3.0 V and 3.6 V		1.8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+2.7\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Hold time, high or low, mAn after mCLKAB↑ or mBn after mCLKBA↑	t_{h1}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	1.1		ns
				3.0 V and 3.6 V		1.4		
Hold time, high or low, mAn after mLEAB↓ or mBn after mLEBA↓	t_{h2}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	4.2		ns
				3.0 V and 3.6 V		3.4		
Maximum mCLKAB or mCLKBA frequency	f_{MAX1}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	80		MHz
				3.0 V and 3.6 V		90		
Propagation delay time, mAn to mBn, or mBn to mAn 3003	t_{PLH1} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		5.8	ns
				3.0 V and 3.6 V		1.1	5.1	
	t_{PHL1} 10/		All	2.7 V	9,10,11		5.8	
				3.0 V and 3.6 V		1.3	5.2	
Propagation delay time, mCLKAB to mBn, or mCLKBA to mAn 3003	t_{PLH2} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		7.2	ns
				3.0 V and 3.6 V		1.1	6.7	
	t_{PHL2} 10/		All	2.7 V	9,10,11		7.2	
				3.0 V and 3.6 V		1.5	6.7	
Propagation delay time, mLEAB to mBn, or mLEBA to mAn 3003	t_{PLH3} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		9.3	ns
				3.0 V and 3.6 V		1.5	7.8	
	t_{PHL3} 10/		All	2.7 V	9,10,11		7.0	
				3.0 V and 3.6 V		1.3	6.7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+2.7\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, output enable m$\overline{OEAB}$ to mBn or m$\overline{OEBA}$ to mAn 3003	t_{PZH1} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		8.8	ns
				3.0 V and 3.6 V		1.0	8.2	
	t_{PZL1} 10/		All	2.7 V	9,10,11		9.1	
				3.0 V and 3.6 V		1.5	8.1	
Propagation delay time, output disable, m$\overline{OEAB}$ to mBn or m$\overline{OEBA}$ to mAn 3003	t_{PHZ1} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		10.0	ns
				3.0 V and 3.6 V		2.3	9.3	
	t_{PLZ1} 10/		All	2.7 V	9,10,11		9.2	
				3.0 V and 3.6 V		2.0	9.0	
TEST MODE								
Clock frequency, TCK	f_{CLK2}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	0	40	MHz
				3.0 V and 3.6 V		0	50	
Pulse width, TCK high or low	t_{w3}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	10.5		ns
				3.0 V and 3.6 V		9.5		
Setup time, high or low, mAn, mBn, mCLKAB, mCLKBA, mLEAB, mLEBA, m$\overline{OEAB}$, or m$\overline{OEBA}$, before TCK↑	t_{s4}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	7.1		ns
				3.0 V and 3.6 V		6.7		
Setup time, high or low, TDI before TCK↑	t_{s5}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	3.5		ns
				3.0 V and 3.6 V		2.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+2.7\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Setup time, high or low, TMS before TCK↑	t_{s6}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	3.5		ns
				3.0 V and 3.6 V		2.5		
Hold time, high or low, mAn, mBn, mCLKAB, mCLKBA, mLEAB, mLEBA, m$\overline{OEAB}$, or m$\overline{OEBA}$, after TCK↑	t_{h3}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	1.0		ns
				3.0 V and 3.6 V		1.5		
Hold time, high or low, TDI after TCK↑	t_{h4}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	1.0		ns
				3.0 V and 3.6 V		1.5		
Hold time, high or low, TMS after TCK↑	t_{h5}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	1.0		ns
				3.0 V and 3.6 V		1.5		
Maximum TCK frequency	f_{MAX2}	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11	40		MHz
				3.0 V and 3.6 V		50		
Propagation delay time, TCK↓ to mAn, or mBn 3003	t_{PLH4} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		18.0	ns
				3.0 V and 3.6 V		1.6	15.0	
	t_{PHL4} 10/		All	2.7 V	9,10,11		18.0	
				3.0 V and 3.6 V		2.5	15.0	
Propagation delay time, TCK↓ to TDO 3003	t_{PLH5} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		7.0	ns
				3.0 V and 3.6 V		1.0	6.0	
	t_{PHL5} 10/		All	2.7 V	9,10,11		9.0	
				3.0 V and 3.6 V		1.0	8.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+2.7\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, output enable, TCK↓ to mAn, or mBn 3003	t_{PZH2} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		21.0	ns
				3.0 V and 3.6 V		3.0	19.0	
	t_{PZL2} 10/		All	2.7 V	9,10,11		21.0	
				3.0 V and 3.6 V		3.2	18.0	
Propagation delay time, output enable, TCK↓ to TDO 3003	t_{PZH3} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		7.0	ns
				3.0 V and 3.6 V		1.0	6.0	
	t_{PZL3} 10/		All	2.7 V	9,10,11		7.0	
				3.0 V and 3.6 V		1.5	6.0	
Propagation delay time, output disable, TCK↓ to mAn, or mBn 3003	t_{PHZ2} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		21.0	ns
				3.0 V and 3.6 V		2.6	19.0	
	t_{PLZ2} 10/		All	2.7 V	9,10,11		19.5	
				3.0 V and 3.6 V		3.6	18.0	
Propagation delay time, output disable, TCK↓ to TDO 3003	t_{PHZ3} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 7	All	2.7 V	9,10,11		9.0	ns
				3.0 V and 3.6 V		1.5	7.5	
	t_{PLZ3} 10/		All	2.7 V	9,10,11		8.5	
				3.0 V and 3.6 V		1.5	7.5	

See footnotes on next sheet.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilized the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, $V_{IN} \leq 0.8$ V or ≥ 2.0 V.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ For I/O ports, the limit includes I_{OZH} or I_{OZL} leakage current from the output circuitry.

5/ For I/O ports, the limit includes I_{IH} or I_{IL} leakage current from the output circuitry.

6/ This parameter shall be guaranteed, if not tested, to the limits specified in table I herein, when performed with control inputs that affect the state of the output under test at $V_{IN} = 0.8$ V or 2.0 V.

7/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 0.6$ V (alternate method). When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 0.2 mA, and the preferred method and limits are guaranteed.

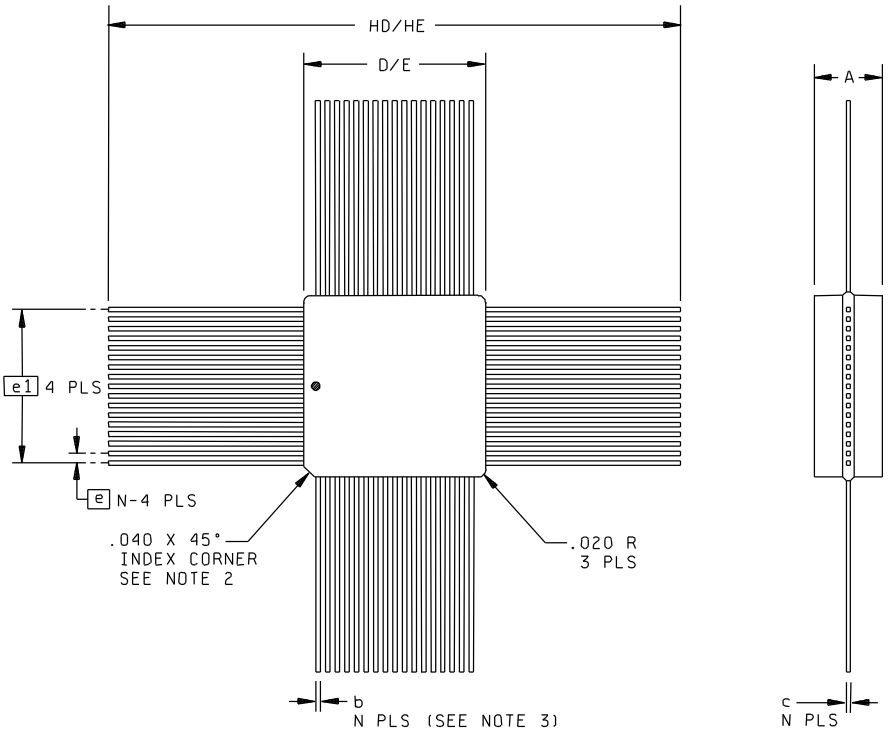
8/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 6). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 6). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 6). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, $V_{IL} = 0.4$ V and $V_{IH} = 2.4$ V. For outputs, $L \leq 0.8$ V, $H \geq 2.0$ V.

10/ For propagation delay tests, test all functions of each input and output.



Dimension	Millimeters		Inches	
	Min	Max	Min	Max
HD/HE	33.02	38.10	1.300	1.500
D/E	12.32	12.70	.485	.500
A	3.404	3.912	.134	.154
b	0.203	0.330	.008	.013
e	0.635 BSC		.025 BSC	
e1	10.160 BSC		.400 BSC	
c	0.127	0.178	.005	.007
N	68		68	

NOTES:

1. The US government preferred system of measurement is the metric SI system. However, this item is originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. A terminal 1 identification mark shall be located on the first side clockwise from the index corner. Terminal numbers shall increase in a counterclockwise direction when viewed as shown.
3. N is the maximum number of terminals.

FIGURE 1. Case outline.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	35	NC
2	V_{CC}	36	V_{CC}
3	TDO	37	TCK
4	1CLKAB	38	2CLKBA
5	1LEAB	39	2LEBA
6	GND	40	GND
7	$1\overline{OEAB}$	41	$2\overline{OEBA}$
8	1A1	42	2B9
9	1A2	43	2B8
10	1A3	44	2B7
11	1A4	45	2B6
12	1A5	46	2B5
13	GND	47	GND
14	1A6	48	2B4
15	1A7	49	2B3
16	1A8	50	2B2
17	1A9	51	2B1
18	NC	52	NC
19	V_{CC}	53	V_{CC}
20	2A1	54	1B9
21	2A2	55	1B8
22	2A3	56	1B7
23	GND	57	GND
24	2A4	58	1B6
25	2A5	59	1B5
26	2A6	60	1B4
27	2A7	61	1B3
28	2A8	62	1B2
29	2A9	63	1B1
30	GND	64	GND
31	$2\overline{OEAB}$	65	$1\overline{OEBA}$
32	2LEAB	66	1LEBA
33	2CLKAB	67	1CLKBA
34	TDI	68	TMS

NC = No internal connection

Terminal descriptions	
Terminal symbol	Description
mAn (m = 1 to 2, n = 1 to 9)	A-bus input/output ports
mBn (m = 1 to 2, n = 1 to 9)	B-bus input/output ports
$m\overline{OEAB}$, $m\overline{OEBA}$ (m = 1 to 2)	A-to B/B-to-A output enable control inputs
mLEAB, mLEBA (m = 1 to 2)	A-to-B/B-to-A latch enable inputs
mCLKAB, mCLKBA (m = 1 to 2)	A-to-B/B-to-A clock inputs
TDI	Test data input
TDO	Test data output
TMS	Test mode select input
TCK	Test clock input

FIGURE 2. Terminal connections.

Normal mode, each register 1/

Inputs				Outputs
m$\overline{\text{OEAB}}$	mLEAB	mCLKAB	mAn	mBn
L	L	L	X	B_0
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = Disabled
↑= Low-to-high clock transition.
B_0 = The output level of B before the indicated steady-state input conditions were established.

1/ mAn-to-mBn data flow is shown. mBn-to-mAn data flow is similiar but uses m$\overline{\text{OEBA}}$, mLEBA, and mCLKBA.

FIGURE 3. Truth table.

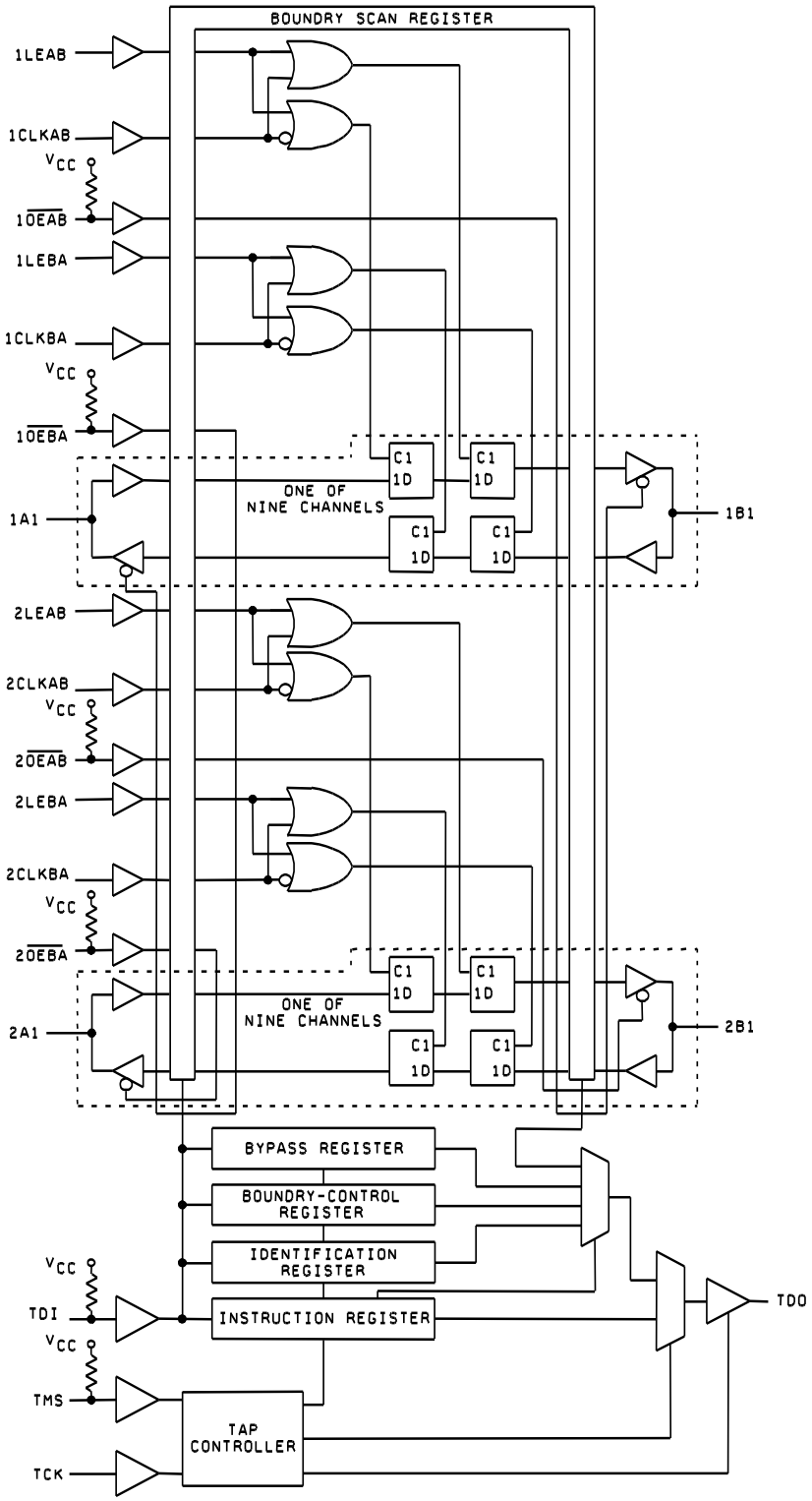


FIGURE 4. Logic diagram.

Test access port (TAP) controller state diagram

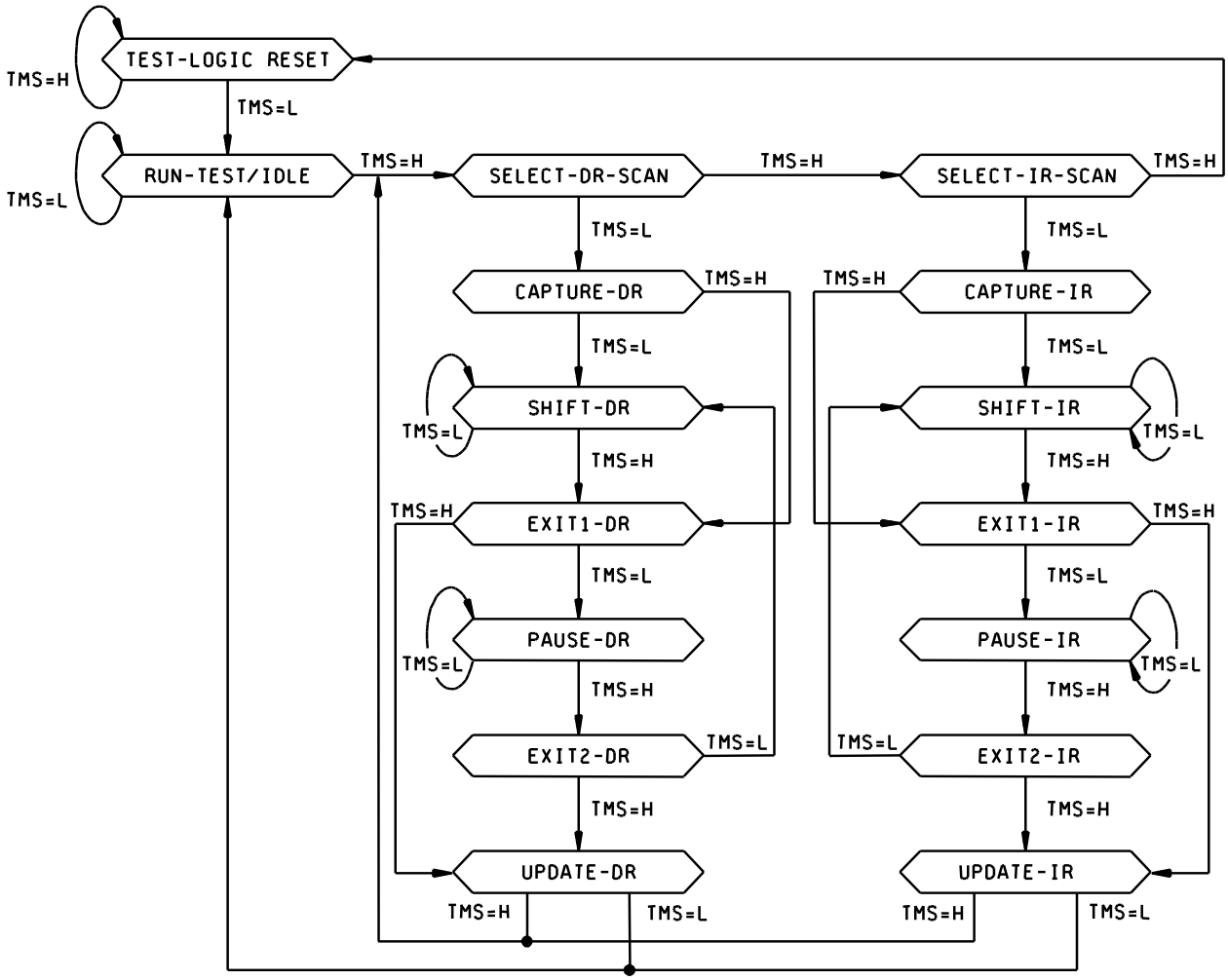
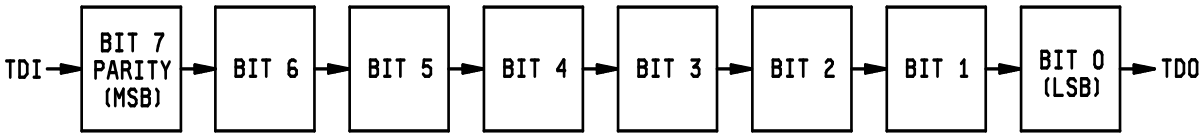


FIGURE 5. Test access port controller and scan test registers.

Instruction register (IR) order of scan



NOTE: During capture-IR, the IR captures the binary value 10000001. At power up or in the test-logic-reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction.

Instruction-Register Opcodes

BINARY CODE 1/ BIT 7→BIT 0 MSB→LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	IDCODE	Identification read	Device identification	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	BYPASS 2/	Bypass scan	Bypass	Normal
10000100	BYPASS 2/	Bypass scan	Bypass	Normal
00000101	BYPASS 2/	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS 2/	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

1/ Bit 7 is used to maintain even parity in the 8-bit instruction.
2/ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the device.

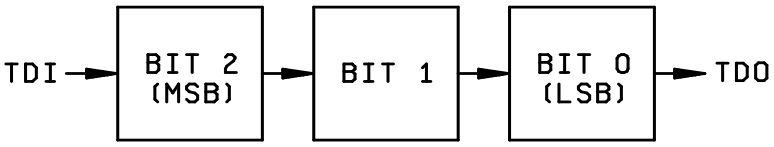
FIGURE 5. Test access port controller and scan test registers - Continued.

Boundary-scan register (BSR) configuration

BSR bit number	Device signal	BSR bit number	Device signal	BSR bit number	Device signal
47	$2\overline{OEAB}$	35	2A9-I/O	17	2B9-I/O
46	$1\overline{OEAB}$	34	2A8-I/O	16	2B8-I/O
45	$2\overline{OEBA}$	33	2A7-I/O	15	2B7-I/O
44	$1\overline{OEBA}$	32	2A6-I/O	14	2B6-I/O
43	2CLKAB	31	2A5-I/O	13	2B5-I/O
42	1CLKAB	30	2A4-I/O	12	2B4-I/O
41	2CLKBA	29	2A3-I/O	11	2B3-I/O
40	1CLKBA	28	2A2-I/O	10	2B2-I/O
39	2LEAB	27	2A1-I/O	9	2B1-I/O
38	1LEAB	26	1A9-I/O	8	1B9-I/O
37	2LEBA	25	1A8-I/O	7	1B8-I/O
36	1LEBA	24	1A7-I/O	6	1B7-I/O
---		23	1A6-I/O	5	1B6-I/O
---		20	1A5-I/O	4	1B5-I/O
---		21	1A4-I/O	3	1B4-I/O
---		20	1A3-I/O	2	1B3-I/O
---		19	1A2-I/O	1	1B2-I/O
---		18	1A1-I/O	0	1B1-I/O

NOTE: The source data to be captured into the BSR during capture-DR is determined by the current instruction. The contents of the BSR can change during run-test/idle as determined by the current instruction. At power up or in test-logic-reset, BSCs 47 through 44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the output would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

Boundary-control register order of scan



NOTE: During capture-DR (DR stands for data register), the contents of the BCR are not changed. At power up or in the test-logic-reset state, the BCR is reset to the binary value 010, which selects the PSA test operation.

FIGURE 5. Test access port controller and scan test registers - Continued.

Boundary-control-register-opcodes

BINARY CODE BIT 2→BIT 0 MSB→LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/36-bit mode (PRPG)
X10	Parallel-signature analysis/36-bit mode (PSA)
011	Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT)

Bypass register order of scan

NOTE: During capture-DR, the bypass register captures a logic 0.

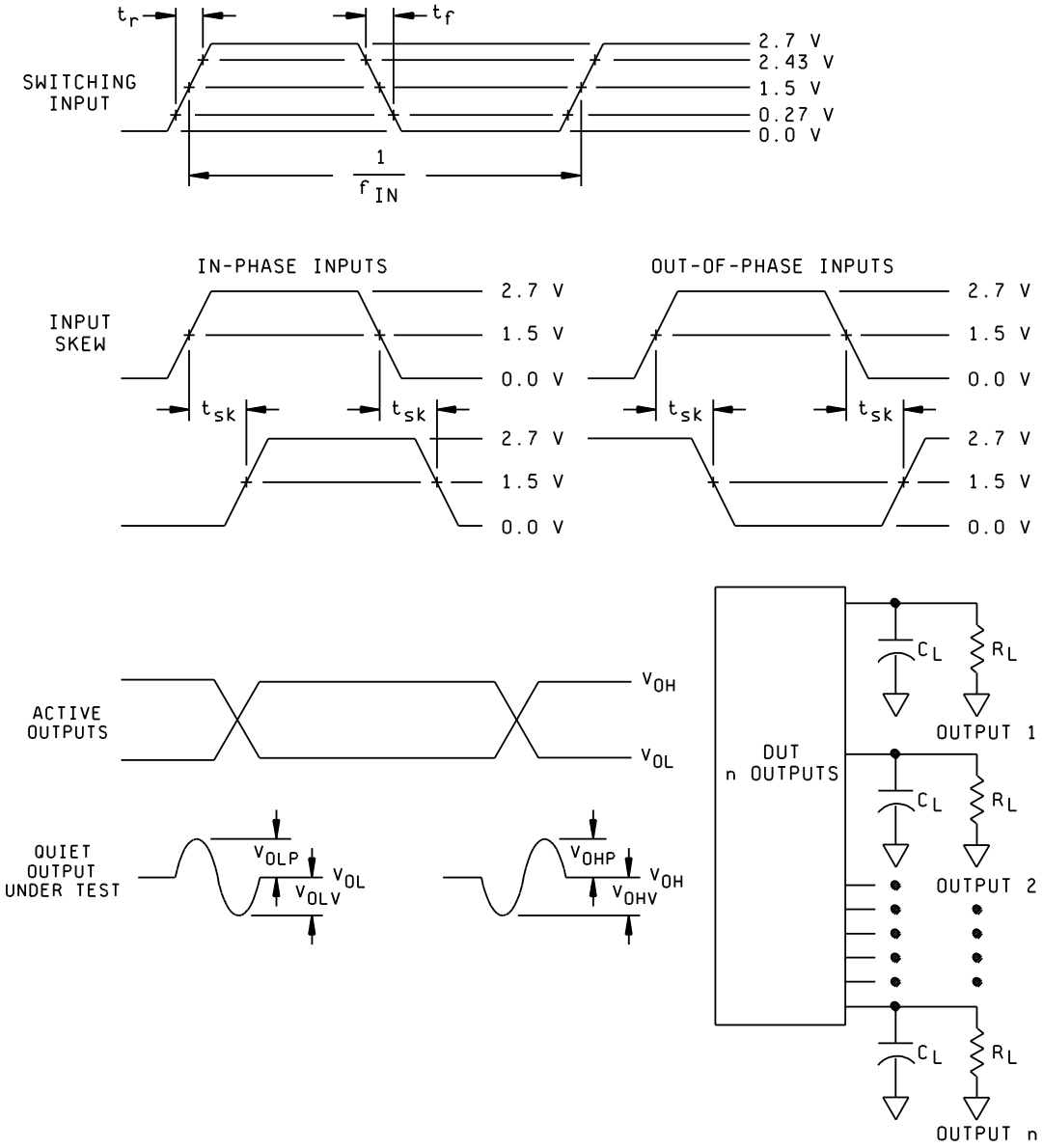
Device identification register (IDR) configuration

IDR bit number	Identification significance	IDR bit number	Identification significance	IDR bit number	Identification significance 1/
31	VERSION3	27	PARTNUMBER15	11	MANUFACTURER10
30	VERSION2	26	PARTNUMBER14	10	MANUFACTURER09
29	VERSION1	25	PARTNUMBER13	9	MANUFACTURER08
28	VERSION0	24	PARTNUMBER12	8	MANUFACTURER07
---	---	23	PARTNUMBER11	7	MANUFACTURER06
---	---	22	PARTNUMBER10	6	MANUFACTURER05
---	---	21	PARTNUMBER09	5	MANUFACTURER04
---	---	20	PARTNUMBER08	4	MANUFACTURER03
---	---	19	PARTNUMBER07	3	MANUFACTURER02
---	---	18	PARTNUMBER06	2	MANUFACTURER01
---	---	17	PARTNUMBER05	1	MANUFACTURER00
---	---	16	PARTNUMBER04	0	LOGIC1
---	---	15	PARTNUMBER03	---	---
---	---	14	PARTNUMBER02	---	---
---	---	13	PARTNUMBER01	---	---
---	---	12	PARTNUMBER00	---	---

1/ For TI products, bits 11-0 of the device identification register always contain the binary value 000000101111 (02F, hex)

NOTE: During capture-DR, the binary value 00000000000000011100000000101111 (0001C02F, hex) is captured in the device identification register to identify this device as Texas Instruments SNJ54LVT18502.

FIGURE 5. Test access port controller and scan test registers - Continued.



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 2.7 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. t_r, t_f = 2.7 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 2.7 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 2.7 ns ±1.0 ns; skew between any two switching inputs signals (t_{sk}) ≤ 250 ps.

FIGURE 6. Ground bounce test circuit and waveforms.

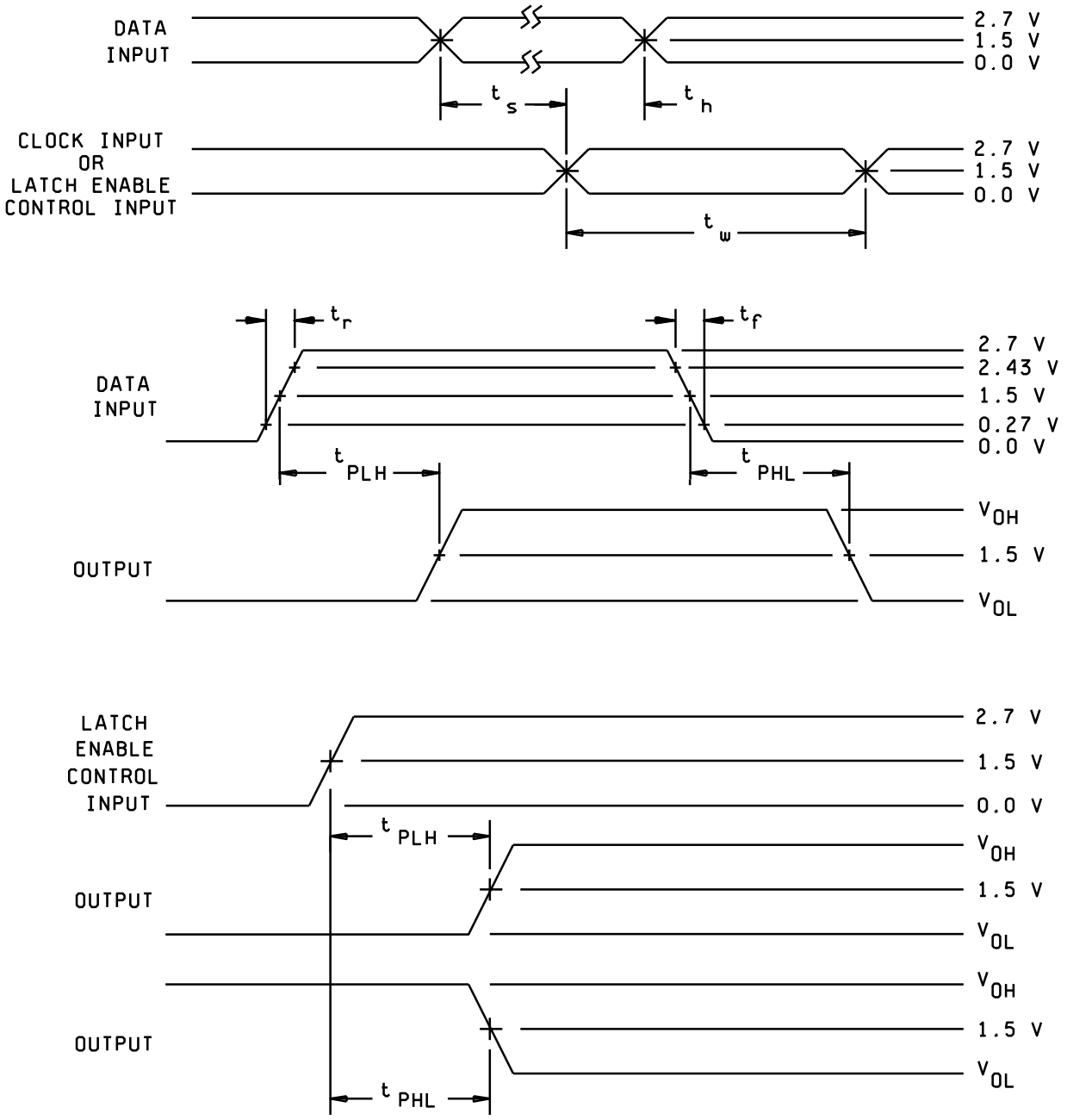


FIGURE 7. Switching waveforms and test circuit.

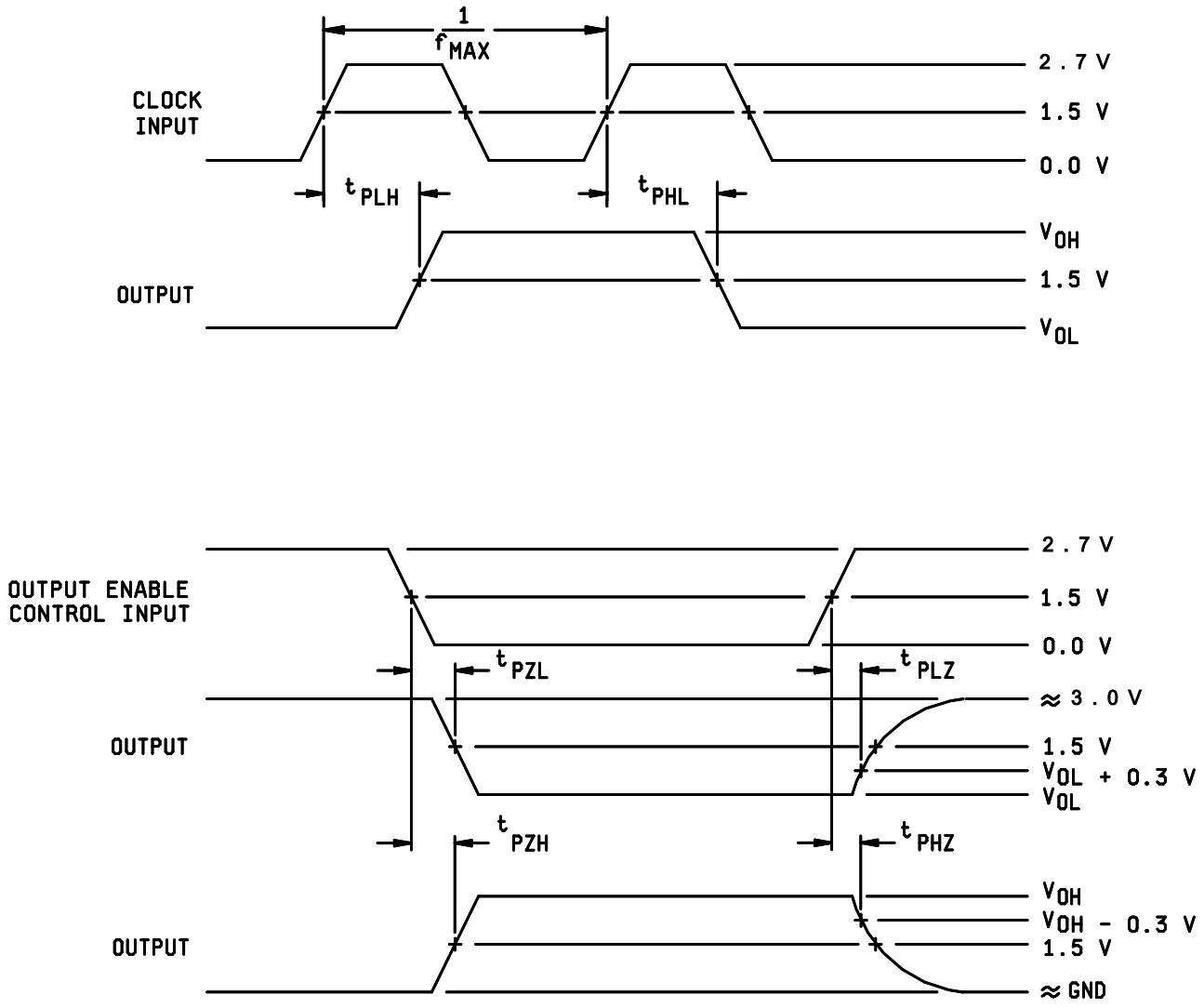


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FIGURE 7. Switching waveforms and test circuit - Continued.

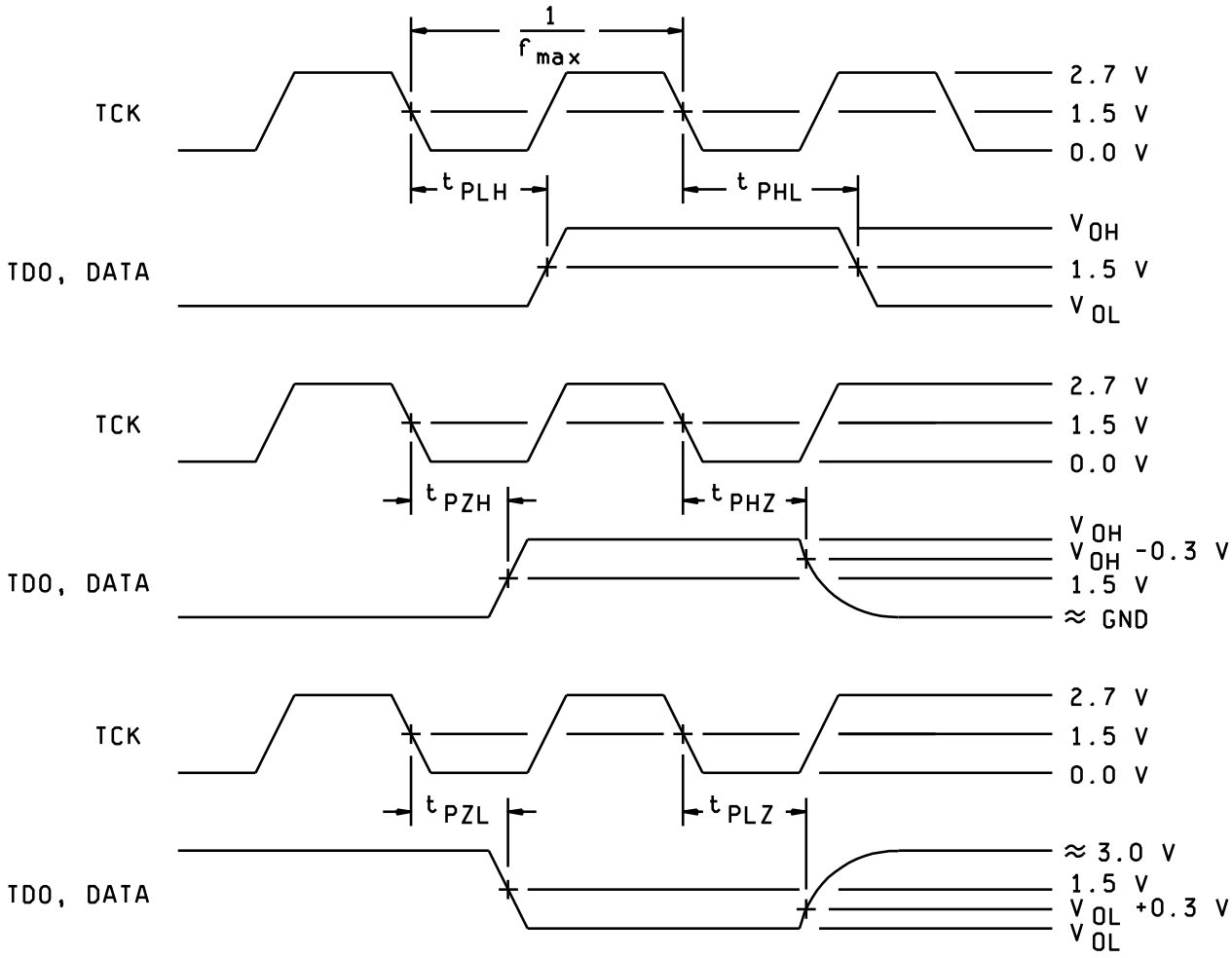
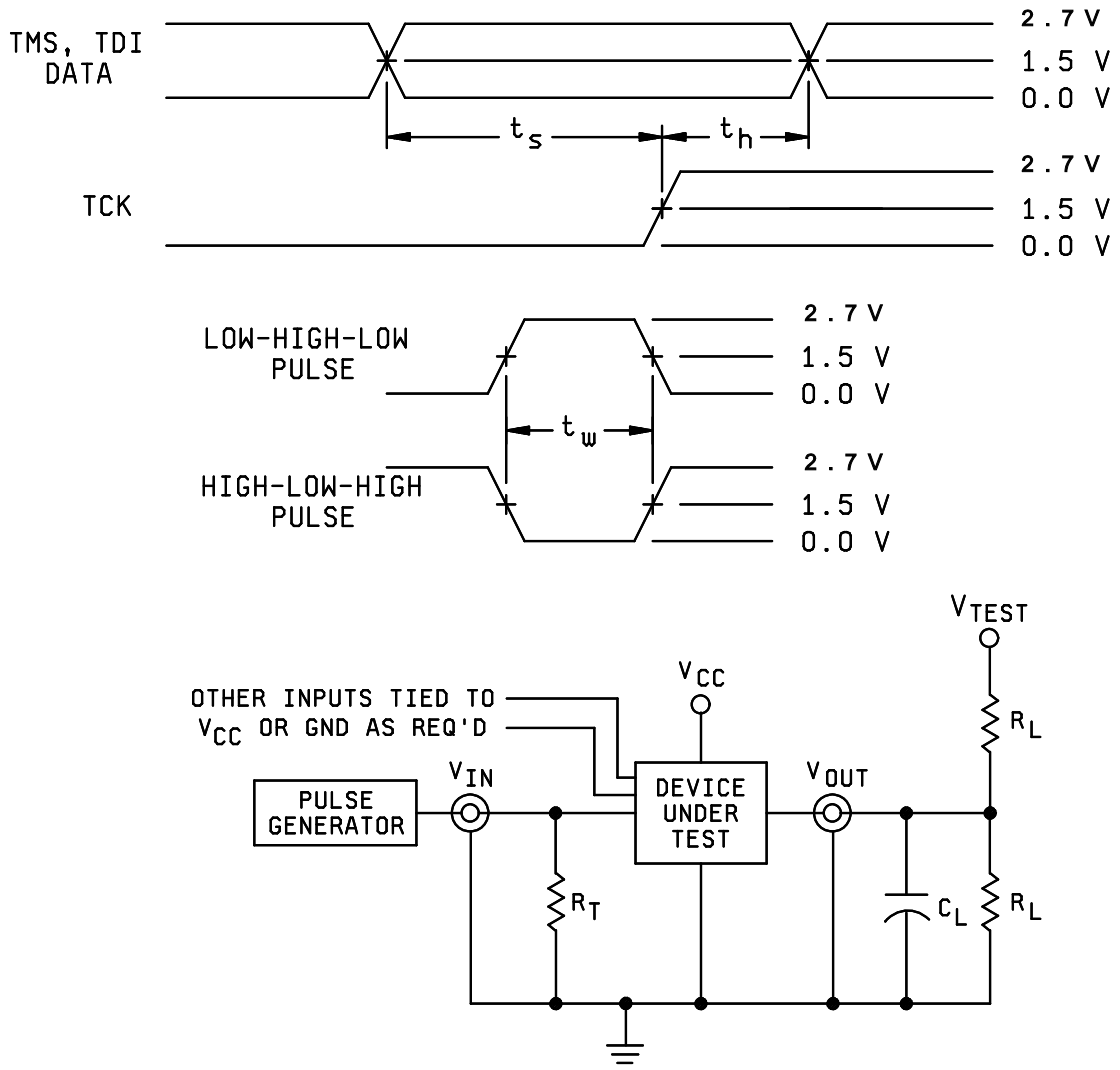


FIGURE 7. Switching waveforms and test circuit - Continued.



NOTES:

1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 6.0 V.
2. When measuring t_{PLH} and t_{PHL}: V_{TEST} = open.
3. When measuring t_{PHZ} and t_{PZH}: V_{TEST} = GND.
4. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
5. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
6. R_L = 500Ω or equivalent.
7. R_T = 50Ω or equivalent.
8. Input signal from pulse generator: V_{IN} = 0.0 V to 2.7 V; PRR ≤ 10 MHz; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns; t_r and t_f shall be measured from 0.27 V to 2.43 V and 2.43 V to 0.27 V, respectively; duty cycle = 50 percent.
9. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
10. The outputs are measured one at a time with one transition per measurement.

FIGURE 7. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN}, $C_{I/O}$, and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN}, $C_{I/O}$, and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN}, $C_{I/O}$, and C_{OUT}, test all applicable pins on five devices with zero failures.

For C_{IN}, $C_{I/O}$, and C_{OUT}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the C_{IN}, $C_{I/O}$, and C_{OUT} tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results for each device tested.

d. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DLA Land and Maritime-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DLA Land and Maritime-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DLA Land and Maritime-VA data from testing on both fixtures, that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For V_{OHP}, V_{OHV}, V_{OLP}, and V_{OLV}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the V_{OHP}, V_{OHV}, V_{OLP}, and V_{OLV} tests. The device manufacturer may then test one device function from a functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-09-23

Approved sources of supply for SMD 5962-96811 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9681101QXA	01295	SNJ54LVTH18502AHV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243