REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE 27014. Add case outline Z. Update boilerplate to MIL-PRF-38535 requirements. – jak	01-08-27	Thomas M. Hess
B	Add vendor CAGE F8859. Add case outline X. Add device type 02. Add table III, delta limits. Editorial changes throughout. – jak	03-04-17	Thomas M. Hess
C	Add section 1.5, radiation features. Update boilerplate to MIL-PRF-38535 requirements and to include radiation hardness assured requirements. Editorial changes throughout. – LTG	05-05-10	Thomas M. Hess
D	Update dimensions of case outline X to figure 1. - LTG	12-08-23	Thomas M. Hess
E	Add case outline Y for device type 02. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	18-10-26	Thomas M. Hess
F	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - TTM	24-05-23	Muhammad A. Akbar

REV																				
SHEET																				
REV																				
SHEET																				
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
96-02-23

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL	SIZE	CAGE CODE	
	F	A	**67268**	**5962-96773**

SHEET 1 OF 18

DSCC FORM 2233
APR 97

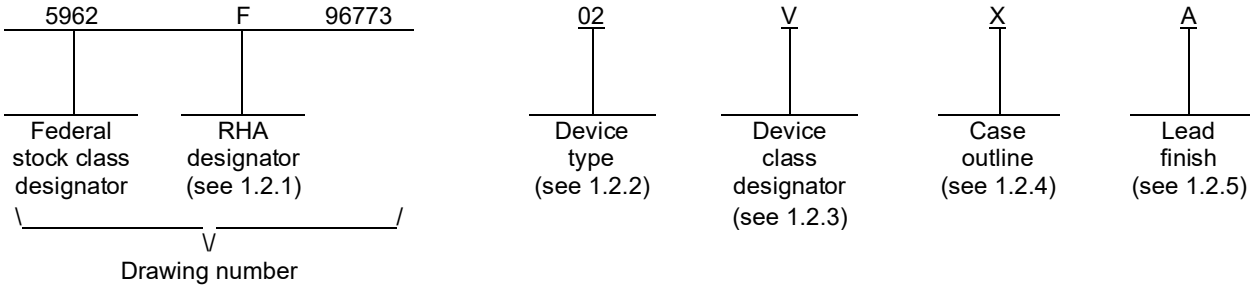
5962-E247-24

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC574	Octal edge-triggered D-type flip-flop with three-state outputs
02	54AC574	Octal edge-triggered D-type flip-flop with three-state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier
Z	GDFP1-G20	20	Flat pack with gullwing
X	See figure 1	20	Flat pack 1/
Y	See figure 1	20	Flat pack 2/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Package case outline X flat pack with isolated lid.
2/ Package case outline Y flat pack with grounded lid.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc 4/
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V or V_{IN} > V_{CC})	±20 mA
DC output clamp current (I_{OK}) (V_{OUT} < 0.0 V or V_{OUT} > V_{CC})	±20 mA
Continuous output current (I_O) (V_{OUT} = 0.0 V to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds):	
Case outline X	+260°C
All other case outlines except case X	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Minimum high level input voltage (V_{IH}):	
V_{CC} = 3.0 V	+2.1 V
V_{CC} = 4.5 V	+3.15 V
V_{CC} = 5.5 V	+3.85 V
Maximum low level input voltage (V_{IL}):	
V_{CC} = 3.0 V	+0.9 V
V_{CC} = 4.5 V	+1.35 V
V_{CC} = 5.5 V	+1.65 V
Maximum high level output current (I_{OH}):	
V_{CC} = 3.0 V	-12 mA
V_{CC} = 4.5 V	-24 mA
V_{CC} = 5.5 V	-24 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 3.0 V	+12 mA
V_{CC} = 4.5 V	+24 mA
V_{CC} = 5.5 V	+24 mA
Input rise or fall time rate ($\Delta t/\Delta V$)	0 to 8 ns/V
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features.

Device type 02:	
Maximum total dose available (dose rate = 50 – 300 rad(Si)/s)	300 kradS(Si)
No Single Event Latchup (SEL) occurs at effective LET (see 4.4.4.2)	≤ 93 MeV-cm^2/mg 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C. Unused inputs must be held high or low.
4/ The input negative voltage rating may be exceeded provided that the input clamp current rating is observed.
5/ Limits obtained during technology characterization/qualification, guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at https://www.jedec.org/.)

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$, $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
							Min	Max	
Positive input clamp voltage 3022	V_{IC+}	For input under test, I_{IN} = 1 mA		All V	GND	1	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, I_{IN} = -1 mA		All V	OPEN	1	-0.4	-1.5	V
High level output voltage 3006	V_{OH1}	For all inputs affecting output under test $V_{IN} = V_{IL}$ or V_{IH} For all other inputs $V_{IN} = V_{CC}$ or GND	I_{OH} = -50 µA	All All	3.0 V	1, 2, 3	2.9		V
					4.5 V		4.4		
					5.5 V		5.4		
	V_{OH2}		I_{OH} = -12 mA		3.0 V	1	2.56		
						2, 3	2.4		
	V_{OH3}		I_{OH} = -24 mA		4.5 V	1	3.94		
						2, 3	3.7		
					5.5 V	1	4.94		
						2, 3	4.7		
	V_{OH4}		I_{OH} = -50 mA	02 All	5.5 V	1, 2, 3	3.85		
Low level output voltage 3007	V_{OL1}	For all inputs affecting output under test $V_{IN} = V_{IL}$ or V_{IH} For all other inputs $V_{IN} = V_{CC}$ or GND	I_{OL} = +50 µA	All All	3.0 V	1, 2, 3		0.1	V
					4.5 V			0.1	
					5.5 V			0.1	
	V_{OL2}		I_{OL} = +12 mA		3.0 V	1		0.36	
						2, 3		0.5	
	V_{OL3}		I_{OL} = +24 mA		4.5 V	1		0.36	
						2, 3		0.5	
					5.5 V	1		0.36	
						2, 3		0.5	
	V_{OL4}		I_{OL} = +50 mA	02 All	5.5 V	1, 2, 3		1.65	
Input current high 3010	I_{IH}	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All All	5.5 V	1		+0.1	µA
						2, 3		+1.0	
Input current low 3009	I_{IL}	For input under test, V_{IN} = GND For all other inputs, $V_{IN} = V_{CC}$ or GND		All All	5.5 V	1		-0.1	µA
						2, 3		-1.0	
Three-state output leakage current, high 3021	I_{OZH}	$\overline{OE} = V_{IH}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All All	5.5 V	1		0.5	µA
						2, 3		5.0	
		$V_{OUT} = V_{CC}$	M, D, P, L, R, F	02 Q, V	5.5 V	1		5.0	
Three-state output leakage current, low 3020	I_{OZL}	$\overline{OE} = V_{IH}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All All	5.5 V	1		-0.5	µA
						2, 3		-5.0	
		V_{OUT} = GND	M, D, P, L, R, F	02 Q, V	5.5 V	1		-5.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$, $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/ Min	Limits 4/ Max	Unit
Quiescent supply current, output high 3005	I_{CCH}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0.0$ A	All	5.5 V	1		4.0	µA
			All		2, 3		80.0	
		M, D, P, L, R, F 5/	02		1		50	
			Q, V					
Quiescent supply current, output low 3005	I_{CCL}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0.0$ A	All	5.5 V	1		4.0	µA
			All		2, 3		80.0	
		M, D, P, L, R, F 5/	02		1		50	
			Q, V					
Quiescent supply current, output three-state 3005	I_{CCZ}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0.0$ A	All	5.5 V	1		4.0	µA
			All		2, 3		80.0	
		M, D, P, L, R, F 5/	02		1		50	
			Q, V					
Power dissipation capacitance	C_{PD} 6/	$T_C = +25°C$, See 4.4.1c	All	5.0 V	4		30	pF
			All					
Input capacitance 3012	C_{IN}	$T_C = +25°C$, $V_{IN} = V_{CC}$ or GND, See 4.4.1c	All	5.0 V	4		9.0	pF
			All					
Functional tests 3014	7/	For all inputs, $V_{IN} = V_{IH}$ or V_{IL}, Verify output V_{OUT}, See 4.4.1b	All	3.0 V	7, 8	L	H	
			All	4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	
Pulse duration, CLK high or low	t_w	$C_L = 50$ pF minimum, $R_L = 500\Omega$, See figure 5	All	3.0 V and 3.6 V	9	6.0		ns
			All		10, 11	4.5		
				4.5 V and 5.5 V	9	4.0		ns
					10, 11	5.0		
Setup time, high or low, data before CLK↑	t_s	$C_L = 50$ pF minimum, $R_L = 500\Omega$, See figure 5	All	3.0 V and 3.6 V	9	2.5		ns
			All		10, 11	6.5		
				4.5 V and 5.5 V	9	1.5		ns
					10, 11	3.5		
Hold time, high or low, data after CLK↑	t_h	$C_L = 50$ pF minimum, $R_L = 500\Omega$, See figure 5	All	3.0 V and 3.6 V	9	1.5		ns
			All		10, 11	2.5		
				4.5 V and 5.5 V	9	1.5		ns
					10, 11	2.5		
Maximum operating frequency	f_{MAX}	$C_L = 50$ pF minimum, $R_L = 500\Omega$, See figure 5	All	3.0 V and 3.6 V	9	75		MHz
			All		10, 11	55		
				4.5 V and 5.5 V	9	95		MHz
					10, 11	85		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$, $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/ Min	Limits 4/ Max	Unit
Propagation delay time, CLK to mQ 3003	t_{PLH} 8/	$R_L = 500\Omega$, $C_L = 50$ pF minimum, See figure 5	All	3.0 V and 3.6 V	9	3.5	13.5	ns
			All		10, 11	1.0	16.5	
			All	4.5 V and 5.5 V	9	2.0	9.5	ns
			All		10, 11	1.5	11.5	
	t_{PHL} 8/	$C_L = 50$ pF minimum, $R_L = 500\Omega$, See figure 5	01	3.0 V and 3.6 V	9	3.5	12.0	ns
			All		10, 11	1.0	15.0	
			02		9	3.5	13.5	ns
			All		10, 11	1.0	16.5	
			01	4.5 V and 5.5 V	9	2.0	8.5	ns
			All		10, 11	1.5	10.5	
			02		9	2.0	9.5	ns
			All		10, 11	1.5	11.5	
Propagation delay time, output enable, $\overline{OE}$ to mQ 3003	t_{PZH} 8/	$C_L = 50$ pF minimum, $R_L = 500\Omega$, See figure 5	All	3.0 V and 3.6 V	9	2.5	11.0	ns
			All		10, 11	1.0	13.0	
			All	4.5 V and 5.5 V	9	2.0	8.5	ns
			All		10, 11	1.5	9.5	
	t_{PZL} 8/		01	3.0 V and 3.6 V	9	3.0	10.5	ns
			All		10, 11	1.0	12.5	
			02		9	3.0	11.0	ns
			All		10, 11	1.0	14.5	
			01	4.5 V and 5.5 V	9	2.0	8.0	ns
			All		10, 11	1.5	9.5	
			02		9	2.0	8.5	ns
			All		10, 11	1.5	9.5	
Propagation delay time, output disable, $\overline{OE}$ to mQ 3003	t_{PHZ} 8/	$C_L = 50$ pF minimum, $R_L = 500\Omega$, See figure 5	All	3.0 V and 3.6 V	9	3.5	12.0	ns
			All		10, 11	1.0	14.0	
			All	4.5 V and 5.5 V	9	2.0	9.5	ns
			All		10, 11	1.5	11.5	
	t_{PLZ} 8/		01	3.0 V and 3.6 V	9	2.0	9.0	ns
			All		10, 11	1.0	10.5	
			02		9	2.0	12.0	ns
			All		10, 11	1.0	14.0	
			01	4.5 V and 5.5 V	9	1.0	7.5	ns
			All		10, 11	1.5	9.0	
			02		9	1.0	9.5	ns
			All		10, 11	1.5	11.5	

See footnotes on next sheet.

1/ For tests not listed in the referenced MIL-STD-883, utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. The values to be used for V_{IH} and V_{IL} shall be the V_{IH} minimum and V_{IL} maximum values listed in section 1.4 herein.

3/ RHA parts for device type 02 have been characterized through all levels M, D, P, L, R, and F of irradiation. However, this device is only tested at the 'F' level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level for any device, T_A = +25°C.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

5/ The maximum limit for this parameter at 100 krads(Si) is 4 μA.

6/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and current consumption (I_S). Where:

$P_D = (C_{PD} + C_L) (V_{CC} \times I_{CC}) f + (I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC} f + I_{CC}$

f is the frequency of the input signal and C_L is the external output load capacitance.

7/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances in accordance with MIL-STD 883 for the input voltage levels may be incorporated. For outputs, $L < 0.3V_{CC}$ and $H \geq 0.7V_{CC}$.

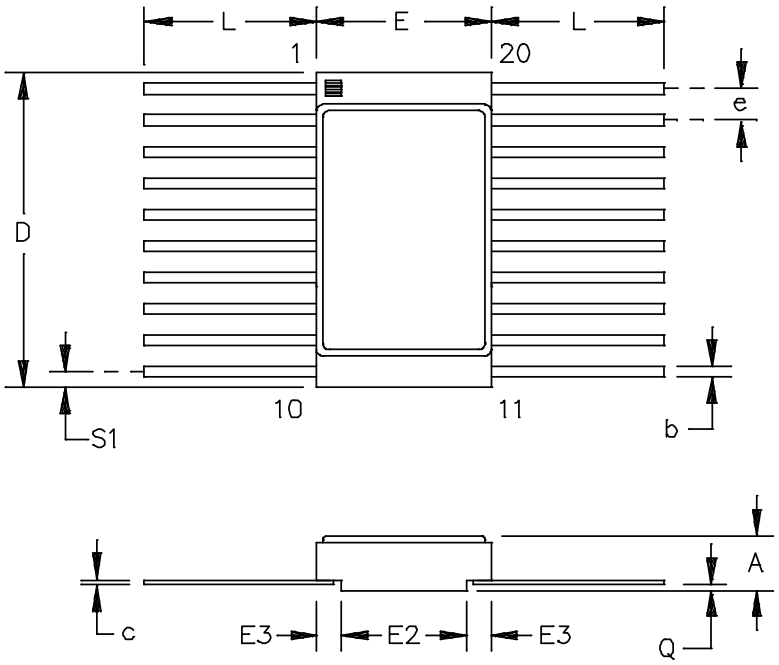
8/ For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	Bias V_{CC} = 5.5 V For latch-up (SEL) test 3/ No SEL occurs at effective LET
02	LET ≤ 93 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested at worst case temperature, T_A = +125°C ± 10°C for latch-up.

Case outlines X and Y



Symbol	Dimensions					
	Inches			Millimeters		
	Typical	Min	Max	Typical	Min	Max
A		0.075	0.087		1.91	2.21
b		0.015	0.019		0.38	0.48
c		0.003	0.006		0.076	0.152
D		0.505	0.515		12.83	13.08
E		0.275	0.285		6.99	7.24
E2		0.199	0.211		5.05	5.36
E3	0.037			0.95		
e		0.045	0.055		1.14	1.40
L		0.250	0.370		6.35	9.39
Q		0.010	---		0.25	---
S1	0.021			0.55		

Note: Deviation from MIL-STD-1835 REF. F-9, CONFIG. B the dimension c is 0.003 inches minimum instead of 0.004 inches minimum and dimension Q is 0.010 inches Minimum instead of 0.026 inches minimum.

FIGURE 1. Case outlines X and Y.

Device types	01, 02
Case outlines	R, S, X, Y, Z, and 2
Terminal number	Terminal symbol
1	$\overline{OE}$
2	1D
3	2D
4	3D
5	4D
6	5D
7	6D
8	7D
9	8D
10	GND
11	CLK
12	8Q
13	7Q
14	6Q
15	5Q
16	4Q
17	3Q
18	2Q
19	1Q
20	V_{CC}

Pin description	
Terminal symbol	Description
mD (m = 1 to 8)	Data inputs
mQ (m = 1 to 8)	Data outputs
$\overline{OE}$	Output enable control input (active low)
CLK	Clock input

FIGURE 2. Terminal connections.

Inputs			Outputs
$\overline{OE}$	CLK	mD	mQ
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance
↑ = Low-to-high clock transition
Q_0 = The level of Q before the indicated steady-state input conditions were established.

FIGURE 3. Truth table.

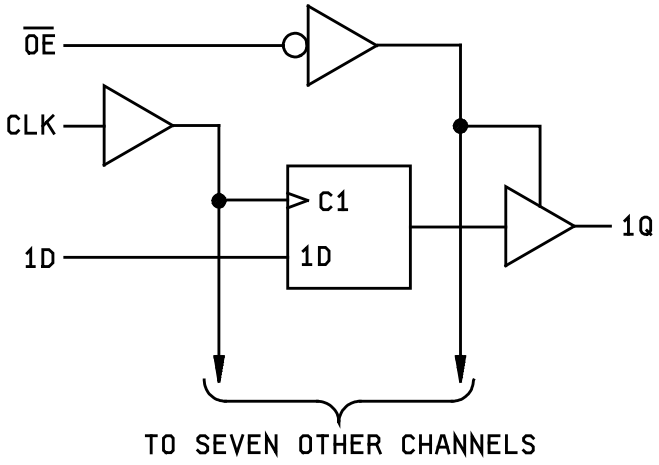


FIGURE 4. Logic diagram.

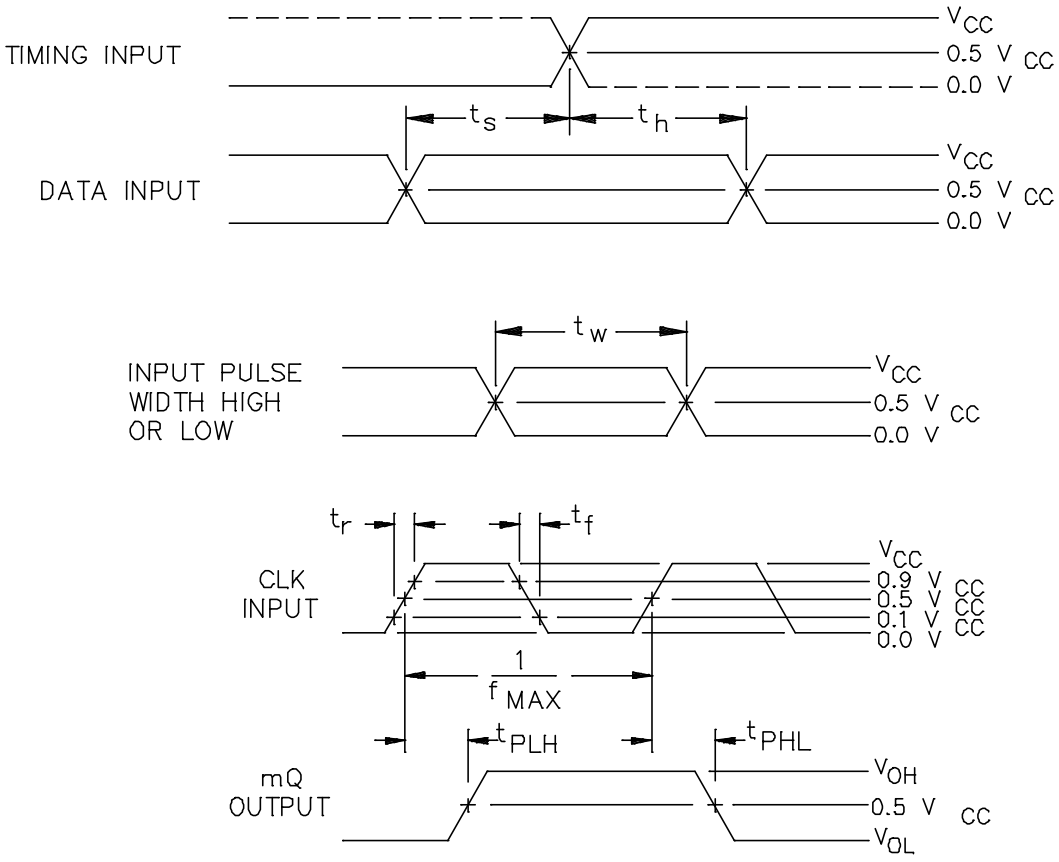
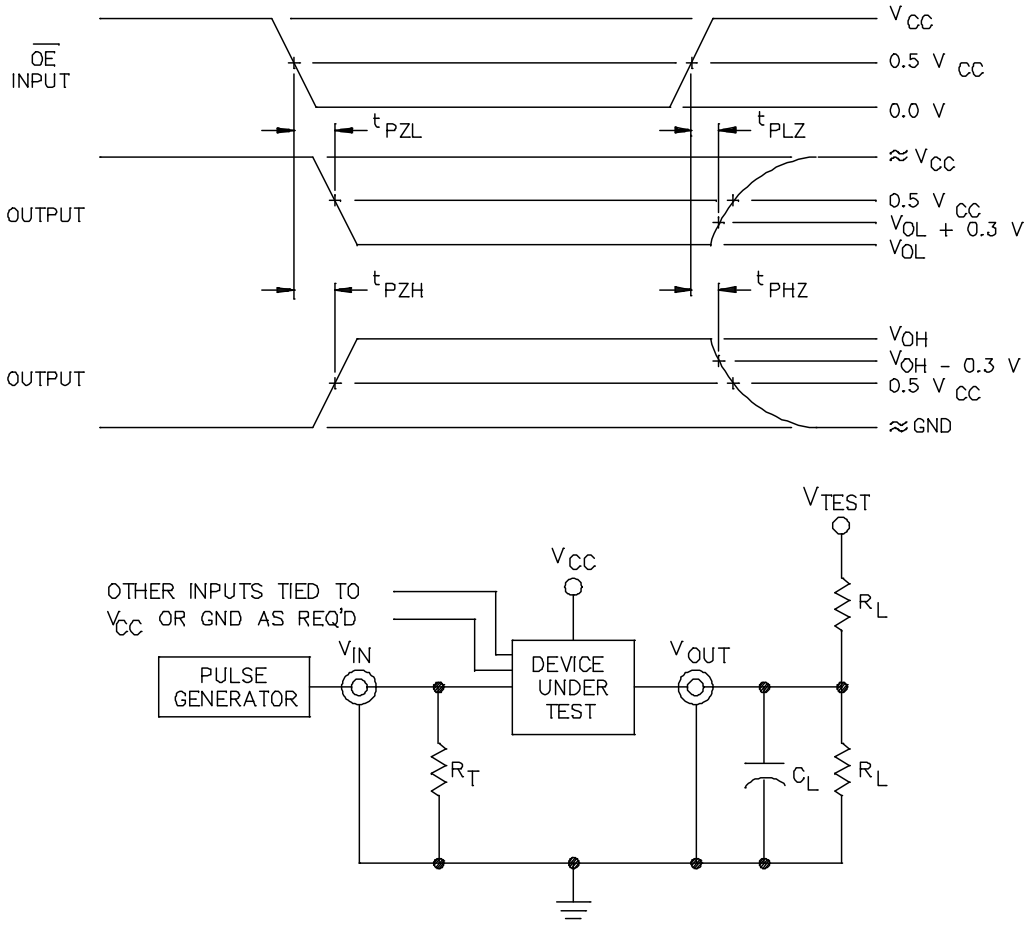


FIGURE 5. Switching waveforms and test circuit.



NOTES:

1. When measuring t_{PLZ} and t_{PZL}: $V_{TEST} = 2 \times V_{CC}$.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. $R_L = 500\Omega$ or equivalent, $R_T = 50\Omega$ or equivalent.
6. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; $t_r \leq 3.0$ ns; $t_f \leq 3.0$ ns; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC}, respectively; duty cycle = 50 percent.
7. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
8. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table IA herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Device type	Delta limits
Supply current	I_{CCH}, I_{CCL}, I_{CCZ}	02	±300 nA
Input current low level	I_{IL}	02	±20 nA
Input current high level	I_{IH}	02	±20 nA
Output voltage low level (V_{CC} = 5.5 V, I_{OL} = +24 mA)	V_{OL}	02	±0.04 V
Output voltage high level (V_{CC} = 5.5 V, I_{OH} = -24 mA)	V_{OH}	02	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta limits.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019 condition A, and as specified herein.

Device type 02:

a. Inputs tested high, V_{CC} = 5.5 V dc ±5%, V_{IN} = 5.0 V dc +10%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

b. Inputs tested low, V_{CC} = 5.5 V dc ±5%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C for the upset measurements and the maximum rated operating temperature ±10°C for the latch-up measurements.

f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions of SEP.

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latch-up (SEL)

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-05-23

Approved sources of supply for SMD 5962-96773 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9677301QRA	01295	SNJ54AC574J
5962-9677301QSA	01295	SNJ54AC574W
5962-9677301QZA	3/	54AC574WG-QML
5962-9677301Q2A	01295	SNJ54AC574FK
5962-9677302QXA	3/	54AC574K02Q
5962-9677302QXC	3/	54AC574K01Q
5962-9677302VXA	3/	54AC574K02V
5962-9677302VXC	3/	54AC574K01V
5962F9677302QRA	F8859	RHFAC574D04Q
5962F9677302QRC	F8859	RHFAC574D03Q
5962F9677302QXA	F8859	RHFAC574K02Q
5962F9677302QXC	F8859	RHFAC574K01Q
5962F9677302VRA	F8859	RHFAC574D04V
5962F9677302VRC	F8859	RHFAC574D03V
5962F9677302VXA	F8859	RHFAC574K02V
5962F9677302VYA	F8859	RHFAC574K04V
5962F9677302VXC	F8859	RHFAC574K01V
5962F9677302VYC	F8859	RHFAC574K03V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243
F8859	STMicroelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE