

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	03-11-13	Raymond Monnin
B	Update drawing to current requirements. Editorial changes throughout. - gap	09-10-02	Charles F. Saffle
C	Update drawing to current MIL-PRF-38535 requirements. Remove class M references. - jt	15-06-17	C. SAFFLE
D	Update drawing to latest MIL-PRF-38535 requirements. - jt	20-04-15	James R. Eschmeyer



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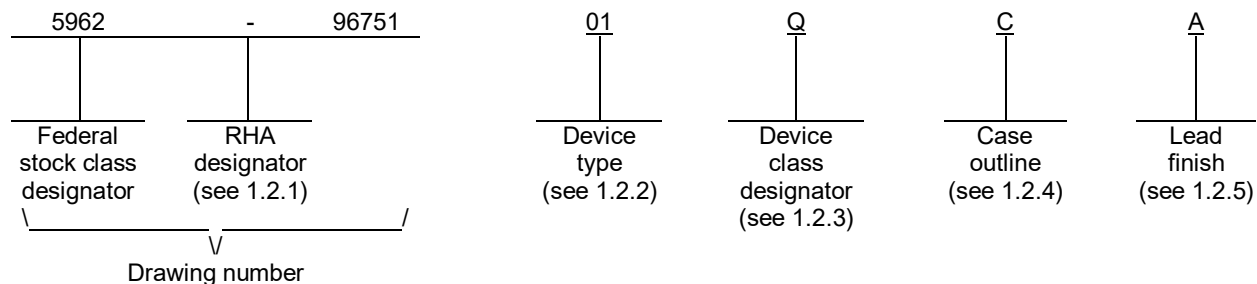
REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D			
	SHEET	1	2	3	4	5	6	7	8	9	10	11				

PMIC N/A	PREPARED BY Larry T. Gauder	<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="https://www.dla.mil/LandandMaritime">https://www.dla.mil/LandandMaritime</a></p>													
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Thomas M. Hess														
	APPROVED BY Monica L. Poelking	<p align="center">MICROCIRCUIT, DIGITAL, BIPOLAR, LOW-POWER SCHOTTKY TTL, DUAL J-K FLIP-FLOPS WITH CLEAR, MONOLITHIC SILICON</p>													
	DRAWING APPROVAL DATE 96-02-09														
	REVISION LEVEL D	<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE <b>67268</b></td> <td><b>5962-96751</b></td> </tr> </table>	SIZE A	CAGE CODE <b>67268</b>	<b>5962-96751</b>										
SIZE A	CAGE CODE <b>67268</b>	<b>5962-96751</b>													
		SHEET 1 OF 11													

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54LS73A	Dual J-K flip-flops with clear

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line package
D	GDFP1-F14 or CDFP2-F14	14	Flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range .....	-1.5 V dc at -18 mA to +7.0 V dc
Storage temperature range .....	-65°C to +150°C
Maximum power dissipation ( $P_D$ ) 2/ .....	110 mW
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	See MIL-STD-1835
Junction temperature ( $T_J$ ) .....	+175°C

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ) .....	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level output current ( $I_{OH}$ ) .....	-0.4 mA
Maximum low level output current ( $I_{OL}$ ) .....	4 mA
Maximum input clamp voltage ( $V_{IK}$ ) .....	-1.5 V
Pulse width ( $t_W$ ) :	
Clock high .....	20 ns
Clear low .....	25 ns
Setup time ( $t_{SU}$ ) 3/ .....	20 ns ↓
Hold time ( $t_H$ ) 3/ .....	0 ns ↓
Case operating temperature range ( $T_C$ ) .....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.  
2/ Maximum power dissipation is defined as  $V_{CC} \times I_{CC}$ , and must withstand the added  $P_D$  due to short circuit test e.g.,  $I_{OS}$ .  
3/ The symbol ↓ indicates the falling edge of the clock pulse is used for reference.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IL</sub> = 0.7 V, V <sub>IH</sub> = 2.0 V, I <sub>OH</sub> = -0.4 mA		1, 2, 3	2.5		V
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IL</sub> = 0.7 V, V <sub>IH</sub> = 2.0 V, I <sub>OL</sub> = 4.0 mA		1, 2, 3		0.4	V
Input clamp voltage	V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		1		-1.5	V
Input current @ max input voltage	I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 7.0 V	J or K	1, 2, 3		0.1	mA
			Clear			0.3	
			Clock			0.4	
High level input current	I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V	J or K	1, 2, 3		20	μA
			Clear			60	
			Clock			80	
Low level input current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V	J or K	1, 2, 3		-0.4	mA
			Clear			-0.8	
			Clock			-0.8	
Supply current <u>1/</u>	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V		1, 2, 3		65	mA
Short circuit output current <u>2/</u>	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V		1, 2, 3	-20	-100	mA
Functional tests		See 4.4.1b, V <sub>CC</sub> = 4.5 V, 5.5 V		7, 8			
Maximum clock frequency <u>3/</u>	f <sub>MAX</sub>	V <sub>CC</sub> = 5.0 V, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF		9, 10, 11	30		MHz
Propagation delay time clear to Q, clear to $\bar{Q}$ <u>3/</u>	t <sub>PHL1</sub> , t <sub>PLH1</sub>			9		20	ns
				10, 11		28	
Propagation delay time clock to Q or $\bar{Q}$ <u>3/</u>	t <sub>PHL2</sub> , t <sub>PLH2</sub>			9		20	ns
				10, 11		28	

- 1/ With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock is grounded.
- 2/ Not more than one output should be shorted at a time, and the duration of the short-circuit conditions should not exceed one second.
- 3/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

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Device type 01	
Case outlines	C and D
Terminal number	Terminal symbol
1	CLK1
2	CLR1
3	K1
4	V <sub>CC</sub>
5	CLK2
6	CLR2
7	J2
8	Q2
9	Q2
10	K2
11	GND
12	Q1
13	$\bar{Q}1$
14	J1

FIGURE 1. Terminal connections.

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

H = High logic level.

L = Low logic level.

X = Either low or high logic level

↓ = Negative going edge of pulse

Q<sub>0</sub> = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

FIGURE 2. Truth table.

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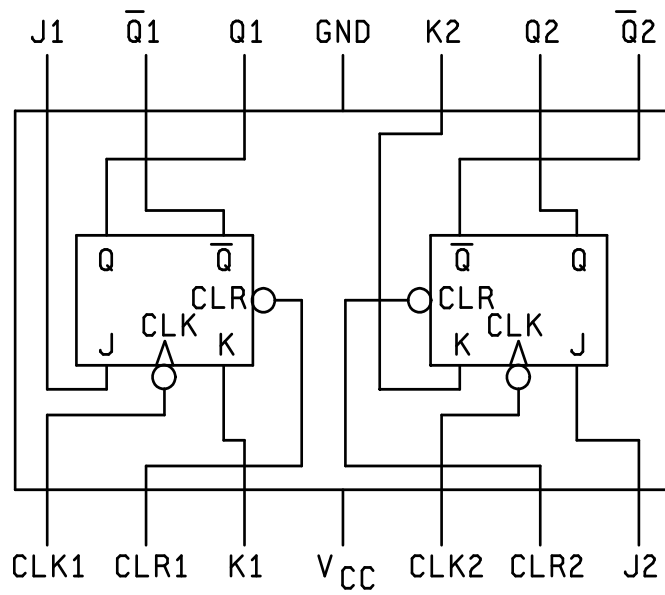


FIGURE 3. Logic diagram.

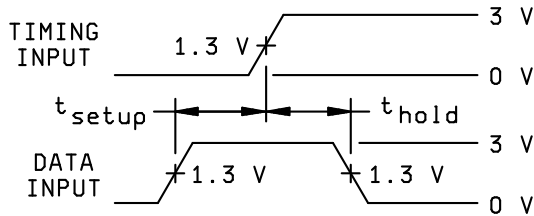
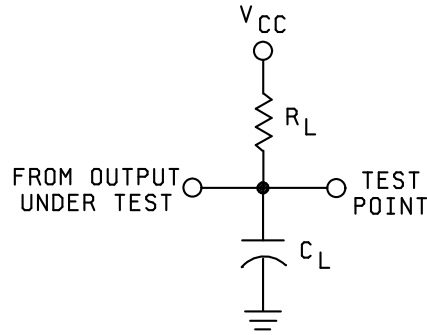
**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

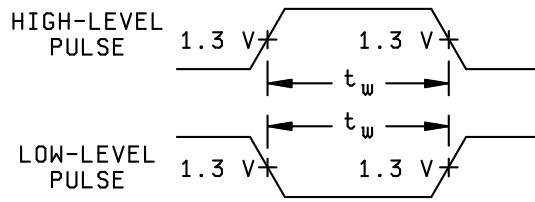
**5962-96751**

REVISION LEVEL  
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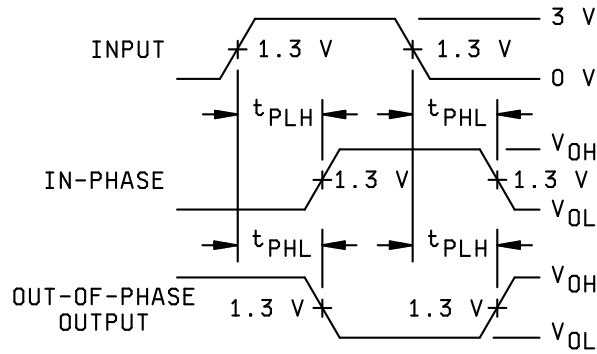
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VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE WIDTHS



NOTES:

1.  $R_L = 2 \text{ k}\Omega$
2.  $C_L$  = Load capacitance includes jig and probe capacitance.
3. All input pulses have the following characteristics:  $\text{PRR} \leq 1 \text{ MHz}$ ,  $Z_{\text{OUT}} = 50 \Omega$ ,  $t_r \leq 2.0 \text{ ns}$ ,  $t_f \leq 2.0 \text{ ns}$ .
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Timing waveforms.

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COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**D**

**5962-96751**

SHEET  
**8**



4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---
Final electrical parameters (see 4.2)	<u>1/ 3/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/ 3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	<u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 8,
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 8

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

3/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ , after exposure, to the subgroups specified in table II herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-04-15

Approved sources of supply for SMD 5962-96751 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9675101QCA	01295	SNJ54LS73AJ
5962-9675101VCA	<u>3/</u>	SNV54LS73AJ
5962-9675101QDA	01295	SNJ54LS73AW
5962-9675101VDA	<u>3/</u>	SNV54LS73AW

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE  
number

Vendor name  
and address

01295

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
PO Box 660199  
Dallas, TX 75243

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