REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add paragraph 3.1.1 and die appendix A. Changes in accordance with NOR 5962-R104-98. - rrp	98-05-11	R. Monnin
B	Add class T requirements. Update boilerplate. Redrawn. - rrp	98-12-09	R. Monnin
C	Made changes to 1.5 and added new RHA designator P in table I. - rrp	99-04-19	R. Monnin
D	Add device type 02. Make changes to 1.2.2, 1.5, table I, figure 1, and appendix A. - ro	99-11-24	R. Monnin
E	Made changes to figure 3. - rrp	00-01-03	R. Monnin
F	Redraw. Update drawing to current requirements. - drw	11-01-05	Charles F. Saffle
G	Add device type 03. Add new footnote to paragraph 1.2.2. Delete dose rate burnout paragraphs and Table III. Add paragraph 2.2 and SEP Table IB. Make changes to paragraphs 3.2.5, 3.10 and 4.4.4.4. - ro	12-05-10	Charles F. Saffle
H	Delete the word “CMOS” from the description block on sheet 1. Delete references to device class M requirements. Update document paragraphs to current requirements. - ro	17-06-02	Charles F. Saffle

REV																				
SHEET																				
REV	H	H	H	H	H	H	H	H	H	H										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS	REV	H	H	H	H	H	H	H	H	H	H	H	H	H
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Sandra Rooney

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Sandra Rooney

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
96-01-10

REVISION LEVEL
H

MICROCIRCUIT, LINEAR, RADIATION HARDENED, MULTIPLEXER WITH OVERVOLTAGE PROTECTION, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96742**

SHEET 1 OF 24

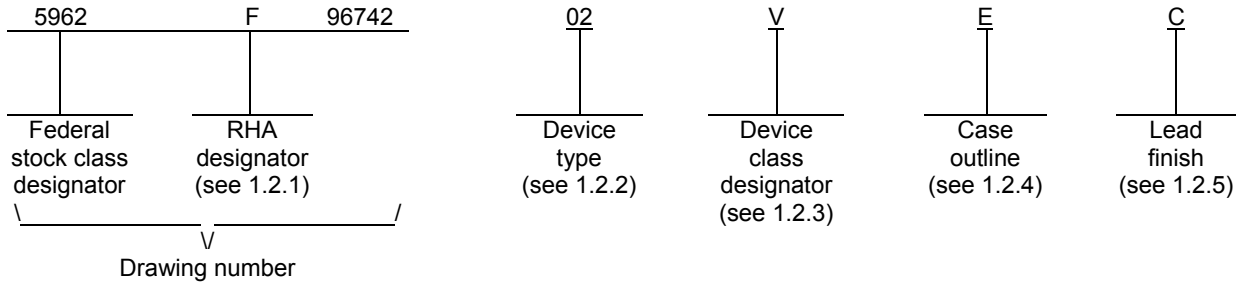
DSCC FORM 2233
APR 97

5962-E331-17

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-508ARH	Radiation hardened DI CMOS single 8-channel MUX with overvoltage protection
02 1/	HS-508BRH	Radiation hardened dielectrically isolated (DI) BiCMOS single 8-channel MUX with overvoltage protection
03 1/	HS-508BEH	Radiation hardened dielectrically isolated (DI) BiCMOS single 8-channel MUX with overvoltage protection

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1/ This device is BiCMOS as it utilizes both bipolar and CMOS technologies in the design and manufacturing processes.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	CDIP2-T16	16	Dual-in-line
X	CDFP4-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 2/

Supply voltage between +V and –V ..... 40 V
Supply voltage between +V and ground ..... +20 V
Supply voltage between -V and ground ..... -20 V
Digital input overvoltage:
  $+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ + 4 V
  $-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ - 4 V
Analog input overvoltage:
  $+V_S$ ..... $+V_{SUPPLY}$ +20 V
  $-V_S$ ..... $-V_{SUPPLY}$ -20 V
Peak current, S or D (pulsed at 1 ms, 10 percent duty cycle max) ..... 40 mA
Storage temperature range ..... -65°C to +150°C
Maximum package power dissipation at T_A = +125°C (P_D): 3/
  Case outline E ..... 0.67 W
  Case outline X ..... 0.59 W
Thermal resistance, junction-to-case (θ_{JC}):
  Case outline E ..... 12°C/W
  Case outline X ..... 25°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):
  Case outline E ..... 75°C/W
  Case outline X ..... 85°C/W
Lead temperature (soldering, 10 seconds) ..... +275°C
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Operating supply voltage ($\pm V_{SUPPLY}$) ..... ±15 V
Logic low level (V_{AL}) ..... +0.8 V
Logic high level (V_{AH}) ..... +4.0 V
Ambient operating temperature range (T_A) ..... -55°C to +125°C

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the following rates:
  Case outline E ..... 13.3 mW/°C
  Case outline X ..... 11.76 mW/°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):
Device classes Q and V:
Device type 01 ..... 100 krads(Si)
Device type 02 ..... 300 krads(Si) 4/
Device type 03 ..... 300 krads(Si) 5/
Device class T:
Device type 01 ..... 100 krads(Si)
Device type 02 ..... 100 krads(Si) 4/

Maximum total dose available (dose rate ≤ 0.01 rad(Si)/s):
Device type 03 ..... 50 krads(Si) 5/

Single event phenomena (SEP):
Device type 01:
No single event upset (SEU) occurs at an effective linear energy
transfer (LET) (see 4.4.4.4) ..... ≤ 110 (MeV/mg/cm^2) 6/
Device types 02 and 03 ..... Not tested
Single event latch up (SEL) ..... No latch up 7/

Dose rate upset (20 ns pulse):
Device type 01 ..... = 1 x 10^8 rads(Si)/s
Device types 02 and 03 ..... Not tested

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

4/ Device type 02 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si) .
5/ Device type 03 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si), and condition D to a maximum total dose of 50 krads(Si).
6/ Guaranteed by process design, but not tested.
7/ Device types 01, 02, and 03 use dielectrically isolated (DI) technology and latch-up is physically not possible.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Timing diagrams. The timing diagrams shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{AH} = +4 V, V_{AL} = 0.8 V, -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current address, or enable pins	I_{AH}, I_{AL}	Measure inputs sequentially, ground all unused pins	1, 2, 3	All	-1000	+1000	nA
		M, D, P, L, R, F	1		-1000	+1000	
Leakage current into the source terminal of an “OFF” switch	$+I_{S(OFF)}$	V_S = +10 V, all unused inputs and outputs = -10 V, V_{EN} = 0.8 V	1	All	-10	+10	nA
			2, 3		-50	+50	
		M, D, P, L, R, F	1		-50	+50	
	$-I_{S(OFF)}$	V_S = -10 V, all unused inputs and outputs = +10 V, V_{EN} = 0.8 V	1	All	-10	+10	nA
			2, 3		-50	+50	
		M, D, P, L, R, F	1		-50	+50	
Leakage current into the drain terminal of an “OFF” switch	$+I_{D(OFF)}$	V_D = +10 V, all unused inputs and outputs = -10 V, V_{EN} = 0.8 V	1	All	-10	+10	nA
			2, 3		-250	+250	
		M, D, P, L, R, F	1		-250	+250	
	$-I_{D(OFF)}$	V_D = -10 V, all unused inputs and outputs = +10 V, V_{EN} = 0.8 V	1	All	-10	+10	nA
			2, 3		-250	+250	
		M, D, P, L, R, F	1		-250	+250	
Leakage current into the drain terminal of an “OFF” switch with overvoltage applied	$+I_{D(OFF)}$ overvoltage	V_S = +25 V, measure V_D, V_{EN} = 0.8 V, all unused inputs to GND	1, 2, 3	All	-2000	+2000	nA
		M, D, P, L, R, F	1		-2000	+2000	
	$-I_{D(OFF)}$ overvoltage	V_S = -25 V, measure V_D, V_{EN} = 0.8 V, all unused inputs to GND	1, 2, 3	All	-2000	+2000	nA
		M, D, P, L, R, F	1		-2000	+2000	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{AH} = +4 V, V_{AL} = 0.8 V, -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Leakage current from an "ON" driver into the switch (drain and source)	$+I_{D(ON)}$	$V_S = V_D$ = +10 V, V_{EN} = 4.0 V, all unused inputs = -10 V	1	All	-10	+10	nA
			2, 3		-250	+250	
		M, D, P, L, R, F	1		-250	+250	
	$-I_{D(ON)}$	$V_S = V_D$ = -10 V, V_{EN} = 4.0 V, all unused inputs = +10 V	1	All	-10	+10	nA
			2, 3		-250	+250	
		M, D, P, L, R, F	1		-250	+250	
Switch on resistance	$+R_{(ON)}$	V_S = +10 V, V_{EN} = 4.0 V, I_{OUT} = -100 μA	1	All		1500	Ω
			2, 3			1800	
		M, D, P, L, R, F	1			1800	
	$-R_{(ON)}$	V_S = -10 V, V_{EN} = 4.0 V, I_{OUT} = +100 μA	1	All		1500	Ω
			2, 3			1800	
		M, D, P, L, R, F	1			1800	
Positive supply current	I(+)	V_{EN} = 4.0 V	1, 2, 3	All		2	mA
		M, D, P, L, R, F	1			2	
Negative supply current	I(-)	V_{EN} = 4.0 V	1, 2, 3	All	-1		mA
		M, D, P, L, R, F	1		-1		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{AH} = +4 V, V_{AL} = 0.8 V, -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Positive standby supply current	$+I_{(SBY)}$	V_{EN} = 0.8 V	1, 2, 3	All		2	mA
		M, D, P, L, R, F	1			2	
Negative standby supply current	$-I_{(SBY)}$	V_{EN} = 0.8 V	1, 2, 3	All	-1		mA
		M, D, P, L, R, F	1		-1		
Capacitance address input	C_A 2/	$+V_S = -V_S$ = 0 V, f = 1 MHz	4	All		7	pF
Capacitance channel input	$C_{S(OFF)}$ 2/	$+V_S = -V_S$ = 0 V, f = 1 MHz	4	All		7	pF
Capacitance channel output	$C_{D(OFF)}$ 2/	$+V_S = -V_S$ = 0 V, f = 1 MHz	4	All		25	pF
Off isolation	V_{ISO} 2/ 3/	V_{EN} = 0.8 V, f = 200 kHz, C_L = 7 pF, R_L = 1 kΩ, V_S = 3.0 V RMS	4	All	45		dB
Analog signal range	V_S	See 4.4.1b	7, 8	All	-15	+15	V
Break-before-make time delay	T_D	R_L = 1000 Ω, C_L = 50 pF, see figure 3	9	All	25		ns
			10, 11		5		
		M, D, P, L, R, F	9		5		
Access time: Address inputs to I/O channels	$T_{ON(A)}$, $T_{OFF(A)}$	R_L = 10 kΩ, C_L = 50 pF, see figure 3	9	All		600	ns
			10, 11			1000	
		M, D, P, L, R, F	9			3000	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{AH} = +4 V, V_{AL} = 0.8 V, -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Access time: Enable to I/O	$T_{ON(EN)}$,	R_L = 1000 Ω, C_L = 50 pF,	9	All		600	ns
	$T_{OFF(EN)}$	see figure 3	10, 11			1000	
		M, D, P, L, R, F	9			3000	

1/ Devices supplied to this drawing will meet all levels M, D, P, L, and R, for device type 01 (device classes Q and V), and levels M, D, P, L, R and F, for device types 02 and 03 (devices classes Q or V), and levels M, D, P, L and R, for device types 01 and 02 (device class T). However, device type 01 (device classes Q and V) are only tested at the "R" level and device types 02 and 03 (device classes Q and V) are only tested at the "F" level, and device types 01 and 02 (class T) are only tested at the "R" level in accordance with MIL-STDF-883 method 1019 condition A (see paragraph 1.5 herein). Device type 02 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

In addition, device 03 is production lot acceptance tested on a wafer by wafer basis to 300 krads(Si) in accordance with MIL-STD-883 method 1019 condition A, and 50 krads(Si) in accordance with MIL-STD-883 method 1019 condition D.

2/ These parameters are controlled via design or process parameters and not directly tested. These parameters are characterized upon initial qualification and after any process or design changes which would affect these characteristics. See 4.4.1d.

3/ Worst case isolation occurs on channel 4 due to proximity of the output pins.

TABLE IB. SEP test limits. 1/ 2/

Device type	Bias for Single event upset (SEU) test; maximum operating voltage +V = +15 V No SEU at effective LET = [MeV/mg/cm^2] 3/ 4/ 5/
01	LET ≤ 110

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for upset at worst case operating temperature, T_A = +25°C ± 10°C
4/ Tested to LET ≤ 110 MeV/mg/cm^2 and no upset occurs.
5/ Guaranteed by process or design, not tested.

Device types	01, 02, and 03
Case outlines	E and X
Terminal number	Terminal symbol
1	A0
2	EN
3	-V
4	IN 1
5	IN 2
6	IN 3
7	IN 4
8	OUT
9	IN 8
10	IN 7
11	IN 6
12	IN 5
13	+V
14	GND
15	A2
16	A1

FIGURE 1. Terminal connections.

A2	A1	A0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

FIGURE 2. Truth table.

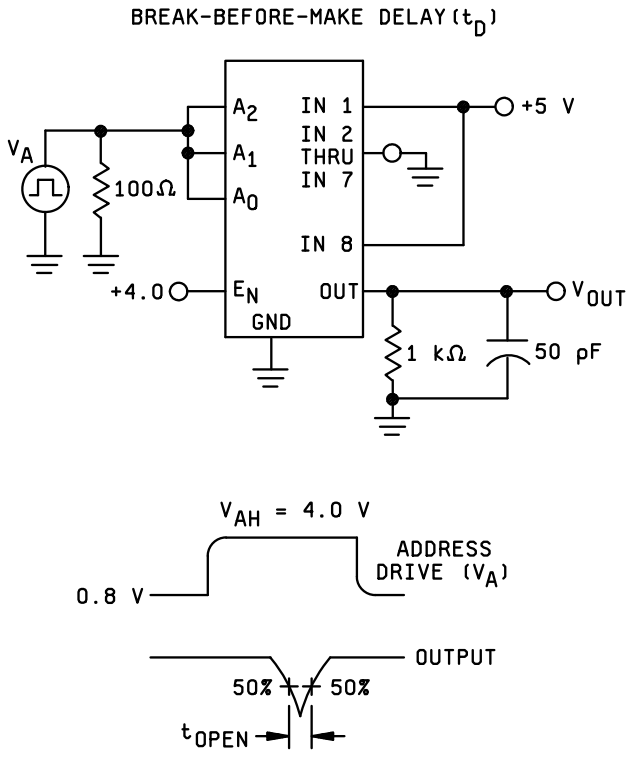


FIGURE 3. Timing diagrams.

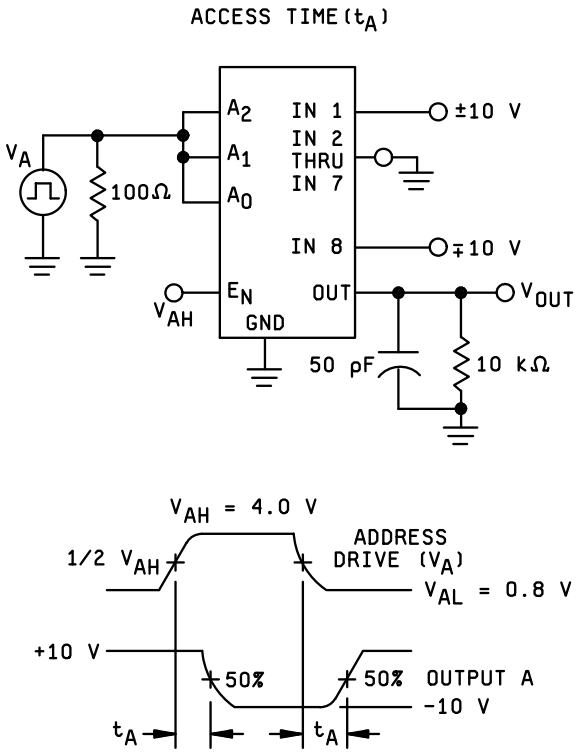


FIGURE 3. Timing diagrams - continued.

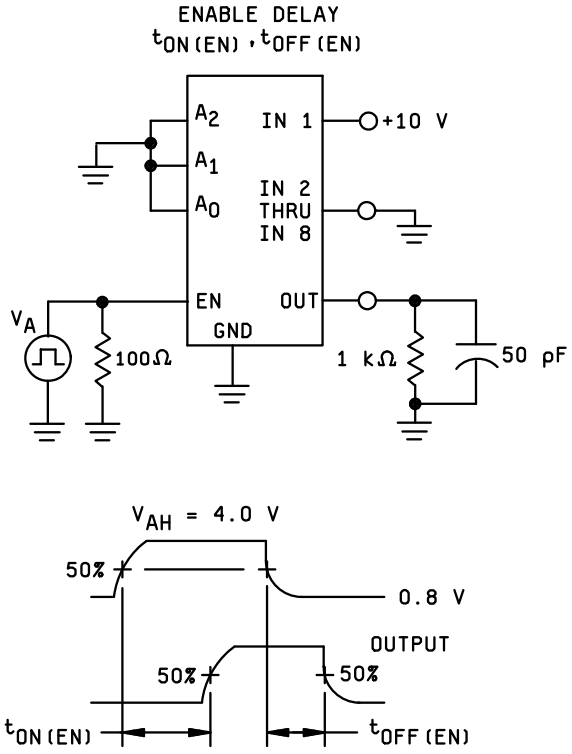


FIGURE 3. Timing diagrams - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

d. Subgroup 4 (C_A, $C_{S(OFF)}$, $C_{D(OFF)}$, and V_{ISO} measurements) should be measured only for initial qualification and after any process or design changes which may affect input, output capacitance or isolation voltage.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	As specified in QM plan
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 1/ 9, 10, 11	1, 2, 3, 1/ 2/ 7, 8, 9, 10, 11	As specified in QM plan
Group A test requirements (see 4.4)	1, 2, 3, 4, 3/ 7, 8, 9, 10, 11	1, 2, 3, 4, 3/ 7, 8, 9, 10, 11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 2/ 8, 9, 10, 11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	As specified in QM plan

1/ PDA applies to subgroup 1 and 7. For class V to subgroups 1, 7 and Δ.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).
3/ Subgroup 4, if not tested, shall be guaranteed to the limits specified in table IA.

4.4.2.2 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01, 02, and 03. In addition, for device type 03 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Delta limits
Input leakage current, Address or Enable pins	I_{AH}	Measure inputs sequentially, ground all unused pins	±100 nA
	I_{AL}		
Leakage current into the source terminal of an "OFF" switch	$+I_{S(OFF)}$	V_S = +10 V, all unused inputs and outputs = -10 V, V_{EN} = 0.8 V	±20 nA
	$-I_{S(OFF)}$	V_S = -10 V, all unused inputs and outputs = +10 V, V_{EN} = 0.8 V	±20 nA
Leakage current into the drain terminal of an "OFF" switch	$+I_{D(OFF)}$	V_D = +10 V, V_{EN} = 0.8 V, all unused inputs = -10 V	±20 nA
	$-I_{D(OFF)}$	V_D = -10 V, V_{EN} = 0.8 V, all unused inputs = +10 V	±20 nA
Leakage current from an "ON" driver into the switch (drain & source)	$+I_{D(ON)}$	$V_S = V_D$ = +10 V, V_{EN} = 4.0 V, all unused inputs = -10 V	±20 nA
	$-I_{D(ON)}$	$V_S = V_D$ = -10 V, V_{EN} = 4.0 V, all unused inputs = +10 V	±20 nA
Switch ON resistance	$+R_{(ON)}$	V_S = +10 V, V_{EN} = 4.0 V, I_{OUT} = -100 μA	±150 Ω
	$-R_{(ON)}$	V_S = -10 V, V_{EN} = 4.0 V, I_{OUT} = +100 μA	±150 Ω
Positive supply current	$I_{(+)}$	V_{EN} = 4.0 V	±200 μA
Negative supply current	$I_{(-)}$	V_{EN} = 4.0 V	±100 μA
Positive standby supply current	$+I_{(SBY)}$	V_{EN} = 0.8 V	±200 μA
Negative standby supply current	$-I_{(SBY)}$	V_{EN} = 0.8 V	±100 μA

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed on a technology process, in accordance with test method 1023 of MIL-STD-883 and herein (see 1.5 herein).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the device. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q, T, and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C for upset and the maximum rated operating temperature $\pm$10°C for latchup.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

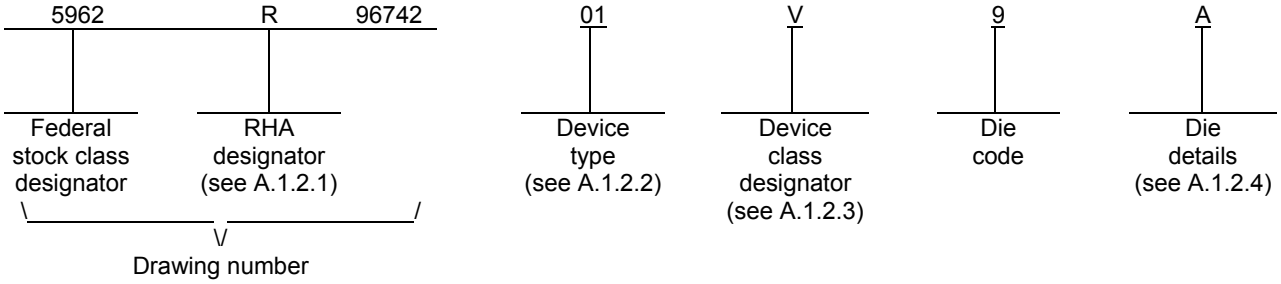
a. RHA upset levels.
b. Test conditions (SEP).
c. Number of upsets (SEU).
d. Occurrence of latchup (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96742

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-508ARH	Radiation hardened, DI, CMOS single 8-channel MUX with overvoltage protection.
02 1/	HS-508BRH	Radiation hardened dielectrically isolated (DI) BiCMOS single 8-channel MUX with overvoltage protection
03 1/	HS-508BEH	Radiation hardened dielectrically isolated (DI) BiCMOS single 8-channel MUX with overvoltage protection

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

1/ This device is BiCMOS as it utilizes both bipolar and CMOS technologies in the design and manufacturing processes.

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02, 03	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02, 03	A-2

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1
02, 03	A-2

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1
02, 03	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1 (device type 01) or figure A-2 (device type 02).

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1 (device type 01) or figure A-2 (device type 02).

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1 (device type 01) or figure A-2 (device type 02).

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1 (device type 01) or figure A-2 (device type 02).

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.2.1, 4.4.4.3, and 4.4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

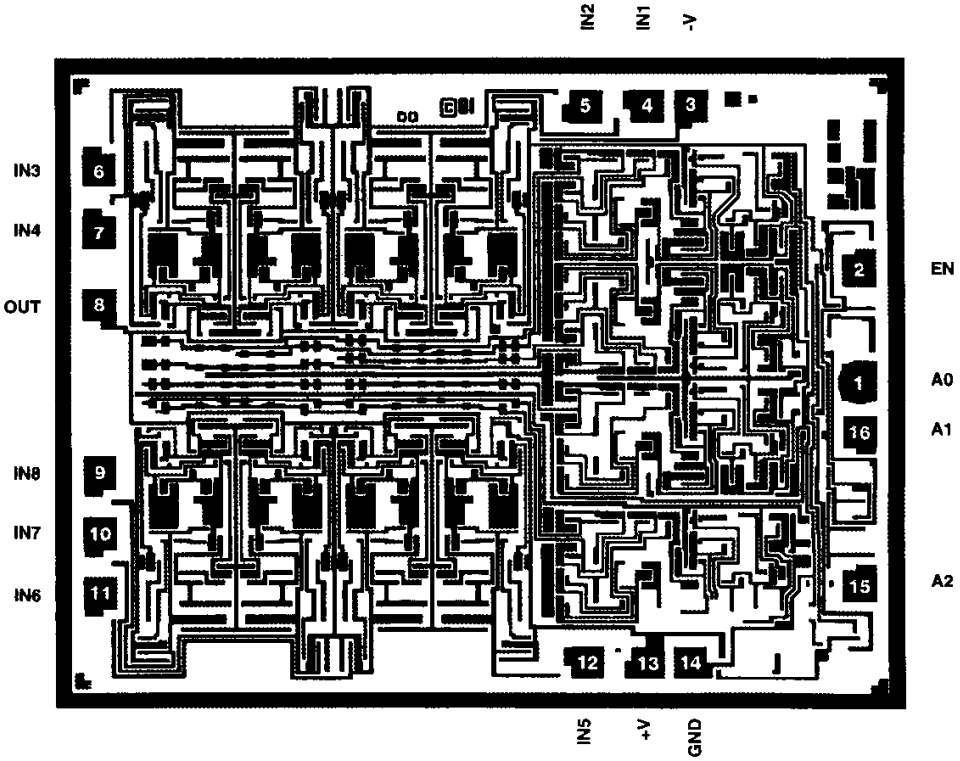
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



Device type 01.

Die physical dimensions.
Die size: 2120 x 2750 microns
Die thickness: 19 ± 1 mils

Interface materials.
Top metallization: Al/Cu 12.5 kÅ ± 2 kÅ
Backside metallization: None.

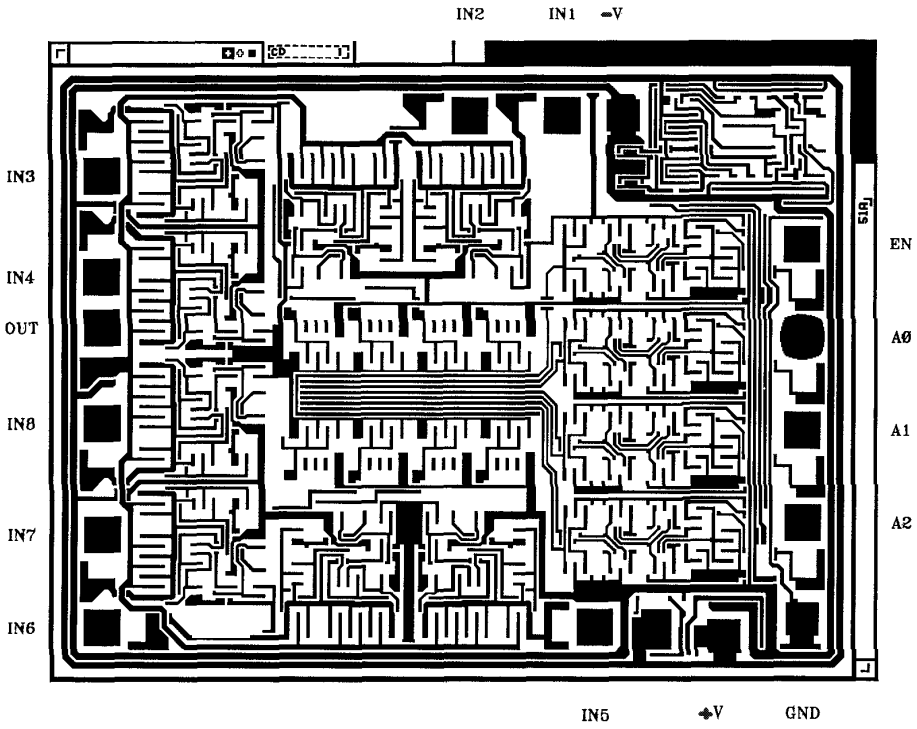
Glassivation.
Type: SiO_2
Thickness: 8 kÅ ± 1 kÅ

Substrate: Dielectrically Isolated (DI)

Assembly related information.
Substrate potential: Insulator
Special assembly instructions: None

NOTE: Pad numbers reflect terminal numbers when placed in case outlines E and X (see Figure 1) for device type 01.

FIGURE A-1. Die bonding pad locations and electrical functions.



Device types 02 and 03.

Die physical dimensions.
Die size: 3050 x 2360 microns
Die thickness: 19 ± 1 mils

Interface materials.
Top metallization: Al/Si/Cu 16.0 kÅ ± 2 kÅ
Backside metallization: None.

Glassivation.
Type: PSG
Thickness: 8 kÅ ± 1 kÅ

Substrate: Dielectrically Isolated (DI)

Assembly related information.
Substrate potential: Insulator
Special assembly instructions: None

NOTE: Pad numbers reflect terminal numbers when placed in case outlines E and X (see Figure 1) for device types 02 and 03.

FIGURE A-2. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-06-02

Approved sources of supply for SMD 5962-96742 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9674201TEC	3/	HS1-508ARH-T
5962R9674201TXC	3/	HS9-508ARH-T
5962R9674201QEC	3/	HS1-508ARH-8
5962R9674201QXC	3/	HS9-508ARH-8
5962R9674201VEC	3/	HS1-508ARH-Q
5962R9674201VXC	3/	HS9-508ARH-Q
5962R9674201V9A	3/	HS0-508ARH-Q
5962R9674202TEC	34371	HS1-508BRH-T
5962R9674202TXC	34371	HS9-508BRH-T
5962F9674202QEC	34371	HS1-508BRH-8
5962F9674202QXC	34371	HS9-508BRH-8
5962F9674202VEC	34371	HS1-508BRH-Q
5962F9674202VXC	34371	HS9-508BRH-Q
5962F9674202V9A	34371	HS0-508BRH-Q
5962F9674203VEC	34371	HS1-508BEH-Q
5962F9674203VXC	34371	HS9-508BEH-Q
5962F9674203V9A	34371	HS0-508BEH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406