

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R091-97	96-11-20	Monica L. Poelking
B	Add footnote to dose rate upset and dose rate survivability in section 1.5. Add test circuit and make changes to voltage level in figure 4. Incorporate revision A into document. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - LTG	03-11-20	Thomas M. Hess
C	Add device types 02 and 03. Delete RHA level "H" for device type 01. Editorial changes throughout. - LTG	04-08-02	Thomas M. Hess
D	Correct radiation features for device type 02 in section 1.5 and add footnote 8/. Correct footnotes 2/ and 8/ in Table IA. Correct SEP test limit in the table IB. Correct paragraph 4.4.4.1. Update boilerplate paragraphs to current requirements of MIL-PRF-38535. - MAA	09-09-09	Thomas M. Hess
E	Make corrections to table IA, output voltage tests V_{OH} and V_{OL} , change condition V_{IN} - jak	11-02-02	David J. Corbett
F	Add footnote 8 to figure 4. Add equivalent test circuit to figure 4. - jak	12-07-24	Thomas M. Hess
G	To correct switching wave forms input/output test limits to figure 4. Add test equivalent circuits and footnote 5 to figure 4. Add paragraph 2.2 for ASTM F1192 document. Delete class M requirements throughout.—MAA	13-02-19	Thomas M. Hess
H	Add footnote 4/ for capacitance limit for measurements of propagation delay time to table IA. - MAA	13-09-12	Thomas M. Hess
J	Update quiescent supply current (IDDQ) limit to table IA. - PHN	17-10-25	Thomas M. Hess
K	Update to current boilerplate paragraphs - jwc	24-05-29	Muhammad Akbar

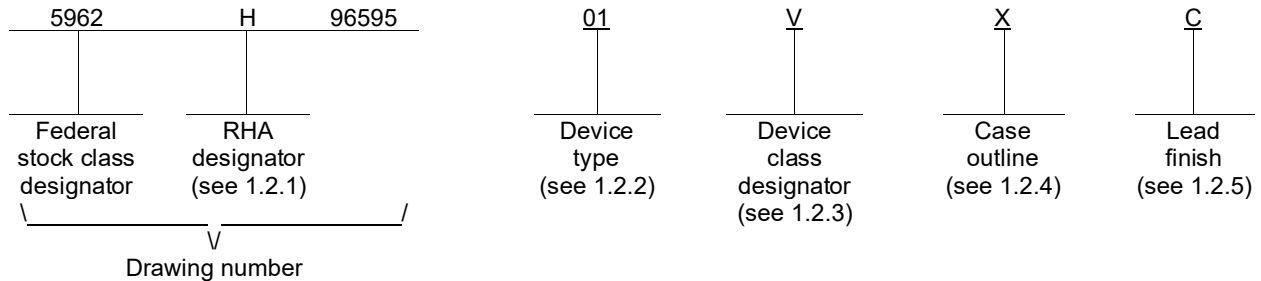


REV SHEET																				
REV SHEET	K	K	K																	
REV STATUS OF SHEETS	15	16	17																	
PMIC N/A	PREPARED BY Thanh V. Nguyen			DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/Land-and-Maritime																
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Thanh V. Nguyen			MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, NONINVERTING OCTAL BUFFER/LINE DRIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON																
	APPROVED BY Monica L. Poelking																			
	DRAWING APPROVAL DATE 96-05-13																			
AMSC N/A	REVISION LEVEL K			SIZE A	CAGE CODE 67268	5962-96595														
SHEET 1 OF 17																				

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ACTS541	Radiation hardened, non-inverting octal buffer/line driver with three-state outputs, TTL compatible inputs
02	54ACTS541E	Enhanced radiation hardened, non-inverting octal buffer/line driver with three-state outputs, TTL compatible inputs
03	54ACTS541E	Enhanced radiation hardened, non-inverting octal buffer/line driver with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
X	CDFP4-F20	20	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V _{DD}).....	-0.3 V dc to +7.0 V dc
DC input voltage range (V _{IN}).....	-0.3 V dc to V _{DD} + 0.3 V dc
DC output voltage range (V _{OUT}).....	-0.3 V dc to V _{DD} + 0.3 V dc
DC input current, any one input (I _{IN}).....	±10 mA
Latch-up immunity current (I _{LU}).....	±150 mA
Storage temperature range (T _{STG}).....	-65°C to +150°C
Lead temperature (soldering, 5 seconds).....	+300°C
Case outline R and X (device type 01).....	See MIL-STD-1835
Case outline X (device types 02 and 03).....	15°C/W
Junction temperature (T _J).....	+175°C
Maximum package power dissipation (P _D):	
Device type 01.....	1.0 W
Device types 02 and 03.....	3.2 W 4/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V _{DD}):	
Device type 01.....	+4.5 V dc to +5.5 V dc
Device types 02 and 03.....	+3.0 V dc to +5.5 V dc
Input voltage range (V _{IN}).....	+0.0 V dc to V _{DD}
Output voltage range (V _{OUT}).....	+0.0 V dc to V _{DD}
Case operating temperature range (T _C).....	-55°C to +125°C
Maximum input rise or fall time rate at V _{DD} = 4.5 V (t _r , t _f).....	1 ns/V 5/

1.5 Radiation features. 6/

Maximum total dose available:	
Device type 01 (dose rate = 50 – 300 rad (Si)/s).....	500 krad (Si) 7/
Device type 02 (effective dose rate = 1 rad (Si)/s).....	1 Mrads (Si) 8/
Device type 03 (dose rate = 50 – 300 rad (Si)/s).....	500 krad (Si) 7/
Single event phenomenon (SEP):	
Device type 01:	
No SEU occurs at effective LET (see 4.4.4.4).....	≤ 80 MeV/(mg/cm ²) 9/
No SEL occurs at effective LET (see 4.4.4.4).....	≤ 120 MeV/(mg/cm ²) 9/
Device types 02 and 03:	
No SEU occurs at effective LET (see 4.4.4.4).....	≤ 108 MeV/(mg/cm ²) 9/
No SEL occurs at effective LET (see 4.4.4.4).....	≤ 120 MeV/(mg/cm ²) 9/
Dose rate upset (20 ns pulse) (device types 01, 02 and 03).....	1 x 10 ⁹ rad (Si)/s 9/ 10/
Dose rate induced latch-up.....	None 9/
Dose rate survivability (device types 01, 02 and 03).....	1 x 10 ¹² rad (Si)/s 9/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to V_{SS}.

3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise specified.

4/ Per MIL-STD-883 method 1012.1 section 3.4.1, P_D (Package) = (T_{J(max)} - T_{C (max)}) / θ_{JC}

5/ Derate system propagation delays by difference in rise time to switch point for t_r or t_f > 1ns/V.

6/ Radiation testing is performed on the standard evaluation circuit.

7/ Device types 01 and 03 are tested in accordance with MIL-STD-883, method 1019, condition A.

8/ Device type 02 is irradiated at dose rate = 50 - 300 rad (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment.

9/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

10/ This limit is applicable for device types 01, 02, 03 with V_{DD} ≥ 4.5 V. Device types 02 and 03 do not meet this limit at V_{DD} < 4.5 V.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <https://www.astm.org>.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as specified on figure 4.

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3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions <u>1/ 2/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device type	V _{DD}	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
High level input voltage	V _{IH}		02, 03	3.0 V	1, 2, 3	2.0		V
			All	4.5 V	1, 2, 3	2.25		
			All	5.5 V	1, 2, 3	2.75		
Low level input voltage	V _{IL}		02, 03	3.0 V	1, 2, 3		0.8	V
			All	4.5 V	1, 2, 3		0.8	
			All	5.5 V	1, 2, 3		0.8	
High level output voltage	V _{OH}	For all inputs affecting output under test, V _{IN} = V _{DD} or V _{SS} For all other inputs V _{IN} = V _{DD} or V _{SS} I _{OH} = -8 mA	02, 03	3.0 V	1, 2, 3	2.4		V
		For all inputs affecting output under test, V _{IN} = V _{DD} or V _{SS} For all other inputs V _{IN} = V _{DD} or V _{SS} I _{OH} = -12 mA	All	4.5 V	1, 2, 3	3.15		V
Low level output voltage	V _{OL}	For all inputs affecting output under test, V _{IN} = V _{DD} or V _{SS} For all other inputs V _{IN} = V _{DD} or V _{SS} I _{OL} = +8 mA	02, 03	3.0 V	1, 2, 3		0.4	V
		For all inputs affecting output under test, V _{IN} = V _{DD} or V _{SS} For all other inputs V _{IN} = V _{DD} or V _{SS} I _{OL} = +12 mA	All	4.5 V	1, 2, 3		0.4	V
Input current high	I _{IH}	For input under test, V _{IN} = V _{DD} For all other inputs V _{IN} = V _{DD} or V _{SS}	All	5.5 V	1, 2, 3		+1.0	μA
Input current low	I _{IL}	For input under test, V _{IN} = V _{SS} For all other inputs V _{IN} = V _{DD} or V _{SS}	All	5.5 V	1, 2, 3		-1.0	μA
Output current (source)	I _{OH} <u>4/</u>	For output under test V _{OUT} = V _{DD} - 0.4 V; For all other inputs, V _{IN} = V _{DD} or V _{SS}	02, 03	3.0 V and 3.6 V	1, 2, 3	-8.0		mA
		For output under test V _{OUT} = V _{DD} - 0.4 V; For all other inputs, V _{IN} = V _{DD} or V _{SS}	All	4.5 V and 5.5 V	1, 2, 3	-12.0		mA
Output current (sink)	I _{OL} <u>4/</u>	For output under test V _{OUT} = 0.4 V; For all other inputs V _{IN} = V _{DD} or V _{SS}	02, 03	3.0 V and 3.6 V	1, 2, 3	8.0		mA
		For output under test V _{OUT} = 0.4 V; For all other inputs V _{IN} = V _{DD} or V _{SS}	All	4.5 V and 5.5 V	1, 2, 3	12.0		mA

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions <u>1/ 2/</u> -55°C ≤ T _c ≤ +125°C unless otherwise specified	Device type	V _{DD}	Group A subgroups	Limits <u>3/</u>		Unit	
						Min	Max		
Quiescent supply current delta, TTL input levels	ΔI_{DDQ} <u>5/</u>	For input under test V _{IN} = V _{DD} - 2.1V For all other inputs V _{IN} = V _{DD} or V _{SS}	All	4.5 V and 5.5 V	1, 2, 3		1.6	mA	
Quiescent supply current	I _{DDQ}	V _{IN} = V _{DD} or V _{SS}	All	5.5 V	1, 2, 3		10.0	μA	
		V _{IN} = V _{DD} or V _{SS}	Max Rated RHA	01	5.5 V	1		50.0	μA
		V _{IN} = V _{DD} or V _{SS}	Max Rated RHA	02	5.5 V	1		130.0	μA
		V _{IN} = V _{DD} or V _{SS}	Max Rated RHA	03	5.5 V	1		50.0	μA
Short circuit output current	I _{OS} <u>6/ 7/</u>	For output under test, V _{OUT} = V _{DD} and V _{SS}	02, 03	3.0 V	1, 2, 3		±150	mA	
			All	5.5 V	1, 2, 3		±300		
Three-state output leakage current high	I _{OZH}	$\bar{G}_m = 5.5 V$ For all other inputs V _{IN} = V _{DD} or V _{SS} V _{OUT} = V _{DD}	All	5.5 V	1, 2, 3		+30.0	μA	
Three-state output leakage current low	I _{OZL}	$\bar{G}_m = 5.5 V$ For all other inputs V _{IN} = V _{DD} or V _{SS} V _{OUT} = V _{SS}	All	5.5 V	1, 2, 3		-30.0	μA	
Input capacitance	C _{IN}	f = 1 MHz, see 4.4.1c	All	0.0 V	4		15.0	pF	
Output capacitance	C _{OUT}	f = 1 MHz, see 4.4.1c	All	0.0 V	4		15.0	pF	
Switching power dissipation	P _{SW} <u>8/</u>	C _L = 50 pF, per switching output	02, 03	3.0 V and 3.6 V	4, 5, 6		0.84	mW/ MHz	
			All	4.5 V and 5.5 V	4, 5, 6		2.1		
Functional test	<u>9/</u>	See 4.4.1b	02, 03	3.0 V and 3.6 V	7, 8	L	H		
			All	4.5 V and 5.5 V	7, 8	L	H		
Propagation delay time, A _n to Y _n	t _{PLH} <u>10/</u>	C _L = 30 pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	1.0	11.0	ns	
			02, 03	4.5 V and 5.5 V	9, 10, 11	1.0	8.0		
		C _L = 50 pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	1.0	15.0	ns	
			All	4.5 V and 5.5 V	9, 10, 11	1.0	11.0		

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions <u>1/</u> <u>2/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device type	V _{DD}	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Propagation delay time, A _n to Y _n	<u>t_{PHL}</u> <u>10/</u>	C _L = 30 pF minimum <u>4/</u> See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	1.0	14.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	1.0	10.0	
		C _L = 50 pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	1.0	18.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	1.0	14.0	
Propagation delay time, output enable, \overline{G}_m to Y _n	<u>t_{PZH}</u> <u>10/</u>	C _L = 30 pF minimum <u>4/</u> See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	15.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	2.0	11.0	
		C _L = 50 pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	19.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	2.0	15.0	
	<u>t_{PZL}</u> <u>10/</u>	C _L = 30 pF minimum <u>4/</u> See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	14.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	2.0	10.0	
		C _L = 50 pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	18.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	2.0	14.0	
Propagation delay time, output disable, \overline{G}_m to Y _n	<u>t_{PHZ}</u> <u>10/</u>	C _L = 30 pF minimum <u>4/</u> See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	13.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	2.0	9.0	
		C _L = 50 pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	17.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	2.0	13.0	
Propagation delay time, output disable, \overline{G}_m to Y _n	<u>t_{PLZ}</u> <u>10/</u>	C _L = 30 pF minimum <u>4/</u> See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	12.0	ns
			02, 03	4.5 V and 5.5 V	9, 10, 11	2.0	8.0	
		C _L = 50 pF minimum See figure 4	02, 03	3.0 V and 3.6 V	9, 10, 11	2.0	16.0	ns
			All	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

- 1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{DDQ} and ΔI_{DD} tests, the output terminals shall be open. When performing the I_{DDQ} and ΔI_{DD} tests, the current meter shall be placed in the circuit such that all current flows through the meter.
- 2/ RHA device type 01 and 03 devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F and G of irradiation. RHA device type 02 devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F, G and H of irradiation.
 Device type 01 is tested in accordance with MIL-STD-883, method 1019, condition A for RHA level "G".
 Device type 02 is irradiated at dose rate = 50 - 300 rad (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment. Device 02 is tested for RHA level "H".
 Device type 03 is tested in accordance with MIL-STD-883, method 1019, condition A for RHA level "G".

 Each device type supplied to this drawing is guaranteed to comply with specification table IA through all RHA levels up to, and including, the maximum RHA level listed in section 1.5 Radiation features. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A=+25°C.
- 3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to V_{SS} and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.
- 4/ This test is guaranteed based on characterization data but not tested.
- 5/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at V_{IN} = V_{DD} - 2.1 V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed. For the preferred method, a minimum of one input shall be tested. All other inputs shall be guaranteed, if not tested, to the limits specified in table IA, herein.
- 6/ This parameter is supplied as design limit but not guaranteed or tested.
- 7/ No more than one output should be shorted at a time for a maximum duration of one second.
- 8/ This value is calculated during the design/qualification process and is supplied as a design limit but is not tested. The power dissipation per switching output (P_{SW}) is calculated for a logic device by using power dissipation equation P_{TOTAL}.
 To determine total power use the formula:

$$P_{TOTAL} = (N_{SWO} \times P_{SW/OUTPUT} \times f) + (Load \times P_{RDY} \times I_{OL} \times V_{OL}) + (Load \times P_{RDY} \times I_{OH} \times V_{DP})$$
 Wherein, N_{SWO} = number of switching outputs, P_{SW/OUTPUT} = Power dissipation per switching output in mW/MHz from Table IA and f is the operating frequency that the outputs are switching at V_{DP} = V_{DD} - V_{OH}, Load = the number of loads that are being driven, Loads = N_{SWO}.
- 9/ The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For V_{OUT} measurements, L ≤ 0.5 V and H ≥ 4.0 V and are tested at V_{DD} = 4.5 V and V_{DD} = 5.5 V; L ≤ 0.5 V and H ≥ 2.5 V and are tested at V_{DD} = 3.0 V and V_{DD} = 3.6 V.
- 10/ For propagation delay tests, all paths must be tested.

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TABLE IB. SEP test limits. 1/ 2/

Device type	V _{DD} = 4.5 V for device type 01 3/ V _{DD} = 3.0 V for device types 02 and 03		Bias V _{DD} = 5.5 V for Latch-up test no SELat effective LET = 4/ 5/
	Effective LET no upsets (SEU)	Maximum device cross section	
01	LET ≤ 80 MeV/(mg/cm ²)	6 x 10 ⁻⁹ cm ² /bit 6/	LET ≤ 120 MeV/(mg/cm ²)
02, 03	LET ≤ 108 MeV/(mg/cm ²)	7/	LET ≤ 120 MeV/(mg/cm ²)

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Tested for upsets at operating temperature, T_A = +25°C ± 10°C.

4/ Tested at operating temperature, T_A = +125°C ± 10°C for latch-up.

5/ Tested to a LET of 120 MeV/(mg/cm²) with no latch-up (SEL).

6/ The bit error cross section is established from a "hard" D flip-flop that is based on the Weibull distribution from SEU testing, and is performed on the Standard Evaluation Circuit (SEC).

7/ Tested to a LET of 120 MeV/(mg/cm²) with no single event upsets (SEU).

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Device type	All		
Case outlines	R and X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\bar{G}1$	11	Y8
2	A1	12	Y7
3	A2	13	Y6
4	A3	14	Y5
5	A4	15	Y4
6	A5	16	Y3
7	A6	17	Y2
8	A7	18	Y1
9	A8	19	$\bar{G}2$
10	V _{SS}	20	V _{DD}

FIGURE 1. Terminal connections.

Inputs			Outputs
$\bar{G}1$	$\bar{G}2$	A _n	Y _n
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance

FIGURE 2. Truth table

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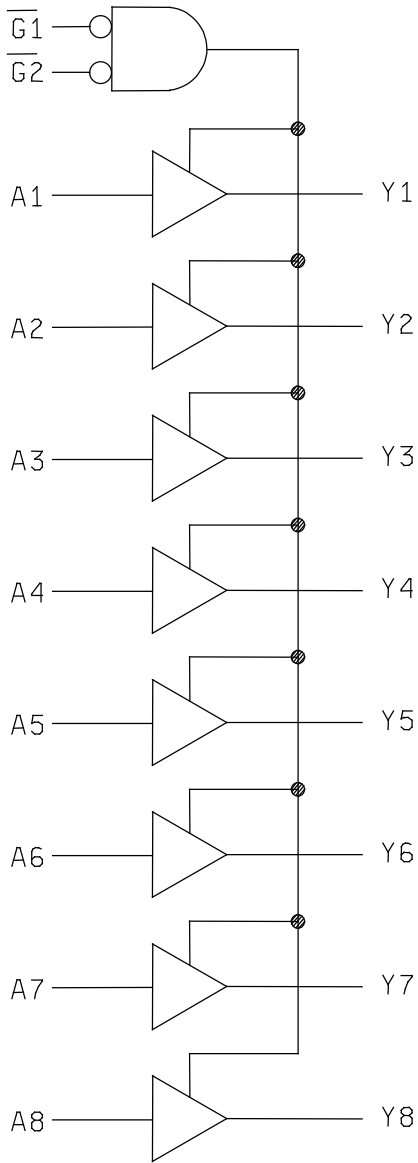
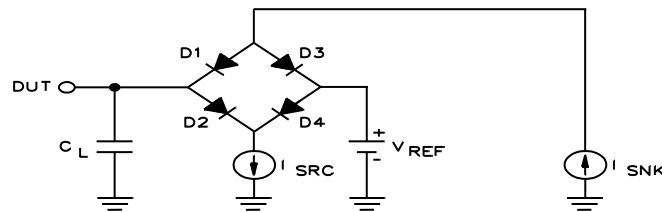
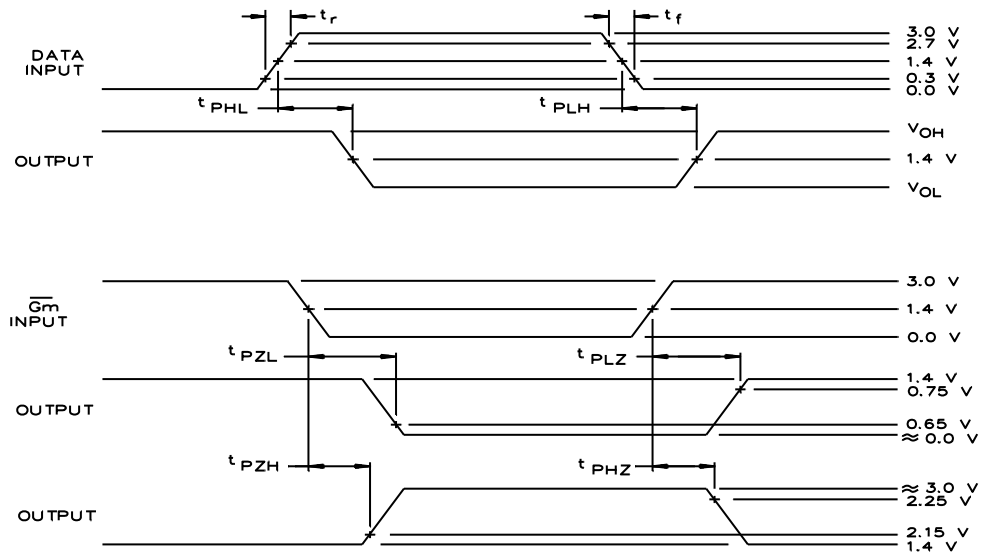
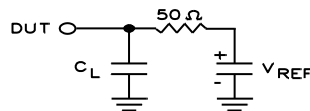


FIGURE 3. Logic diagram.

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TEST CIRCUIT A
OR EQUIVALENT



TEST CIRCUIT B
OR EQUIVALENT

NOTES:

1. $V_{REF} = 1.4 \text{ V}$.
2. $C_L = 50 \text{ pF}$ minimum or equivalent (includes test jig and probe capacitance).
3. I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} , t_{PLH} , t_{PZL} , and t_{PZH} measurements. I_{SRC} is set to -12.0 mA and I_{SNK} is set to 12.0 mA for t_{PLZ} and t_{PHZ} measurements. . Note, either test circuit A or B may be used for these measurements.
4. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $f \leq 10 \text{ MHz}$; $t_r = 1.0 \text{ ns/V} \pm 0.3 \text{ ns/V}$; $t_f = 1.0 \text{ ns/V} \pm 0.3 \text{ ns/V}$; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V , respectively.
5. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

FIGURE 4. Switching waveforms and test circuit.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. For C_{IN} and C_{OUT} , test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>2/ 3/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 <u>3/</u>
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 and 7.

2/ PDA applies to subgroups 1, 7, and delta's.

3/ Delta limits, as specified in table IIB herein, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameters	Symbol	Delta limits
Output voltage low	V _{OL}	±100 mV
Output voltage high	V _{OH}	±100 mV

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

- a. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related an effect is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The upset test temperature shall be $+25^{\circ}\text{C}$. The latchup test temperature shall be at the maximum rated operating temperature $\pm 10^{\circ}\text{C}$.
- f. Bias conditions shall be defined by the manufacturer for latchup measurements.
- g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, P.O. Box 3990, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA test conditions of SEP.
- b. Number of upsets (SEU).
- c. Number of transients (SET).
- d. Occurrence of latch-up (SEL).

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-05-29

Approved sources of supply for SMD 5962-96595 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr>

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962G9659501QXA	65342	UT54ACTS541UQAG
5962G9659501QXC	65342	UT54ACTS541UQCG
5962G9659501VXA	65342	UT54ACTS541UVAG
5962G9659501VXC	65342	UT54ACTS541UVCG
5962H9659501QRA	<u>3/</u>	UT54ACTS541PQAH
5962H9659501QXA	<u>3/</u>	UT54ACTS541UQAH
5962H9659501VRA	<u>3/</u>	UT54ACTS541PVAH
5962H9659501VXA	<u>3/</u>	UT54ACTS541UVAH
5962H9659502QXA	65342	UT54ACTS541EUQAH
5962H9659502QXC	65342	UT54ACTS541EUQCH
5962H9659502VXA	65342	UT54ACTS541EUVAH
5962H9659502VXC	65342	UT54ACTS541EUVCH
5962G9659503QXA	65342	UT54ACTS541EUQAG
5962G9659503QXC	65342	UT54ACTS541EUQCG
5962G9659503VXA	65342	UT54ACTS541EUVAG
5962G9659503VXC	65342	UT54ACTS541EUVCG

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE number

65342

Vendor name and address

Frontgrade Colorado Springs LLC
4350 Centennial Boulevard
Colorado Springs, Colorado 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.