REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. – LTG	01-11-01	Thomas M. Hess
B	Update the boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	09-08-18	Thomas M. Hess
C	Update radiation features in section 1.5 and SEP table IB. Update boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - jwc	16-03-28	Thomas M. Hess
D	Manufacture (CAGE code 65342) name change. Update boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - jwc	22-09-01	Muhammad A. Akbar

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets																						
REV																						
SHEET																						
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19			

PMIC N/A

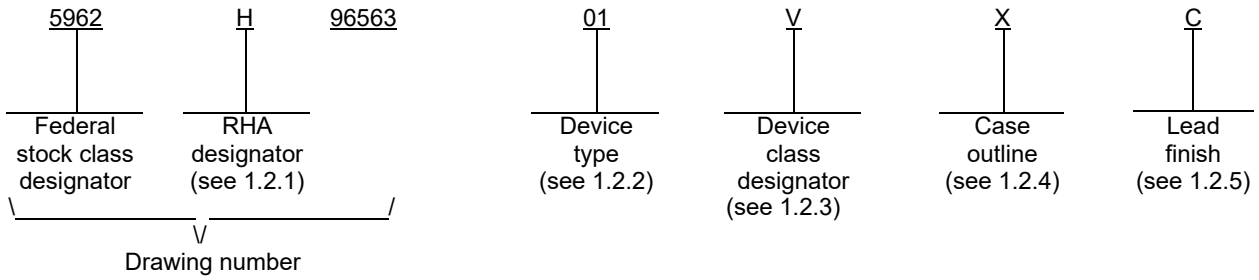
STANDARD MICROCIRCUIT DRAWING	PREPARED BY Larry T. Gauder CHECKED BY Charles F. Saffle	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	APPROVED BY Monica L. Poelking DRAWING APPROVAL DATE 97-01-07	MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, SYNCHRONOUS 4-BIT UP/DOWN BCD DECADE COUNTER, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL D	SIZE A	CAGE CODE **67268**	**5962-96563**
		SHEET 1 OF 19		

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACTS190	Radiation hardened, synchronous 4-bit up/down BCD decade counter, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
X	CDFP4-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD})	-0.3 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.3 V dc to V_{DD} + 0.3 V dc
DC output voltage range (V_{OUT})	-0.3 V dc to V_{DD} + 0.3 V dc
DC input current, any one input (I_{IN})	±10 mA
Latch-up immunity current (I_{LU})	±150 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Maximum package power dissipation (P_D)	1.0 W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{DD}
Output voltage range (V_{OUT})	+0.0 V dc to V_{DD}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise or fall time at V_{DD} = 4.5 V (t_r, t_f)	1 ns/V 4/

1.5 Radiation features. 5/

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	1 Mrads (Si)
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.4)	≤ 120 MeV/(mg/cm^2) 6/
No SEU occurs at effective LET (see 4.4.4.4)	≤ 80 MeV/(mg/cm^2) 6/
Dose rate induced upset (20 ns pulse)	1 x 10^9 Rads (Si)/s 6/
Dose rate survivability	1 x 10^{12} Rads (Si)/s 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise noted.
4/ Derate system propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.
5/ Radiation testing is performed on the standard evaluation circuit.
6/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org/.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 2/		Unit
						Min	Max	
High level input voltage	V_{IH}		All	4.5 V	1, 2, 3	2.25		V
		M, D, P, L, R, F, G, H 3/	All		1	2.25		
			All	5.5 V	1, 2, 3	2.75		
		M, D, P, L, R, F, G, H 3/	All		1	2.75		
Low level input voltage	V_{IL}		All	4.5 V	1, 2, 3		0.8	V
		M, D, P, L, R, F, G, H 3/	All		1		0.8	
			All	5.5 V	1, 2, 3		0.8	
		M, D, P, L, R, F, G, H 3/	All		1, 2, 3	3.15		
High level output voltage	V_{OH}	For all inputs affecting output under test $V_{IN} = V_{DD}$ or V_{SS}, $I_{OH} = -8.0$ mA	All	5.5 V	1, 2, 3	3.15		V
		M, D, P, L, R, F, G, H 3/	All		1	3.15		
Low level output voltage	V_{OL}	For all inputs affecting output under test $V_{IN} = V_{DD}$ or V_{SS}, $I_{OL} = 8.0$ mA	All	5.5 V	1, 2, 3		0.4	
		M, D, P, L, R, F, G, H 3/	All				0.4	
Input current high	I_{IH}	For input under test $V_{IN} = 5.5$ V. For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		+1.0	µA
		M, D, P, L, R, F, G, H 3/	All		1		+1.0	
Input current low	I_{IL}	For input under test $V_{IN} = V_{SS}$, For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		-1.0	A
		M, D, P, L, R, F, G, H 3/	All		1		-1.0	
Quiescent supply current delta, TTL input levels	ΔI_{DD} 4/	For input under test $V_{IN} = V_{DD} - 2.1$ V For all other inputs $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		1.6	mA
		M, D, P, L, R, F, G, H 3/	All		1		1.6	
Quiescent supply current	I_{DDQ}	$V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		10.0	µA
		M, D, P, L, R, F, G, H 3/	All		1		10.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Output current (Sink)	I_{OL} 5/	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4$ V	All	4.5 V and 5.5 V	1, 2, 3	8.0		mA
Output current (Source)	I_{OH} 5/	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD} - 0.4$ V	All	4.5 V and 5.5 V	1, 2, 3	-8.0		mA
Short circuit output current	I_{OS} 6/ 7/	$V_{OUT} = V_{DD}$ and V_{SS}	All	5.5 V	1, 2, 3		±200	mA
Input capacitance	C_{IN}	f = 1 MHz, see 4.4.1c	All	0.0 V	4		15.0	pF
Output capacitance	C_{OUT}	f = 1 MHz, see 4.4.1c	All	0.0 V	4		15.0	pF
Switching power dissipation	P_{SW} 8/	C_L = 50 pF, per switching output	All	4.5 V and 5.5 V	4, 5, 6		2.2	mW/MHz
Functional test	9/	$V_{IH} = 0.5\ V_{DD}$, $V_{IL} = 0.8\ V_{DD}$ See 4.4.1b	All	4.5 V and	7, 8	L	H	
		M, D, P, L, R, F, G, H 3/		5.5 V	7	L	H	
Propagation delay time, $\overline{LOAD}$ to Q_X	t_{PLH1} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	19.0	ns
		M, D, P, L, R, F, G, H 3/			9	2.0	19.0	
	t_{PHL1} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	22.0	
		M, D, P, L, R, F, G, H 3/			9	2.0	22.0	
Propagation delay time, A, B, C, or D to Q_X	t_{PLH2} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	19.0	ns
		M, D, P, L, R, F, G, H 3/			9	2.0	19.0	
	t_{PHL2} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	21.0	
		M, D, P, L, R, F, G, H 3/			9	2.0	21.0	
Propagation delay time, CLK to Q_X	t_{PLH3} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	18.0	ns
		M, D, P, L, R, F, G, H 3/			9	2.0	18.0	
	t_{PHL3} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	20.0	
		M, D, P, L, R, F, G, H 3/	I		9	2.0	20.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Propagation delay time, CLK to $\overline{RCO}$	t_{PLH4} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	16.0	ns
		M, D, P, L, R, F, G, H 3/	All		9	2.0	16.0	
	t_{PHL4} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	16.0	
		M, D, P, L, R, F, G, H 3/			9	2.0	16.0	
Propagation delay time, CLK to MAX/MIN	t_{PLH5} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	18.0	ns
		M, D, P, L, R, F, G, H 3/	All		9	2.0	18.0	
	t_{PHL2} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	23.0	
		M, D, P, L, R, F, G, H 3/	All		9	2.0	23.0	
Propagation delay time, D/$\overline{U}$ to $\overline{RCO}$	t_{PLH6} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	16.0	ns
		M, D, P, L, R, F, G, H 3/	All		9	2.0	16.0	
	t_{PHL6} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	18.0	
		M, D, P, L, R, F, G, H 3/	All		9	2.0	18.0	
Propagation delay time, D/$\overline{U}$ to MAX/MIN	t_{PLH7} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	14.0	ns
		M, D, P, L, R, F, G, H 3/	All		9	2.0	14.0	
	t_{PHL7} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	18.0	
		M, D, P, L, R, F, G, H 3/	All		9	2.0	16.0	
Propagation delay time, $\overline{CTEN}$ to $\overline{RCO}$	t_{PLH8} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	ns
		M, D, P, L, R, F, G, H 3/	All		9	2.0	12.0	
	t_{PHL8} 10/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0	16.0	
		M, D, P, L, R, F, G, H 3/	All		9	2.0	16.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Maximum clock frequency	f_{MAX}	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11		71.0	MHz
Setup time, high or low before CLK↑	t_{S1}	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	13.0		ns
		M, D, P, L, R, F, G, H 3/	All		9	13.0		
Setup time, $\overline{CTEN}$ low before CLK↑	t_{S2}	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	13.0		ns
		M, D, P, L, R, F, G, H 3/	All		9	13.0		
Setup time, A, B, C, D high or low before $\overline{LOAD}$↑	t_{S3}	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	7.0		ns
		M, D, P, L, R, F, G, H 3/	All		9	7.0		
Setup time, $\overline{LOAD}$ high or low before CLK↑	t_{S4}	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0		
		M, D, P, L, R, F, G, H 3/	All		9	2.0		
Hold time, high or low after CLK↑	t_{h1}	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0		ns
		M, D, P, L, R, F, G, H 3/	All		9	2.0		
Hold time, low after CLK↑	t_{h2}	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0		
		M, D, P, L, R, F, G, H 3/	All		9	2.0		
Hold time, A, B, C, D high or low after $\overline{LOAD}$↑	t_{h3} 11/	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	2.0		ns
		M, D, P, L, R, F, G, H 3/	All		9	2.0		
CLK pulse width, high or low	t_{W1}	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	7.0		ns
		M, D, P, L, R, F, G, H 3/	All		9	7.0		
$\overline{LOAD}$ pulse width, low	t_{W2}	C_L = 50 pF, see figure 4	All	4.5 V and 5.5 V	9, 10, 11	7.0		ns
		M, D, P, L, R, F, G, H 3/	All		9	7.0		

See footnotes on next sheet.

TABLE IA. Electrical performance characteristics – Continued.

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{DDQ} and ΔI_{DD} tests, the output terminals shall be open. When performing the I_{DDQ} and ΔI_{DD} tests, the current meter shall be placed in the circuit such that all current flows through the meter.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to V_{SS} and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F, G, and H of irradiation. However, these devices are only tested at the "H" level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{DD} - 2.1$ V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed. For the preferred method, a minimum of one input shall be tested. All other inputs shall be guaranteed, if not tested, to the limits specified in table IA, herein.

5/ This test is guaranteed based on characterization data but not tested.

6/ This parameter is supplied as design limit but not guaranteed or tested.

7/ No more than one output should be shorted at a time for a maximum duration of one second.

8/ This value is calculated during the design/qualification process and is supplied as a design limit but is not tested.

9/ The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For V_{OUT} measurements, L ≤ 0.5 V and H ≥ 4.0 V and are tested at V_{DD} = 4.5 V and V_{DD} = 5.5 V.

10/ For propagation delay tests, all paths must be tested.

11/ Based on characterization, hold time (t_{h3}) of 0 ns can be assumed if the data setup time (t_{s3}) is ≥ 10 ns. This is guaranteed but not tested.

TABLE IB. SEP test limits. 1/ 2/

Device Type	V_{DD} = 4.5 V 3/		Bias V_{DD} = 5.5 V, For SEL test
	Effective LET no upsets	Maximum device cross section	no SEL occurs at effective LET 4/ 5/
01	LET≤ 80MeV/(mg/cm^2)	6 x 10^{-9} cm^2/bit 6/	LET ≤ 120 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for upsets at worse case temperature, T_A = +25°C ± 10°C.
4/ Tested at worst case temperature, T_A = +125°C ± 10°C for latch-up.
5/ Tested to a LET of ≥ 120 MeV/(mg/cm^2) with no latch-up (SEL).
6/ The bit error cross section is established from a “hard” D flip-flop that is based on the Weibull distribution from SEU testing, and is performed on the Standard Evaluation Circuit (SEC).

Device type	All		
Case outlines	E and X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	B	9	D
2	Q_B	10	C
3	Q_A	11	$\overline{LOAD}$
4	$\overline{CTEN}$	12	MAX/MIN
5	$D/\overline{U}$	13	$\overline{RCO}$
6	Q_C	14	CLK
7	Q_D	15	A
8	V_{SS}	16	V_{DD}

FIGURE 1. Terminal connections.

Function	CLK	$D/\overline{U}$	$\overline{CTEN}$	$\overline{LOAD}$
Count up	↑	L	L	H
Count down	↑	H	L	H
Asynchronous reset	X	X	X	L
No change	X	X	H	H

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high clock transition

FIGURE 2. Truth table.

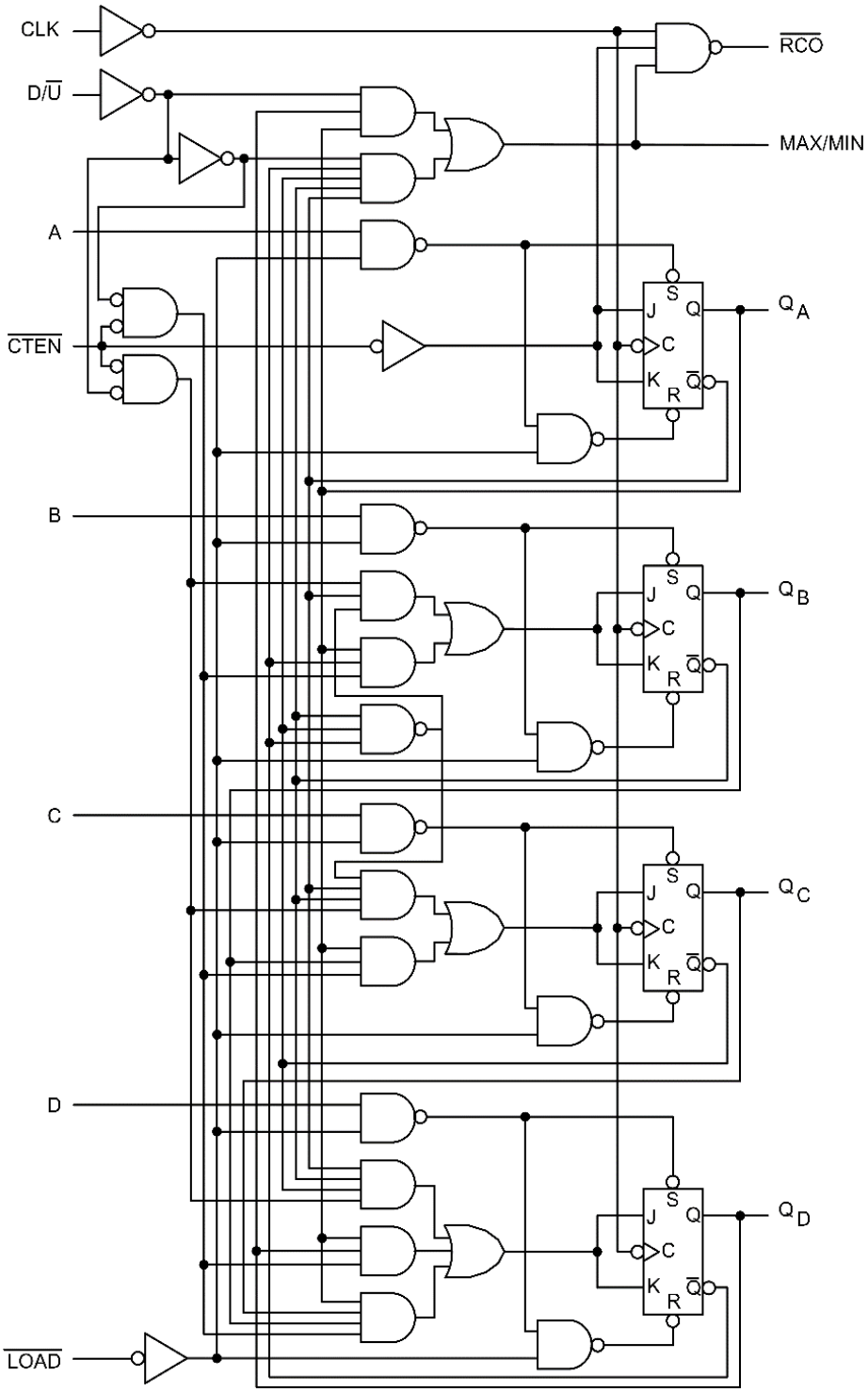
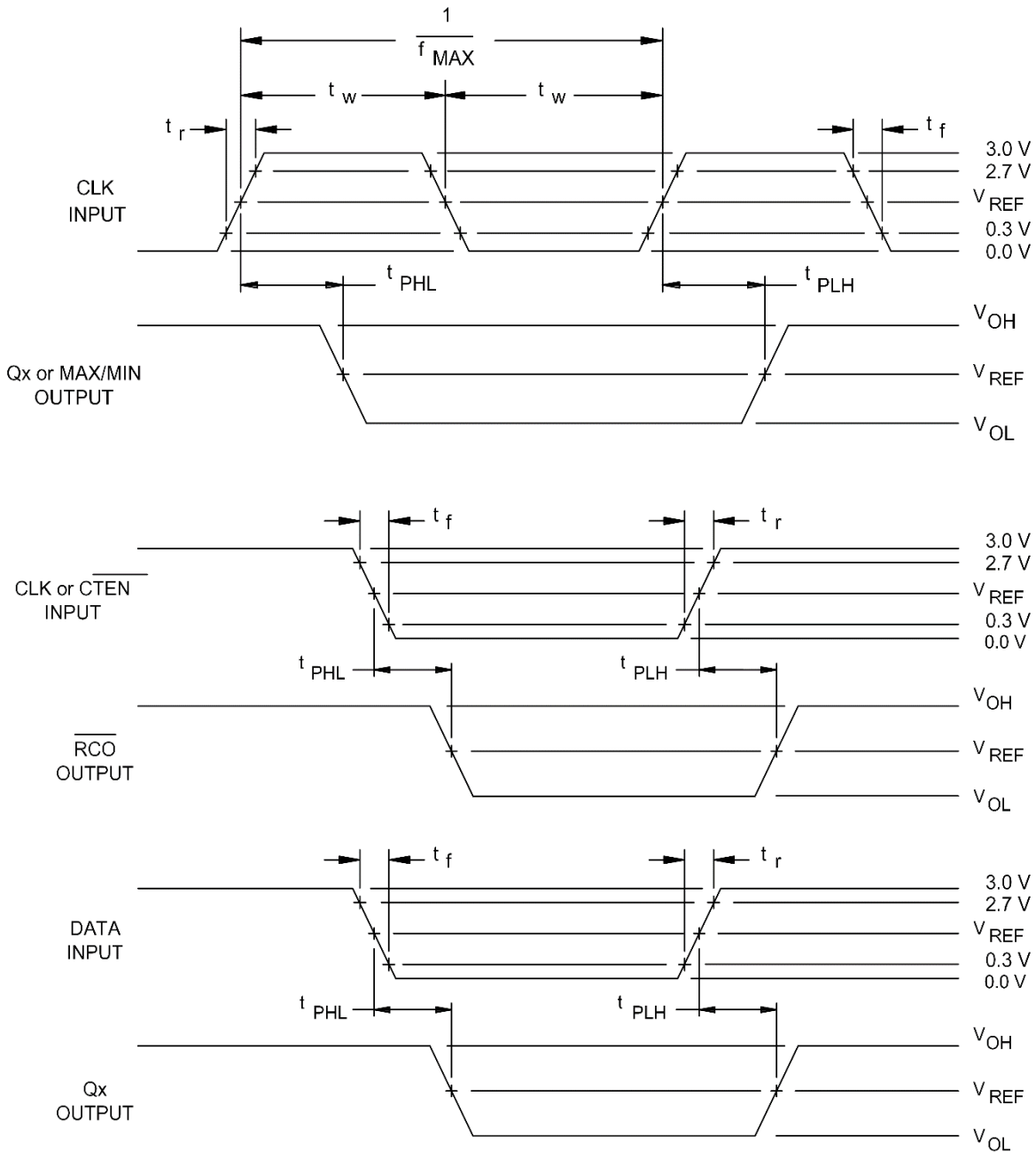


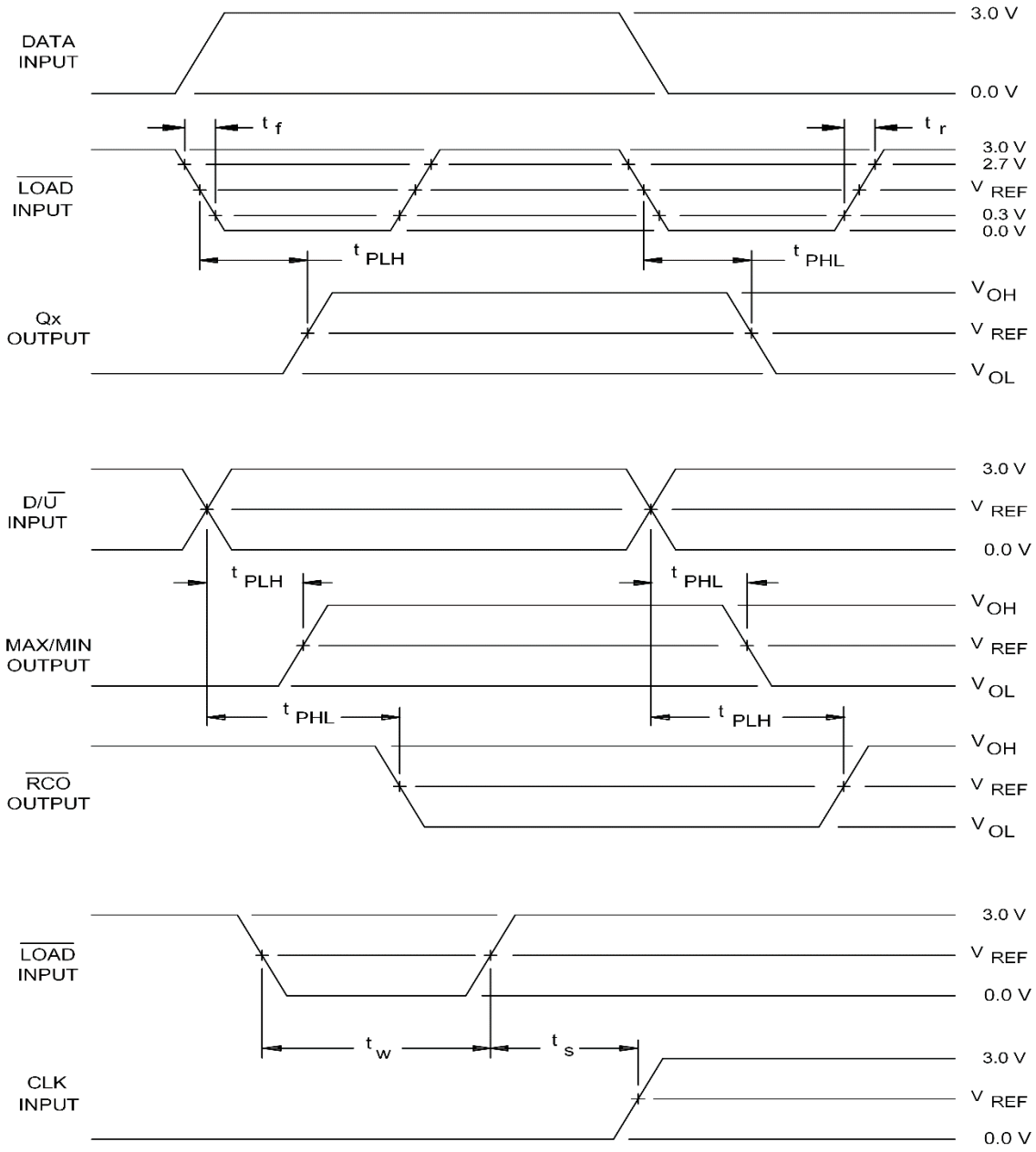
FIGURE 3. Logic diagram



NOTES:

1. V_{REF} = 1.4 V.

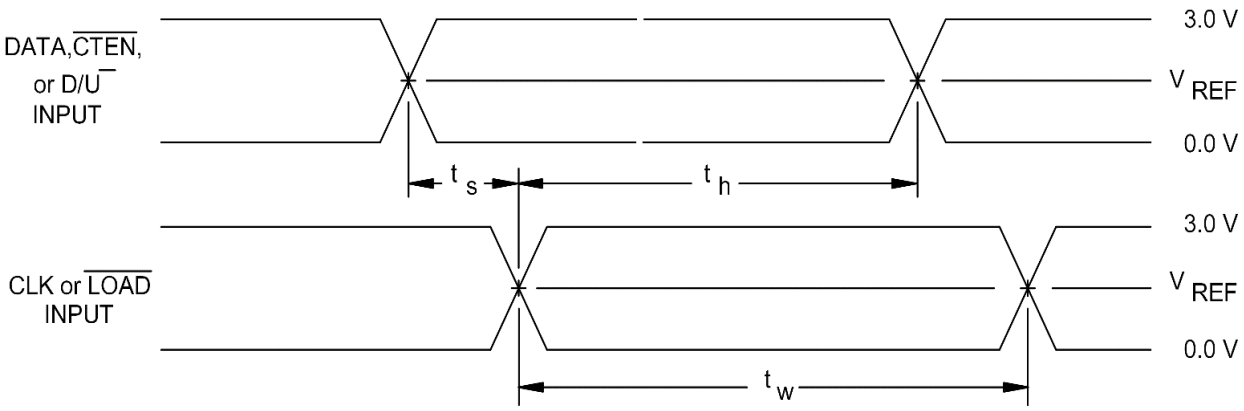
FIGURE 4. Switching waveforms and test circuit.

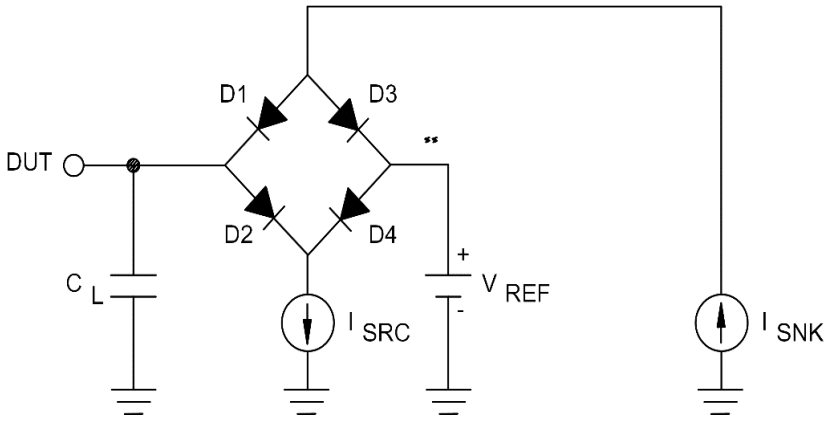


NOTES:

1. V_{REF} = 1.4 V.

FIGURE 4. Switching waveforms and test circuit – Continued.





NOTES:

1/ VREF = 1.4 V
2/ C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
3/ I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} and t_{PLH} measurements.
4/ Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; f ≤ 10 MHz; t_r = 1.0 V/ns ±0.3 V/ns; t_f = 1.0 V/ns ±0.3 V/ns; t_r and t_f shall be measured from 0 V to 3.0 V and from 3.0 V to 0 V, respectively.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{OUT} shall be measured only for the initial test and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroups 1 and 7.
2/ PDA applies to subgroups 1, 7, and delta's.
3/ Delta limits as specified in table IIB herein, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameters	Symbol	Delta limits
Output voltage low	V_{OL}	±100 mV
Output voltage high	V_{OH}	±100 mV

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process change which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions for SEP.

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latch-up (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-08-29

Approved sources of supply for SMD 5962-96563 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9656301VEA	65342	UT54ACTS190PVAH
5962H9656301VXA	65342	UT54ACTS190UVAH
5962H9656301VEC	65342	UT54ACTS190PVCH
5962H9656301VXC	65342	UT54ACTS190UVCH
5962H9656301QEA	65342	UT54ACTS190PQAH
5962H9656301QXA	65342	UT54ACTS190UQAH
5962H9656301QEC	65342	UT54ACTS190PQCH
5962H9656301QXC	65342	UT54ACTS190UQCH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	CAES Colorado Springs, Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3701

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.